PRELIMINARY

Basic Four® Model 4309 Ergonomic Video Display Terminal (Machine Type 4309) Service Manual

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Basic Four® Model 4309 Ergonomic Video Display Terminal (Machine Type 4309) Service Manual

SD 8070P

April 1983

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PREFACE

This manual contains service information for the Model 4309 Ergonomic Video Display Terminal (Machine Type 4309). The information is presented as an aid and will enable field service personnel to install, operate, and maintain the equipment.

The major topics covered in this manual are:

Section I Introduction

Section II Installation and Operation

Section III Functional Description

Section IV Maintenance

Section V Removal/Replacement/Spare Parts

Section VI Reference Data

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications, as temporarily permitted by regulation. It has not been tested for compliance with the limits for Class A Computing Devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference, in which case the User at his own expense will be required to take whatever measures may be required to correct the interference.

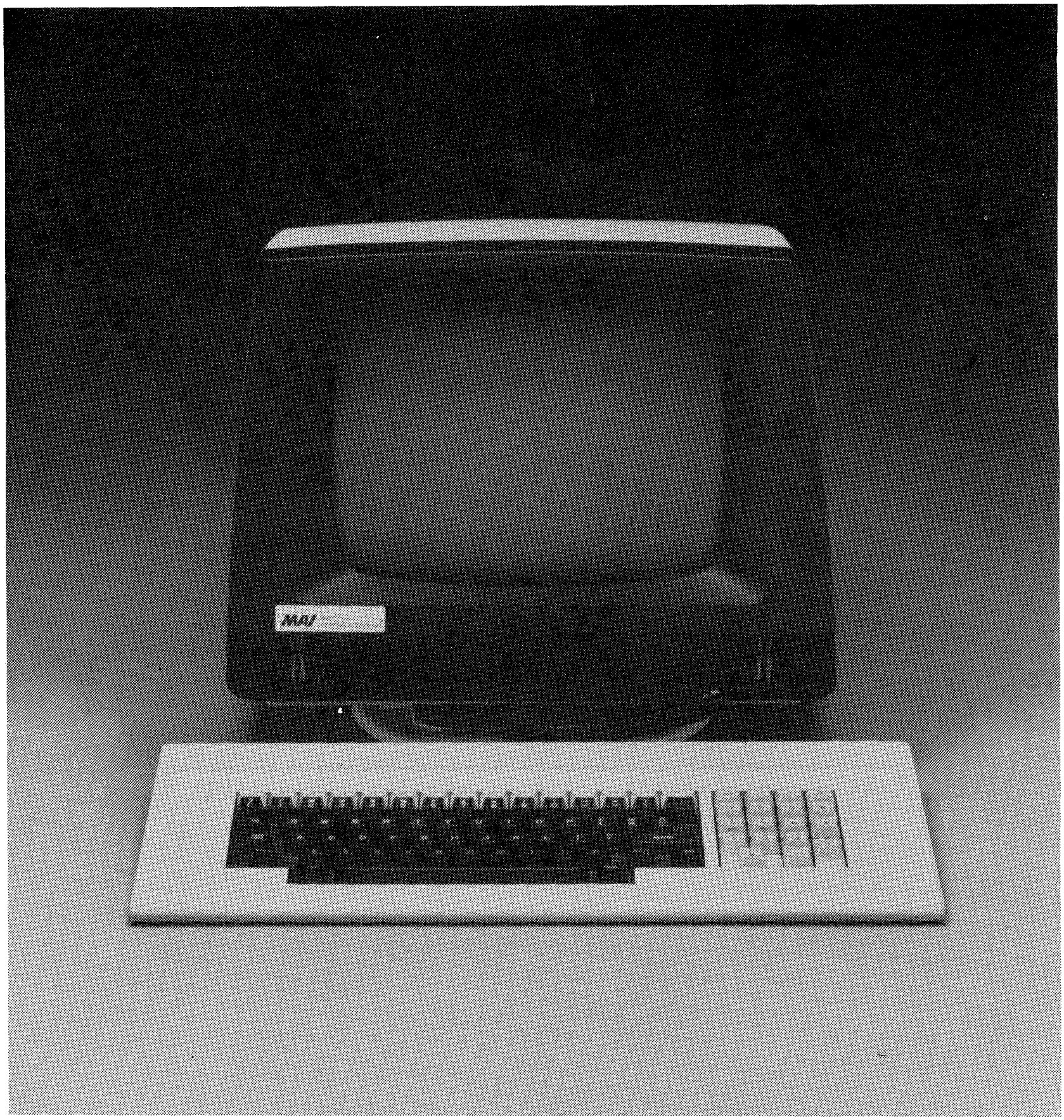

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Figure 1-1. Model 4309 Ergonomic Video Display Terminal

SECTION I

INTRODUCTION

1.1 GENERAL

The Model 4309 Ergonomic Video Display Terminal (Machine Type 4309), hereafter referred to as EVDT, is a general purpose terminal that provides local data entry and display capabilities for Basic Four Systems 110 through 730, and for System 810 as a 7270 replacement. The EVDT (figure 1-1) consists of a pedestal-mounted video display assembly and a separate, detachable keyboard. The EVDT uses an RS-232C asynchronous serial-bit interface for bidirectional communication with the host CPU and a serial printer. (Separate and independently programmable I/O ports are provided for CPU and printer interface connections.)

EVDT capabilities feature keyboard selection (programming) of the following parameters:

- Transmit/receive baud rate (50 to 19,200 baud)
- Data word format (7 or 8 bit word; 1 or 2 stop bits; odd, even or no parity)
- Terminal security (restricted access to keyboard Escape sequences)
- Full or half-duplex operation (in Conversation Mode)
- Display memory refresh rate (50Hz or 60Hz)
- Extension port activiation (I/O Port B recieves data from I/O Port A)
- X-ON/X-OFF input data control (automatically signals host CPU to stop and start data transmission when input data buffer is almost full and half empty)
- Cursor display and operating mode (blank - no cursor, cursor underline, blinking character at cursor, reverse video block, cursor "roll" and combination modes)
- Standard 12-hour clock (AM/PM) or 24-hour (military) clock
- Scrolling (smooth, line-at-a-time, or disabled)
- Keyboard operating features (tactile feedback with audible click, auto line feed with RETURN, keystroke auto-repeat, and end-of-line bell)
- Language (domestic and international character sets all contained in one character ROM - appropriate keycaps provided for language selected)

These keyboard-selectable parameters, all of which are displayed on a "Setup Menu," are stored in continuous (battery-backed) memory.

EVDT general capabilities include:

- 28 programmable function keys (stores user-selected commands up to 77 characters in length per function key - 300 characters maximum)
- Keyboard selection of Block Mode or Conversation Mode
- 127 ASCII characters (95 displayable characters and 32 control characters)
- 24 x 80 character display on non-glare green phosphor CRT screen
- Easy to read 6 x 9 dot-matrix characters with tenth dot for lower case decenders
- 18-key numeric keypad with cursor control keys
- Block Mode editing and transmission control (using ESCAPE, FUNCTION and standard typewriter keys)
- Selectable display attributes for characters, line or lines, and/or full page (reverse video, blinking, underlined, reduced intensity, and combinations thereof)
- Business graphics characters (44 line-graphics characters)
- Special function keys (used with FUNCTION key to control display, configure terminal options, program function keys, and to change terminal mode of operation)
- Self-test functions (tests ROMs, RAMs and LSI device registers - keyboard selectable)
- Personality modification (escape and control sequences modifying default value of control characters used in terminal operation)
- Designated protected fields (character fields are displayed at reduced intensity and cannot be overwritten)
- N-key rollover protection
- Programming/troubleshooting display modes (text from keyboard or host CPU displayed with control characters - permits simplified data insertion and monitoring)

All EVDT data entry, display, and input/output operations are performed under microprocessor control. Data is transmitted from and received by the host CPU via serial device I/O controllers (PCBAs) installed in the CPU card cage.

1.2 EVDT DESCRIPTION

The EVDT consists of two major assemblies: a video display assembly and a separate, detachable keyboard assembly. These assemblies and their related components are illustrated in figure 1-2.

1.2.1 Keyboard Assembly

The Keyboard Assembly (figure 1-2) consists of a two-piece, low-profile housing that contains a 96-position keyswitch matrix with associated logic elements. The keyswitch matrix contains 92 keyswitches that are fitted with sculptured keycaps and arranged in two groups: a typewriter-style alphanumeric group and a numeric keypad group. The 74 keys in the alphanumeric group and the 18 keys in the numeric keypad group include the function and control keys necessary to implement the full-range of EVDT capabilities. The keyboard assembly is connected to the video display assembly with a detachable telephone-style cord.

The keyboard logic elements receive serial 8-bit data (matrix codes) from the microprocessor unit (MPU) in the video display assembly. The keyboard logic uses the matrix code input to select columns and rows, which are scanned to detect keyswitch closures. When a key is pressed, the keyboard logic produces an ouput pulse that coincides with the matrix code input for that key. The output pulse is returned to the MPU for processing of displayable alphanumeric characters or non-displayable control characters.

Of the 127 ASCII characters in the standard EVDT character set, 95 are displayable characters and 32 are control characters. All 32 control characters may be generated at the keyboard, but only 10 are recognized by the EVDT as operational control characters. Non-operational control characters are displayed as reversed video characters. The 10 operational control characters are normally not displayed, but are acted upon by the EVDT when entered at the keyboard or received from the host CPU. (Details of keyboard operation are discussed in Sections II and III.)

International keyboards are available with appropriate keycaps to support the language selected. Also available is the Katakana keyboard, which produces an additional 64 JIS standard symbols for a total of 159 displayable characters.

1.2.2 Video Display Assembly

The Video Display Assembly (figure 1-2) consists of a two-piece enclosure (CRT bezel and rear housing) that contains the following components:

- Monitor Assembly
- Main Logic Board PCBA
- Power Supply PCBA

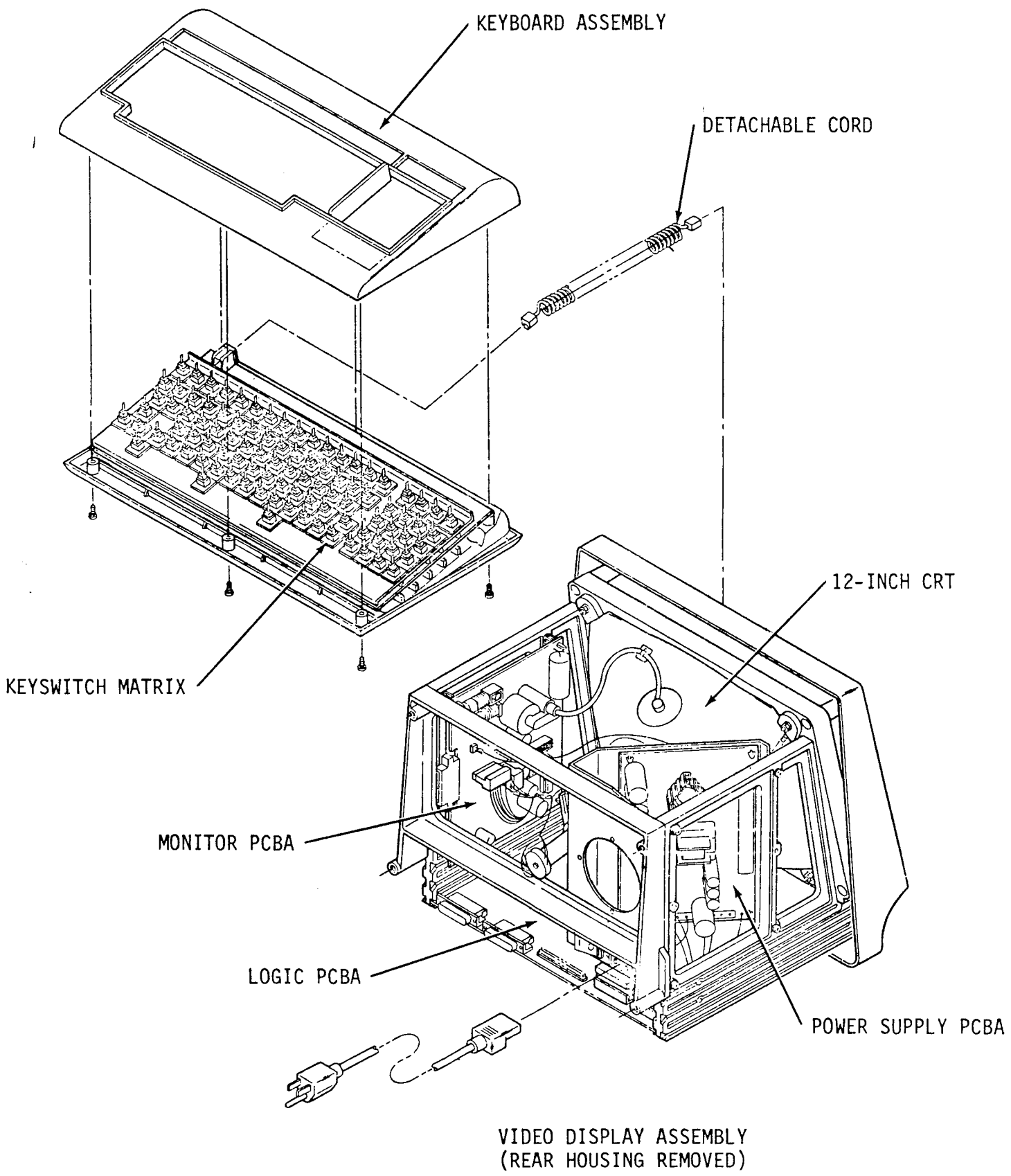


Figure 1-2. Major Assemblies and Related Components, Model 4309 EVDT

1.2.2.1 Monitor Assembly

The Monitor Assembly (figure 1-2) consists of a CRT that displays the alpha-numeric and graphics characters and a Monitor Board PCBA that provides the high voltage, video, and deflection circuits required for CRT operation.

The CRT face plate is 12 inches in diagonal measure and has a non-glare (etched) viewing surface with green phosphor P31). The CRT deflection angle is 90 degrees. The neck of the CRT includes a yoke assembly, which is adjustable, in part or whole, for proper positioning and linearity of the video raster. (Details on the CRT display matrix are provided in Section III.)

The Monitor Board PCBA accepts TTL level video, horizontal drive, and vertical drive signals from the Logic PCBA. The Monitor Board PCBA also accepts 12 volts DC from the Power Supply PCBA, via connections and traces on the Math Logic Board PCBA. These inputs are processed by the Monitor Board PCBA to generate the CRT raster scan and the high voltages that permit the display of video information. (Details of Monitor Board PCBA operation are discussed in Section III.)

1.2.2.2 Main Logic Board PCBA

The Main Logic Board PCBA (figure 1-2) contains the microprocessor unit (MPU), keyboard interface logic, main memory, display memeory, character generator and controller logic, character and display attribute logic, CRT controller logic, composite video logic, and communications interface logic.

These memory and logic elements, under control of the MPU, receive character-coded data from either the keyboard or communications interface. The coded data is written into display memory at addresses coinciding with the character (cursor) position in the display matrix. The character generators read the coded data from display memory and output a character code to the composite video logic (along with data from the character attribute and character controller logic). The CRT controller generates the horizontal and vertical sync pulses and the cursor signal. The cursor signal is used to indicate when the raster scan coincides with the cursor position (or display memory address), at which point the character is displayed on the screen.

When data is transmitted to the host CPU or serial printer, the MPU retrieves a character from display memory and sends it to the communication interface. The communication interface transmits the character bit-by-bit. Start and stop bits, as well as the parity bit (as specified) are included with each character transmitted. (Details of Main Logic Board operation are discussed in Section III.)

The Main Logic Board PCBA includes two 25-pin data interface connectors (DB-25P or equivalent D-Type) for I/O ports A and B. The connectors are accessible at the rear of the EVDT for cable connections to the host CPU and a serial printer. Also included on the Main Logic Board PCBA is a rechargeable 5-volt backup battery for the CMOS RAM (continuous memory).

1.2.2.3 Power Supply PCBA

The Power Supply PCBA (figure 1-2) produces + and -12 volts DC and regulated +5 volts DC. The ±12 and +5 volt outputs are supplied to the Main Logic Board while only the +12 volt output is supplied to the Monitor Board and only the +5 volt output is supplied to the keyboard assembly.

The mounting bracket for the Power Supply PCBA includes a male power cord receptacle and a power on-off switch, both of which are accessible at the rear of the EVDT.

1.3 SPECIFICATIONS

Specifications for the Model 4309 EVDT are listed in table 1-1.

Table 1-1. Specifications, Model 4309 EVDT

PARAMETERS	CHARACTERISTICS
PHYSICAL	
Video Display Assembly	
Height	12 inches (30.5 cm)
Width	16 inches (40.6 cm)
Depth	13.8 inches (35.1 cm)
CRT Screen Size	12 inch (30.5 cm) diagonal measure
Keyboard Assembly	
Height	1.5 inches (3.8 cm)
Width	17.8 inches (45.2 cm)
Depth	7.6 inches (19.3 cm)
Shipping Weight (Keyboard and Display Assembly)	26 pounds (11.8 kg)
AC POWER	
Voltage	100-120 VAC or 220-240 VAC (ranges jumper selectable
Current	1.0A @ 100-120 VAC 0.5A @ 220-240 VAC

Table 1-1. Specifications, Model 4309 EVDT (continued)

PARAMETERS	CHARACTERISTICS
AC POWER (cont'd)	
Frequency	50-60 Hz
Power	40 watts (maximum)
DC POWER	
Voltage	+12 VDC, -12 VDC, and +5 VDC (includes 5-volt battery backup for CMOS RAM)
Tolerance	±10% (12V) and ±5% (5V)
Current	1.2A @ +12 VDC 0.15A @ -12 VDC 2.5A @ +5 VDC
Noise and Ripple	0.20V (12V) and 0.03V (5V)
ENVIRONMENTAL	
Temperature	65°F to 75°F (18°C to 24°C)
Humidity	40% to 60% (non-condensing)
GENERAL	
Data Terminal Type	Smart (microprocessor controlled I/O with user-programmable keyboard, display, and interface parameters)
Microprocessor	Zilog Z-80A (8-bit @ 4MHz)
Main Memory	
Firmware Memory	8K x 8 ROM
Continous (Data) Memory	1K x 8 CMOS RAM (battery backed)
Display Memory	
Screen Memory	2K x 8 RAM (total)
Attribute Memory	2K x 4 RAM (total)
Character Generator Memory	4K x 8 ROM (total
Display Format	24 lines x 80 characters with selectable 25th status line

Table 1-1. Specifications, Model 4309 EVDT (continued)

PARAMETERS	CHARACTERISTICS
GENERAL (cont'd)	
Character Font	8 x 12 character cell with 6 x 10 dot matrix (including lower-case decender)
Character Font Attribute	Normal, double wide, double high, double wide/double high
Display Attributes	Reverse video, reduced intensity, blinking, underlined (assignable to cursor, character, line, or full screen)
Communication Interface	Asynchronous serial-bit per EIA Standard RS-232C
Transmission Format	10- or 11-bit transmission word consisting of 1 start bit, 7 data bits for domestic and World Trade terminals or 8 data bits for international and Katakana terminals, followed optionally by 1 parity bit and 1 or 2 stop bits.
Baud Rates	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200,9600 and 19200 baud
Transmission Modes	
Conversation Mode - Full Duplex	Keyboard codes are sent to host CPU and returned for display or execution of control function
Conversation Mode - Half Duplex	Keyboard codes are displayed or acted upon and are sent to host CPU. Data received from host CPU is displayed or acted upon.
Block Mode	Keyboard codes are displayed or acted upon but not sent to host CPU. Data received from host CPU is displayed or acted upon. Permits editing of data. Requires use of Special Function Keys for Block Mode data transmission.

Table 1-1. Specifications, Model 4309 EVDT (continued)

PARAMETERS	CHARACTERISTICS
GENERAL (cont'd)	
CRT Monitor	
Display Size	8.5 inches x 6 inches (21.6 cm x 15 cm)
Deflection Angle	90 degrees
Refresh Rate	50 or 60 Hz (non-interlaced)
Phosphor	P31 Green
High Voltage	13KV
Horizontal Frequency	19.25 KHz @ 50/60 Hz
Horizontal Period	51.7 microseconds
Horizontal Retrace Time	6.5 microseconds (max.)
Horizontal Drive Pulse Width	4.23 microseconds
Horizontal Video Blanking Time	12 microseconds
Horizontal Lead/Lag	$\pm$2.0 microseconds
Vertical Frequency	50/60 Hz
Vertical Period	20 milliseconds (50 Hz)/ 16.67 milliseconds (60 Hz)
Vertical Retrace Time	800 microseconds (max.)
Vertical Drive Pulse Width	0.1 - 1.2 milliseconds
Vertical Video Blanking Time	4.5 milliseconds (50 Hz)/ 1.2 milliseconds (60 Hz)
Vertical Lead/Lag	None

Table 1-1. Specifications, Model 4309 EVDT (continued)

PARAMETERS	CHARACTERISTICS
GENERAL (cont'd)	
Keyboard	
Physical Layout	74-key, typewriter-style alphanumeric keyboard with 18-key numeric keypad. Alphanumeric keyboard includes control and special function keys. Numeric keypad includes cursor control keys and additional function keys.
Character Sets	Keyboard selection of domestic (standard) or one of seven international character sets (French, Italian, Swedish, Spanish, Norwegian, German, or Danish - all contained in standard character ROM)
Programmable Function Keys (F1 through F14; F15 through F28 with SHIFT)	Execute user-selected character-string commands stored in continuous memory. Each function key has 77-character buffer. Total of 300 characters may be programmed.
Special Function Keys	Pressed with FUNCTION key to invoke special functions. These include terminal setup, block mode, conversation mode, display brightness, clear display, storing/examining data in Programmable Function keys, print, freeze display
Control keys	Control cursor movement and select character entered for dual-character keys. CONTROL key with standard keys generate ASCII control characters, which are acted upon or displayed; ESCAPE key with standard keys emulate host control of EVDT operation
Editing and Control Modes	
Cursor Control	Up, down, forward, backward, tab, back-tab, home (using keypad III key), protect mode tab, and load/read cursor position/content
Block Mode Transmission Control	Send or print line/page of unprotected or protected characters; partial send (using Function keys or Escape sequences)

SECTION II

INSTALLATION AND OPERATION

2.1 INTRODUCTION

This section provides information on the installation and operation of the Model 4309 EVDT. The use of the Special Function, Escape, and Control keys is described in detail as reference for field service and programming personnel.

2.2 UNPACKING/INSPECTION/REPACKING

The EVDT is shipped in one carton, which contains the video display assembly, keyboard, keyboard cable, power cord, and Operator's Guide. The shipping carton is constructed of heavy cardboard and includes specially constructed foam mounting to protect the EVDT from damage. The following procedure is recommended when unpacking the EVDT.

1. Before accepting the EVDT from the carrier, inspect the shipping carton for signs of external damage. Any indication of external damage must be noted by the carrier and reported immediately to your Basic Four sales office.

NOTE

When unpacking the EVDT, save all packing materials and the shipping carton for use at a later date.

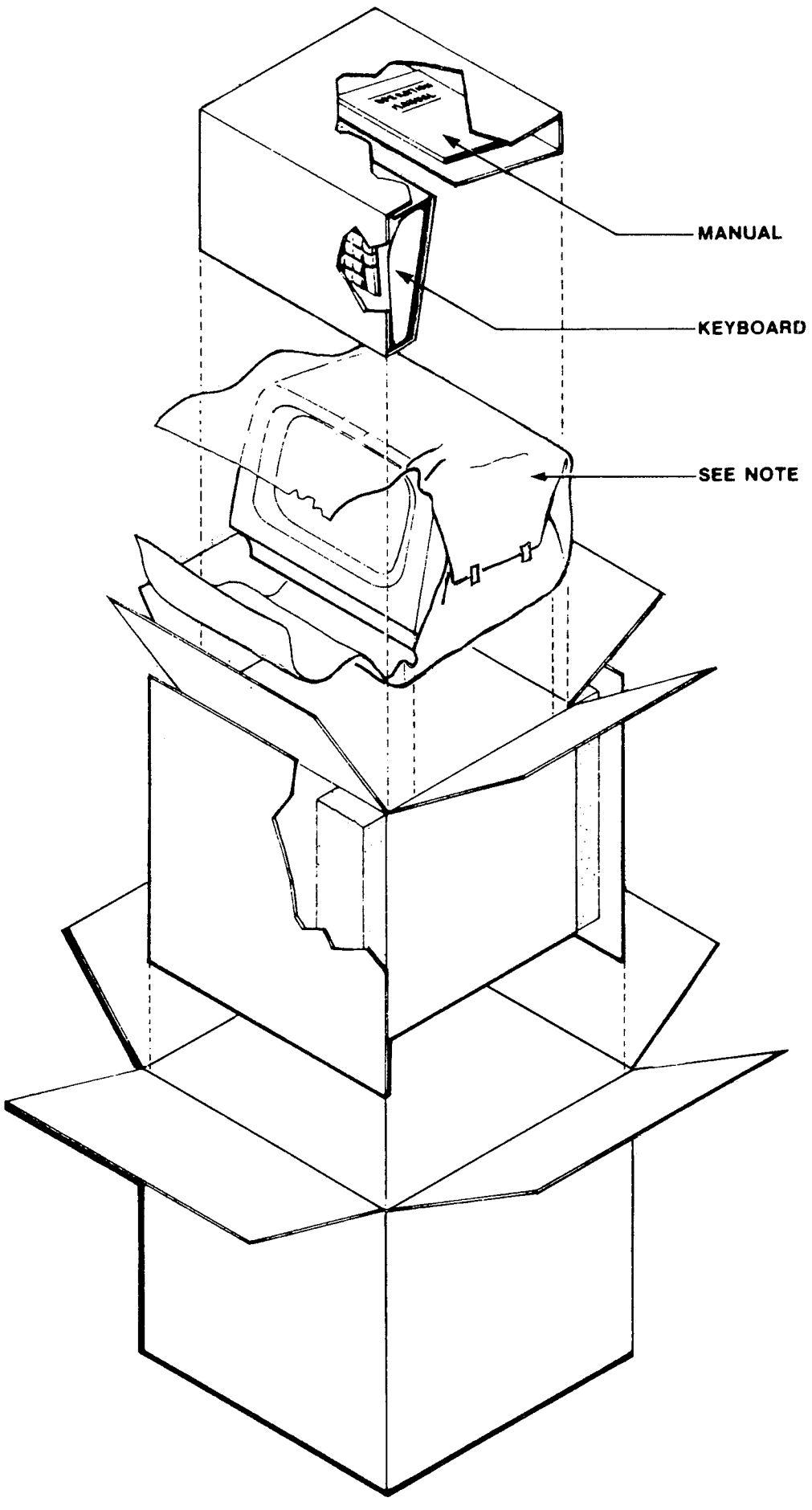
2. With the shipping carton in its upright position, open the carton and carefully remove the EVDT components, as shown in figure 2-1.

3. Carefully unwrap and inspect all items for indications of shipping damage. Check for loose, bent, broken, or otherwise damaged parts. Immediately report any damage to your Basic Four sales office.

4. When returning an EVDT to the factory, repack the unit in its original container, using the original packing materials whenever possible. Repack the EVDT as shown in figure 2-1.

2.3 PREINSTALLATION CHECKS

Before connecting the EVDT to site power, the following checks should be made to assure proper operation and to prevent electrical damage to the equipment.



NOTE:

SAVE ALL PACKAGING MATERIALS FOR FUTURE USE.

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Figure 2-1. EVDT Unpacking/Repacking

Table 1-1. Specifications, Model 4309 EVDT (continued)

PARAMETERS	CHARACTERISTICS
GENERAL (cont'd)	
Editing and Control Modes (cont'd)	
Conversation Mode Transmission Control	Half-duplex (data displayed as entered) or full-duplex (data returned for display from host CPU)
Block Mode Editing	Clear display, erase line, erase page, delete line, insert line, delete character, insert character, set tab, and clear tab(s)
Enter Mode	Display all control characters along with text as aid in programming and troubleshooting
Insert Mode	Permits insertion of characters without overwriting existing characters
Freeze Mode	Stops display from changing while allowing input to data buffer
Protected Field Mode	Uses Write Protect and Protect Modes to prevent characters, lines, or entire display from being overwritten
Scroll Mode	Smooth or line-by-line scrolling
Setup Mode	Display menu of keyboard selectable parameters for word length, stop bits, parity, baud rate, duplex, data buffer (X-ON/X-OFF) protocol, refresh rate, extension port, status line, keyboard security, scroll mode, cursor mode, auto-repeat, linefeed with carriage return, tactile feedback, end-of-line bell, language, and clock select. All selected parameters stored in continuous memory (CMOS RAM)
Self-Test Mode	Invoked at keyboard only; CONTROL key with standard keys cause individual tests to be executed for ROM checksum, MPU scratchpad RAM, screen RAM, LSI registers, and audible tone. ROM and RAM tests are also executed at power up

1.4 RELATED DOCUMENTS

The following manuals are recommended as supplementary reference material for field service personnel.

- Ergonomic Video Display Terminal Operator's Guide, BFISD 5161
- System 810 Service Manual, BFISD 8058P
- System 810 Operator's Guide, BFISD 5115
- Model 1350 Fixed Media Disk CPU Service Manual, BFISD 8065PA (supporting Systems 110, 210 and 310 with High Speed CPU)
- System 110 Operator's Guide, BFISD 5160
- System 200/410 Service Manual, BFISD 8035A
- System 200/410 Operator's Guide, BFISD 5045
- System 210 Operator's Guide, BFISD 5109
- System 310 Operator's Guide, BFISD 5135

2.3.1 AC Power Requirements

Verify the following AC line requirements:

1. The AC line is not shared by devices that cause large transients (e.g., air conditioners, heaters, welding equipment, or equipment with large motors).

2. The AC line is not subject to voltage variations greater than 10%, or frequency variations greater than 0.2%.

3. The AC power outlets are within the proper voltage range (100-120 VAC, 50/60 Hz or 200-240 VAC, 50/60 Hz, as applicable) and near enough to the equipment so that power extension cables are not necessary. (Refer to paragraph 2.3.3.)

2.3.2 Ground Checks

1. Verify that power is not applied and the AC line cord is not connected before making the following checks.

CAUTION

Only three-wire electrical outlets and three-pronged plugs with the third wire connected to earth ground are acceptable electrical connectors. NO two-wire outlets or plugs, with or without connection to a conduit ground, are to be used. Unstable equipment operation may result.

2. Check that the AC line includes a third-wire earth ground that meets or exceeds the requirements of the National Electrical Code. This can be checked as follows:

   a. Locate the circuit breaker that is to supply power to the EVDT. With a digital voltmeter set to measure 20 volts AC, and the circuit breaker turned ON, measure the drop between the green and white wires at the power source (wall outlet). The measured voltage must be less than 1.8 volts AC.

   b. Set the source circuit breaker to OFF. Measure the resistance between the green and white wires at the wall outlet. The resistance must be less than the value shown below for the circuit breaker rating.

Circuit Breaker Rating	Resistance
15 Amperes	0.30 Ohms
20 Amperes	0.25 Ohms
30 Amperes	0.15 Ohms

   c. If the measurement in either step (a or b) is not less than or equal to the value given, request the customer to provide a power source that meets the given requirements.

2.3.3 Power Supply PCBA Input Voltage Range

The EVDT Power Supply PCBA is configured by means of a jumper at its AC input to operate within one of two voltage ranges. These voltage ranges are 100-120 VAC, 50/60 Hz and 220-240 VAC, 50/60 Hz. Verify that the AC input voltage range selected for the Power Supply PCBA is compatible with (includes) the AC voltage supplied by the site power source. Figure 2-2 illustrates the configuration of the AC-input jumper for each of the two PCBA voltage ranges.

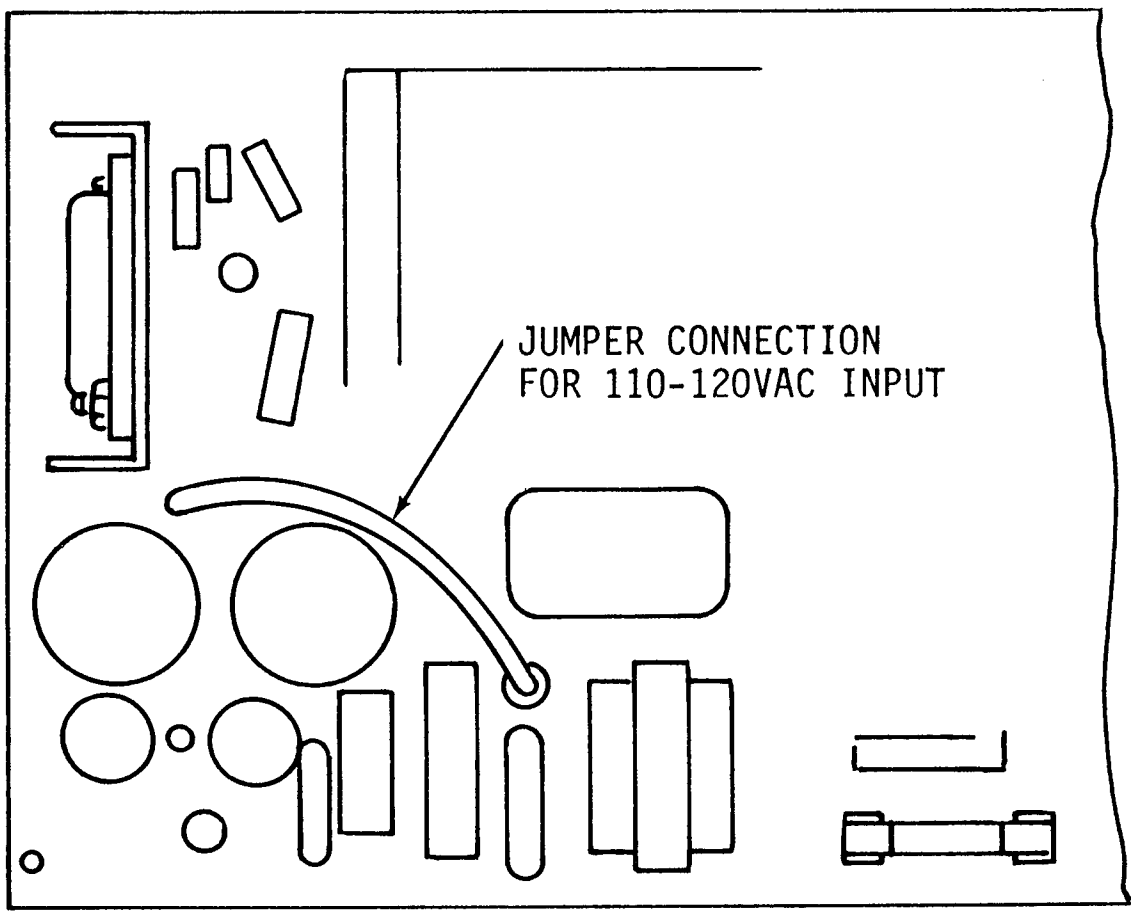
2.4 SYSTEMS INTERFACE REQUIREMENTS

The EVDT systems and serial printer interface cables, along with their point-to-point connections are listed in table 2-1. Interface cable connections are illustrated in the EVDT Installation procedure of paragraph 2.5, which follows.

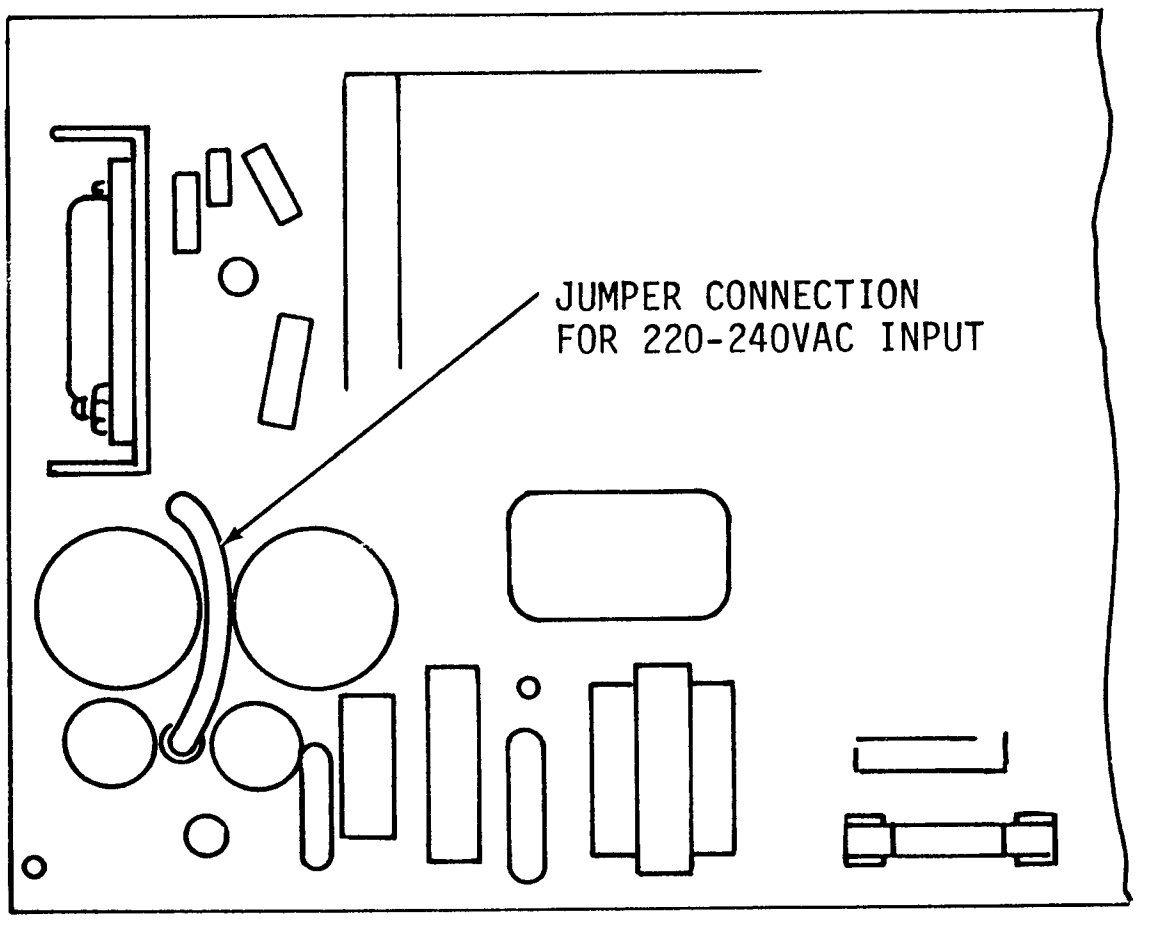
Table 2-1. Systems Interface Cables and Connections

SYSTEM	FROM	CABLE DESCRIPTION, PART NO.	TO
810	EVDT Port A	12-Conductor Cable 8-Way/ RS-232, 50 Ft. Max. 907115-XXX (50/60 Hz)	N8-Way Controller PCBA - J1 thru J7
Fixed Disk CPU (System 200,210, 310, or 410)	EVDT Port A	4-Conductor Cable, Signal, 1000 Ft. Max. -906693-VAR (50 Hz) (See Note) -906041-VAR (60 Hz)	8-Channel Terminal Controller PCBA - J0 thru J7
Removable Disk CPU (System 510, 610,710 or 730)	EVDT Port A	4-Conductor Cable, Terminal Interface, 1,000 Ft. Max. -906694-VAR (See Note) (50 Hz) -906274-VAR (60 Hz)	I/O Panel Connector - Channel 0 thru Channel 7
All Systems	EVDT Port B	4-Conductor Cable, Terminal Interface, 1,000 Ft. Max. -906694-VAR (See Note) (50 Hz) -906274-VAR (60 Hz)	Serial Printer I/O Port Connector

NOTE: Baud rate constraints apply at longer cable lengths. (Refer to Setup Mode instructions, paragraph 2.7.)



A. 110 - 120VAC CONNECTION



B. 220 - 240VAC CONNECTION

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Figure 2-2. AC Input Voltage Configurations, Power Supply PCBA

2.5 EVDT INSTALLATION

Install the EVDT as follows:

1. Place the pedestal for the video display assembly on the surface of the designated EVDT work station.

NOTE

The area chosen for EVDT operation should not contain equipment that radiates RFI (radio-frequency interference) or strong magnetic fields, as these conditions may interfere with EVDT performance.

2. Set the video display assembly atop the pedestal.

3. Place the keyboard in front of the display assembly and plug the coiled keyboard cable into the receptacle located below the right side of the display screen (see figure 2-3).

CAUTION

Be sure to perform the preinstallation checks in paragraph 2.3 before connecting the EVDT to an AC outlet.

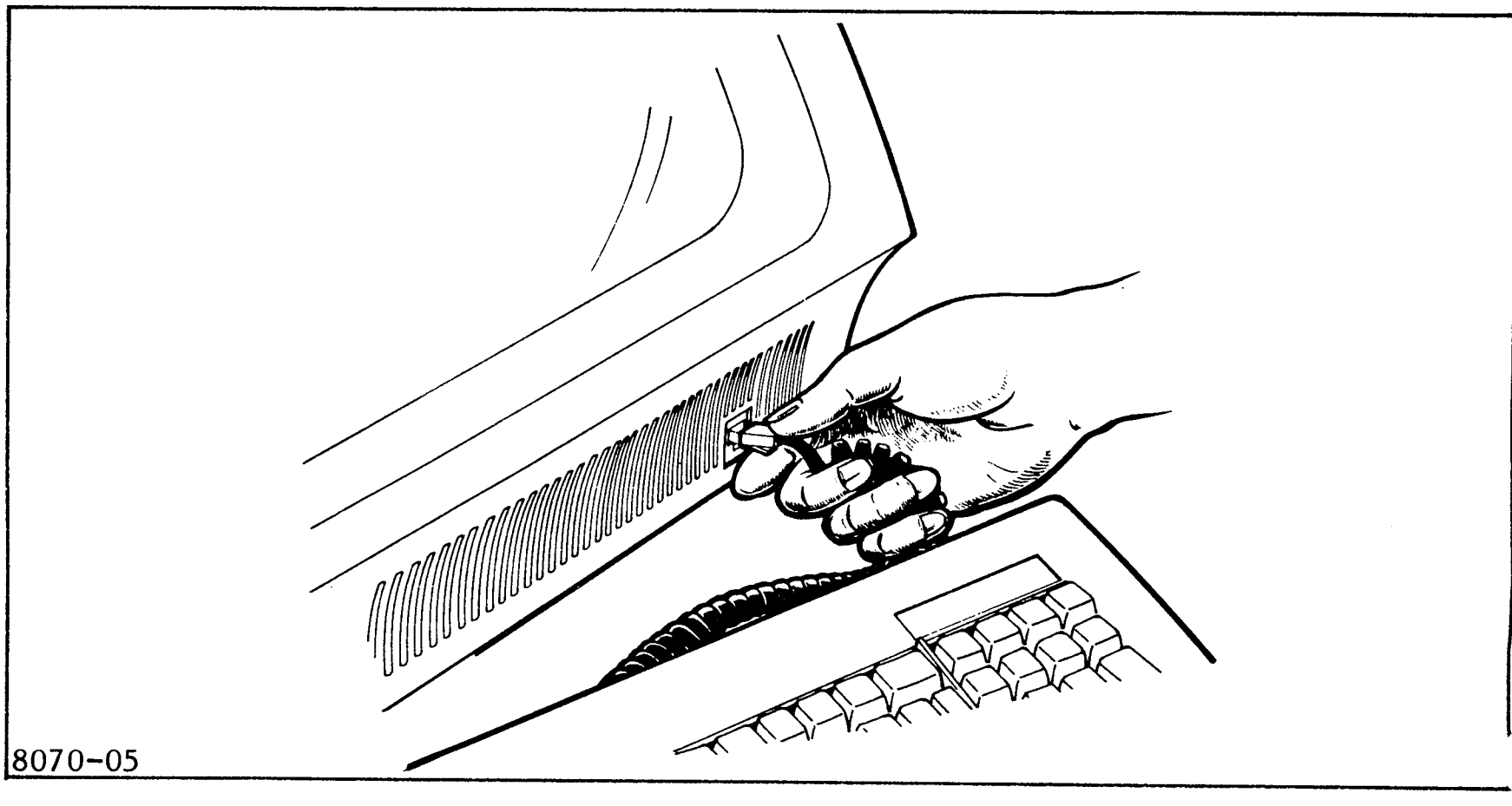

Figure 2-3. Keyboard Cable Connection, Model 4309 EVDT

4. Verify that the POWER ON/OFF switch on the display assembly rear panel is in the OFF position (see figure 3-4). Connect the EVDT power cord from the receptacle on the display assembly rear panel to the designated AC outlet.

5. Connect the appropriate interface cable (table 2-1) from PORT-A (figure 2-4) to the serial I/O controller (PCBA) or I/O connector at the host CPU (see figures 2-5, 2-6, or 2-7 and 2-8).

6. From PORT-B (figure 2-4) connect the interface cable (table 2-1) to the serial printer I/O connector (figures 2-5, 2-6, or 2-7 and 2-8).

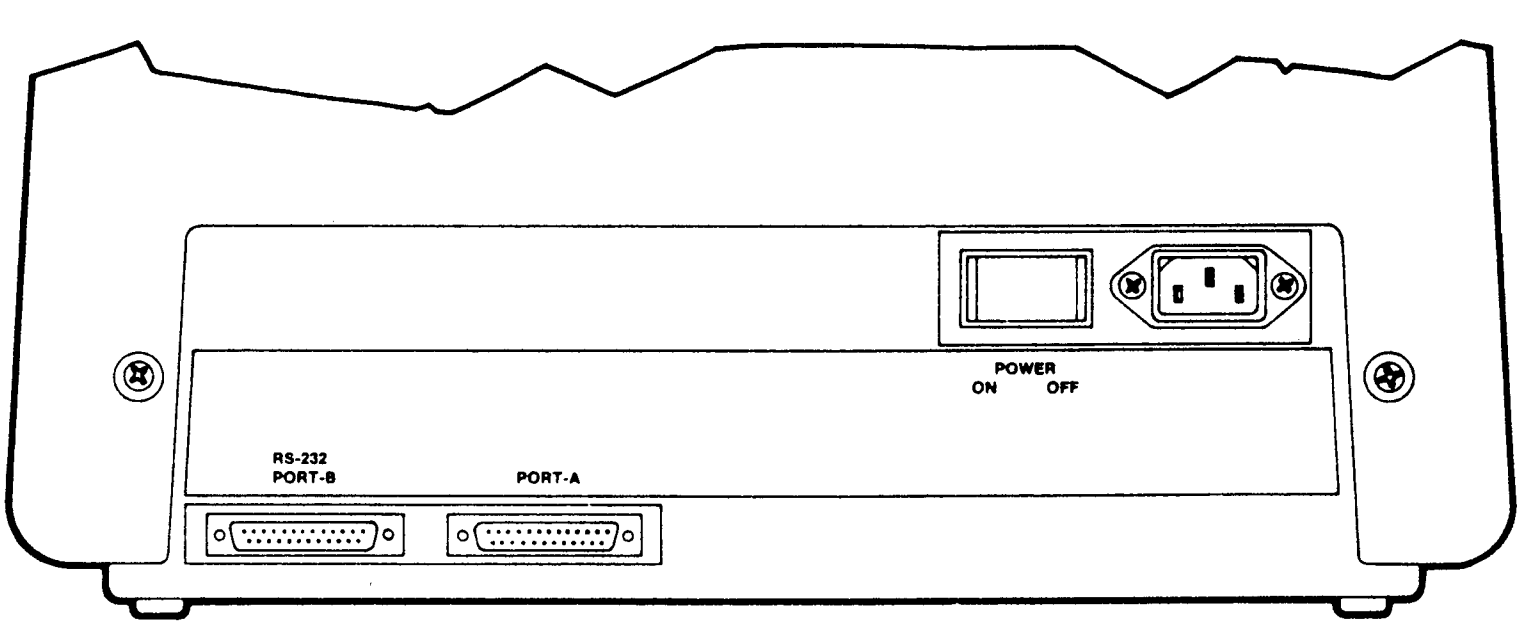

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Figure 2-4. Video Display Assembly Rear Panel, Model 4309 EVDT

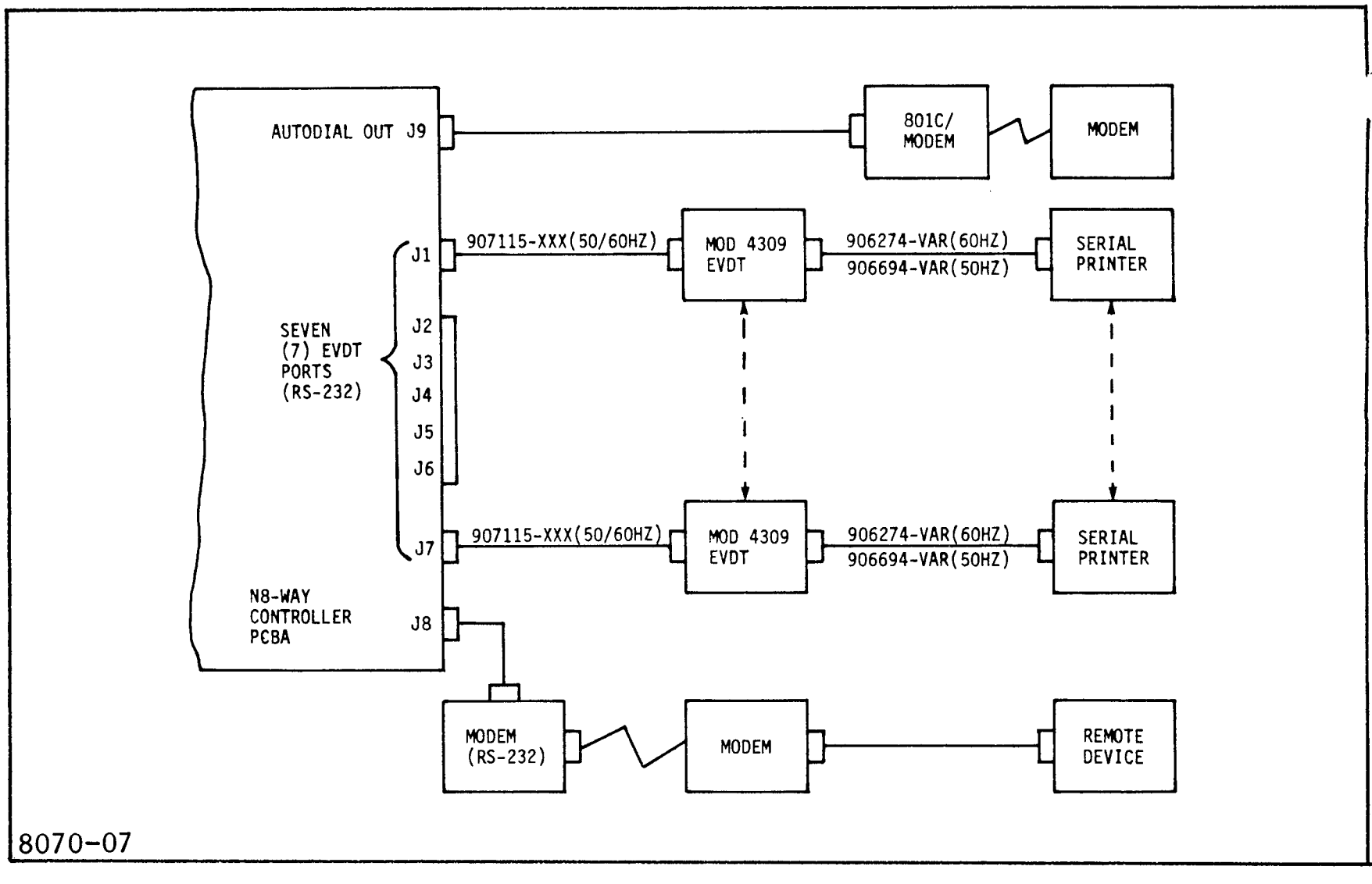


Figure 2-5. EVDT to System 810 Interface Cable Connections

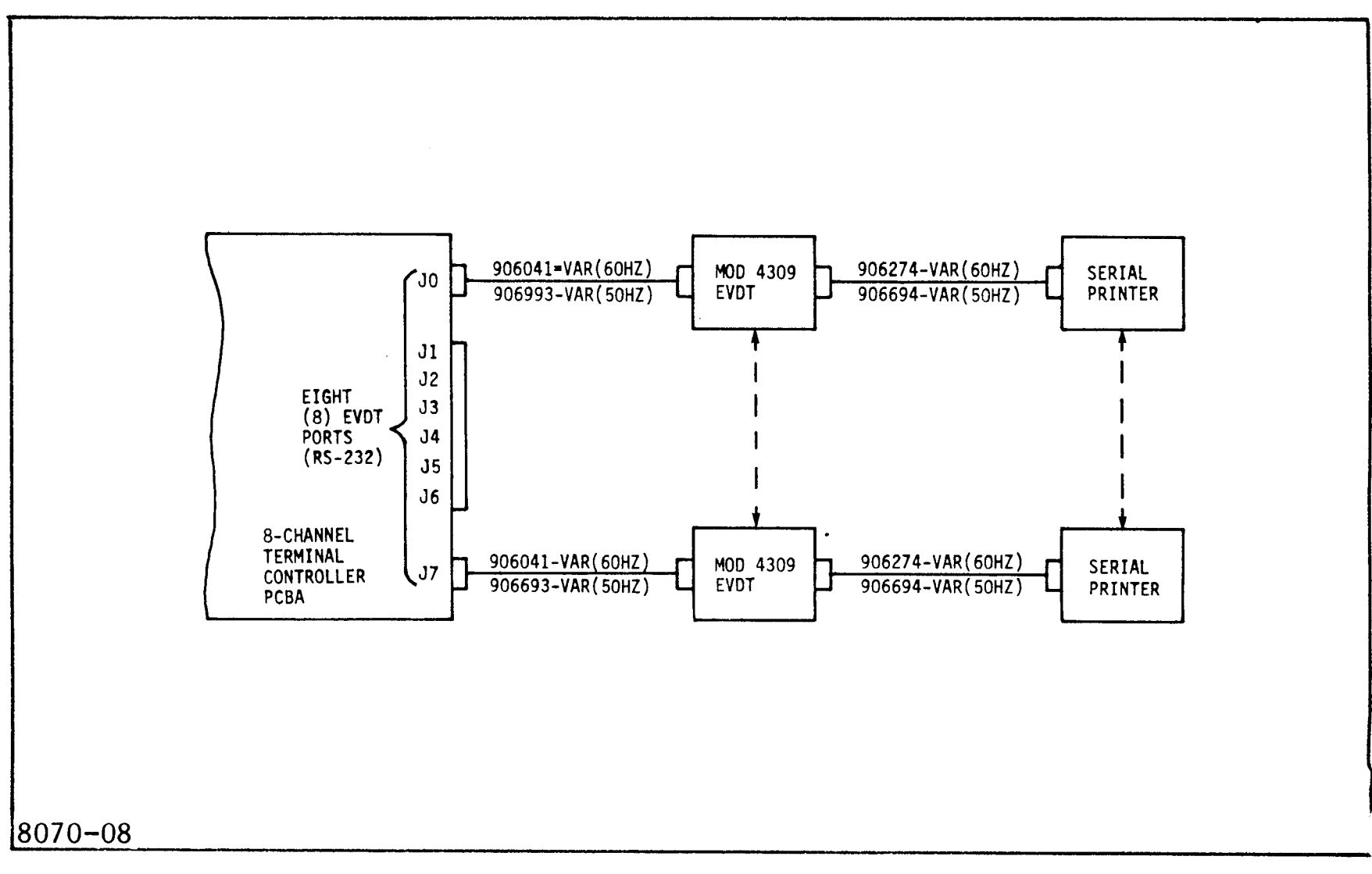


Figure 2-6. EVDT to Fixed Media Disk CPU Interface Cable Connections

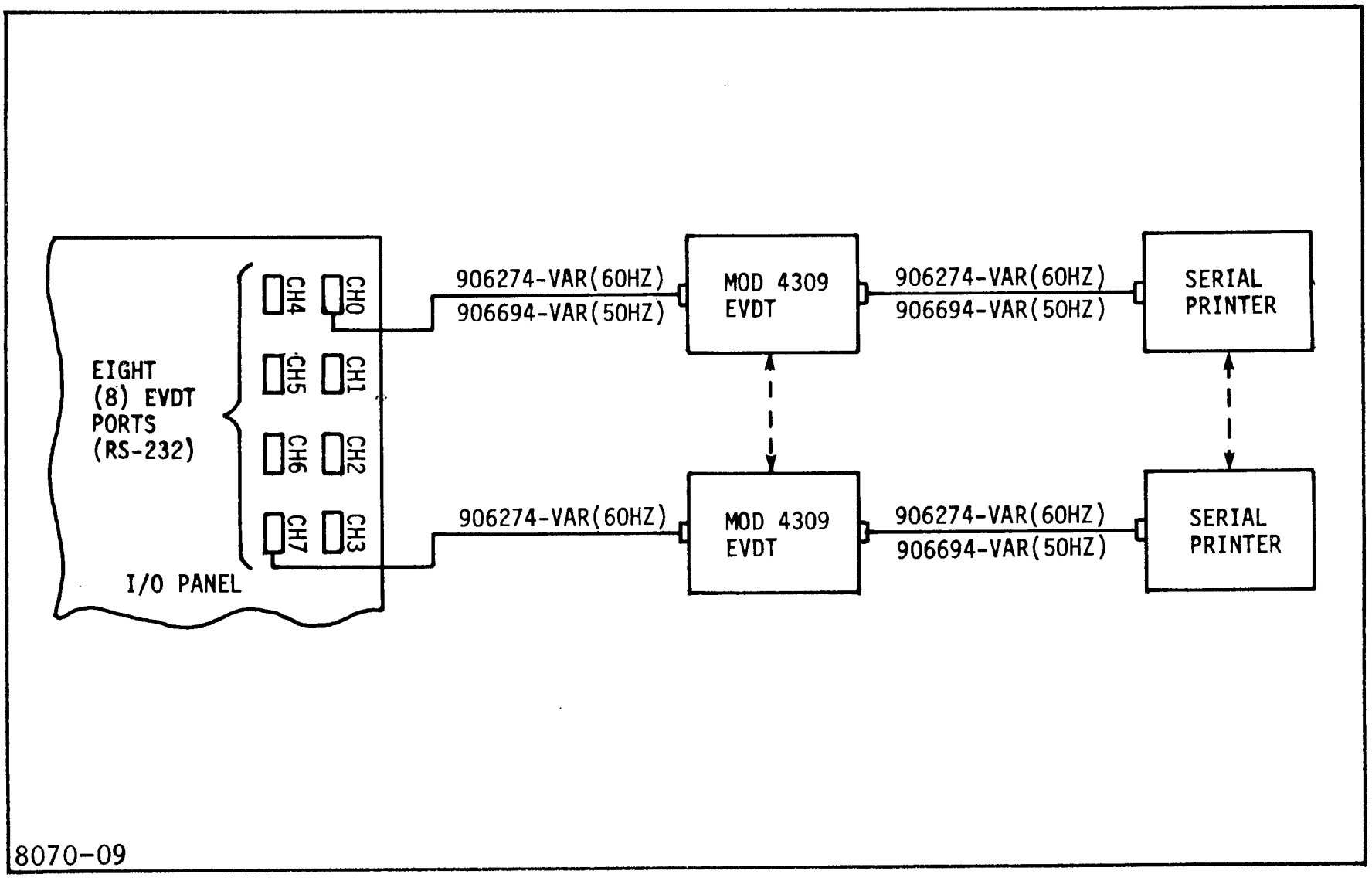


Figure 2-7. EVDT to Removable Disk CPU Interface Cable Connections

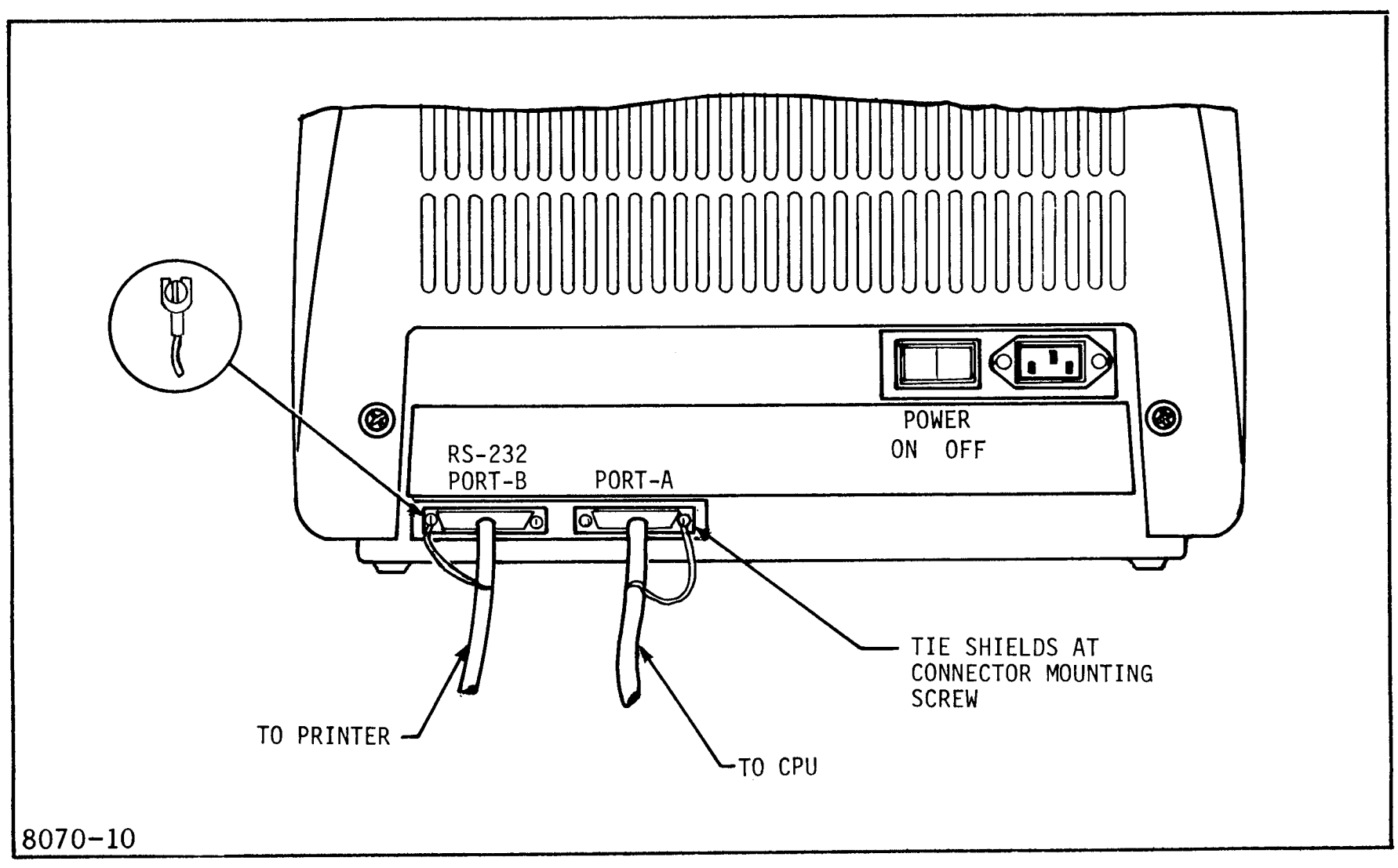


Figure 2-8. EVDT Cable Grounding

2.6 EVDT POWER-UP

Perform the initial EVDT power-up as follows:

1. Press the rear-panel POWER ON/OFF switch to the ON position. The EVDT will automatically perform a power-up self-test. At the completion of the test an audible tone ("beep) will sound, indicating that the self-test ran successfully. After approximately 20 seconds, the cursor and the EVDT status line should appear on the display.

2. Perform the Keyboard Master Reset by pressing the CONTROL, SHIFT, FUNCTION, and CLEAR keys at the same time. Data will be ersed from the screen and the status line clock will be reset to 1:01 AM. (This keyboard operation resets all programmable EVDT parameters to their default settings, assuring that only those parameters modified in the Setup Mode, or their default settings, will affect EVDT operation.)

3. Refer to paragraph 2.7 and select the parameters required for data transmission and the desired keystroke and/or display features.

2.7 SETUP MODE PARAMETER SELECTION

There are a number of keyboard-selectable parameters that may be used to configure the EVDT for particular operations and individual preferences. These parameters fall within two categories: parameters that affect the interface with the host CPU, and parameters that affect keystroke or display operations.

Interface parameters control communications to and from the host CPU. These parameters must be set correctly, or else incorrect data may be sent to or received from the host CPU. Interface parameters are selected and set according to requirements of system software/hardware, and normally will not change (unless unique changes are made to the system).

Keystroke and display parameters allow the EVDT to be configured for individual preferences. These parameters affect only the local operation of the EVDT, and have no effect on the host CPU.

Interface parameters and keyboard or display parameters are selected at the keyboard and stored in continuous memory while the EVDT is in the Setup Mode. When invoked, this mode will place the EVDT in a local condition and display the SETUP menu, either as a single line (line at a time) menu or, if desired, as a full screen menu. (See figure 2-9.) Invoking the full screen SETUP menu will overwrite any data displayed on the screen; invoking the single line SETUP menu, however, permits parameter changes while retaining all screen data. (The single line SETUP menu temporarily displaces the first line of screen data, which returns when the Setup Mode is terminated. The cursor will also return to the same screen position that it occupied before the single line SETUP menu was invoked.)

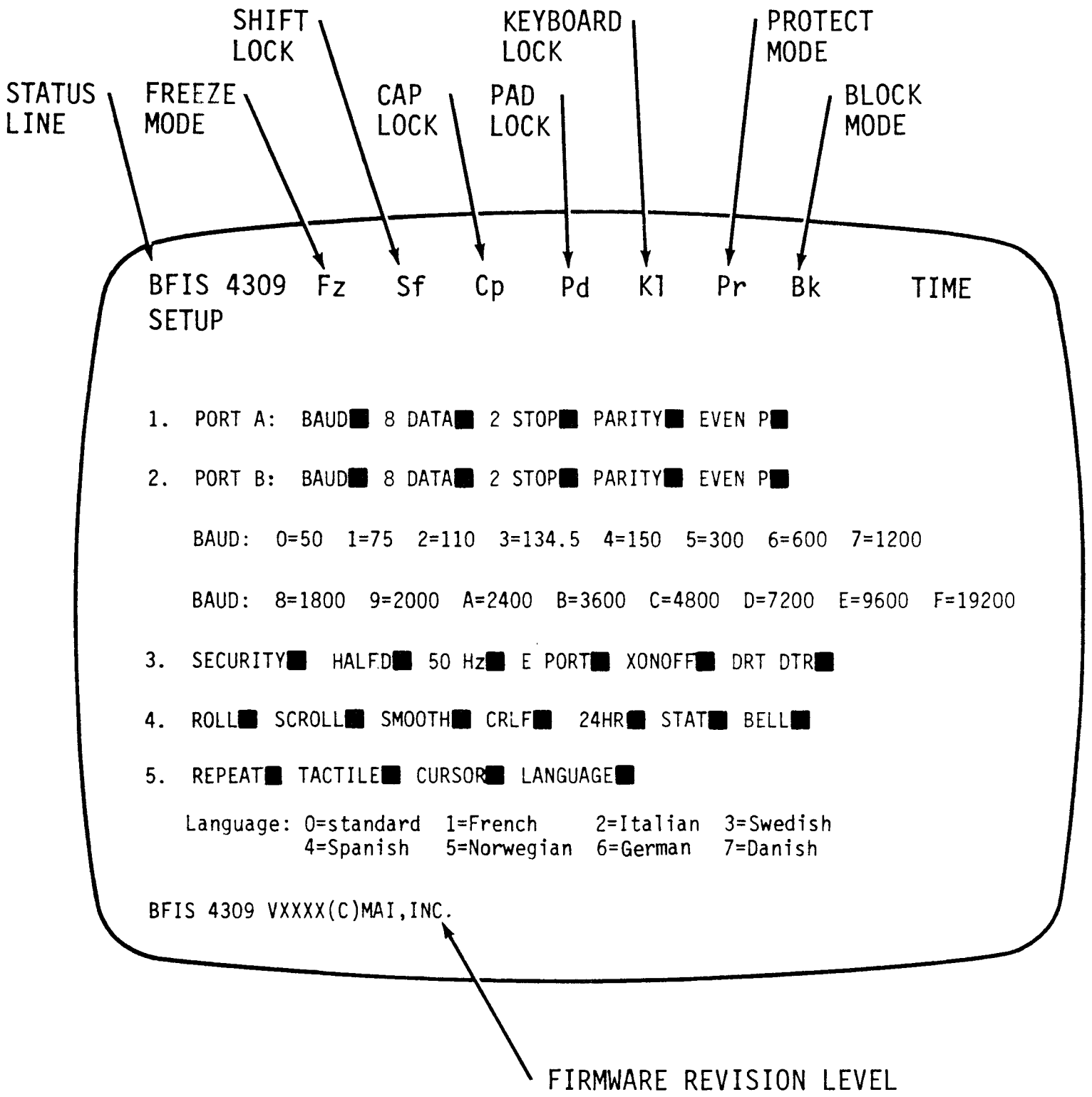


Figure 2-9. Full Screen Setup Menu and Status Line

To invoke the Setup Mode, press and hold the FUNCTION key, and press the numeric keypad zero (0) key. This operation will display the prompt: "SETUP Menu--Select:." To view the single line SETUP menu, a line at a time, press the numeric key (1 thru 5) corresponding with the line of the menu to be displayed. The selected line will then appear. To view the full screen SETUP menu, press the zero key again (either on the main keyboard or the numeric keypad).

NOTE

If Pad Lock or Shift Lock is enabled ("Pd" or "Sf" is displayed on Status Line), the numeric keys on the numeric keypad will not operate. Hold FUNCTION key down and press PAD key to disengage Pad Lock; hold SHIFT key down and press CAPS LOCK key to disengage Shift Lock.

Selecting parameters in the Setup Mode is basically the same when using either the single line or full screen SETUP menu. To select and change a parameter, simply position the block cursor at the box to be changed, and enter the appropriate character from the keyboard. The "0" or "1", 0 thru F for Baud Rate, and 0 thru 7 for Cursor and Language are the only valid characters; all others will result in a bell tone, indicating an attempted illegal character entry. Illegal characters will not be accepted. Select the desired code characters from table 2-2.

The SETUP menu cursor position is changed with the space bar or RETURN key. Press the space bar to move the cursor from left to right one box position at a time on the same line. The cursor will return to the first box on the same line if advanced from the last position. Press the RETURN key to advance the cursor to the first box of the next line.

The single line SETUP menu is manipulated by using the RETURN key to change lines in the menu; for example, to change from line 3 to line 4, in ascending numerical order. Use the space bar to move to cursor position within a single line.

To terminate the single line SETUP menu, press ESCAPE twice; to terminate the full screen SETUP menu, press ESCAPE once.

The procedure for invoking the Setup Mode and for selecting and/or changing EVDT parameters is summarized in table 2-3. Procedures for programming the status-line clock, establishing protected fields, function key programming, and selecting display attributes are provided in paragraph 2.10.

NOTE

The maximum recommended baud rates vs. cable length are: 0 to 250 feet - 9600 baud; 251 to 500 feet - 4800 baud; and 501 to 1000 feet - 2400 baud.

Table 2-2. Setup Menu Parameters and Selection Codes

PARAMETERS	SELECTION CODE/DESCRIPTION
Baud	0-F = Port A baud rate selected from SETUP menu (E*) 0-F = Port B baud rate selected from SETUP menu (A*)
8 Data	0 = Seven-bit word length for I/O port* 1 = Eight-bit word length for I/O port
2 Stop	0 = One stop-bit on data word for I/O port* 1 = Two stop-bit on data word for I/O port
Parity	0 = No parity on data word for I/O port 1 = Parity bit on data word for I/O port*
Even P	0 = If parity is invoked, it will be odd parity* 1 = If parity is invoked, it will be even parity
Security	0 = Escape sequences uninhibited 1 = Selected Escape sequences inhibited*
Half D	0 = Full Duplex* 1 = Half Duplex
50 Hz	0 = 60 Hz for U.S. operation* 1 = 50 Hz for foreign operation
E Port	0 = Extension Port is not activated* 1 = Extension Port is activated and will pass data from Port A at the selected baud rate to a device connected to Port B, such as a serial printer
Xonoff	0 = Xonoff is not activated* 1 = Xonoff is activated and a CONTROL S signals the computer to halt transmission when the terminal buffer is 32 characters short of being full. A CONTROL Q signals the host computer to resume transmission when the character buffer is at least half empty
Dtr	0 = Data Terminal Ready feature is not activated* 1 = Data Terminal Ready feature is activated and will respond by dropping the "Data Terminal Ready" signal, indicating to the host computer that the terminal input buffer is 32 characters from being full. This feature complements the Xonoff by providing an alternative to sending CONTROL S and receiving CONTROL Q for input buffer control. If both Xonoff and Dtr features are selected a CONTROL S code will automatically be sent prior to dropping the "Data Terminal Ready" signal

*Indicates default setting of setup parameters; invokable by Keyboard Master Reset.

Table 2-2. Setup Menu Parameters and Selection Codes (continued)

PARAMETERS	SELECTION CODE/DESCRIPTION
Roll	0 = Cursor will not wrap around to the next line 1 = Cursor advances to first column of the next line when cursor is advanced from the last column on the right*
Scroll	0 = All lines do not move up when the bottom line is filled to the 80th position. Additonal data will continue to be written on the bottom line 1 = All lines move up when the bottom line is filled to the 80th position*
Smooth	0 = Regular Line Scrolling, a single line at a time* 1 = Smooth Scrolling is enabled; at speeds of over 1200 baud the Xonoff will prevent buffer overflow (not yet fully supported by Basic Four software)
Crlf	0 = No line feed when RETURN is pressed* 1 = Line feed when RETURN is pressed
24 hr	0 = Standard 12-hour clock (AM/PM)* 1 = 24-hour clock (military time)
Stat	0 = Status line is not displayed 1 = Status line is displayed*
Repeat	0 = Keystrokes are not automatically repeated* 1 = Keystrokes are automatically repeated when the key is held down for more than one second. Characters or operations are repeated at a rate of 16 per second
Tactile	0 = No audible click is produced when a code-generating key is pressed* 1 = An audible click is produced when a code-generating key is pressed
Bell	0 = No bell before line end* 1 = Bell sounds eight characters before end of line for block mode convenience

*Indicates default setting of setup parameters; invokable by Keyboard Master Reset.

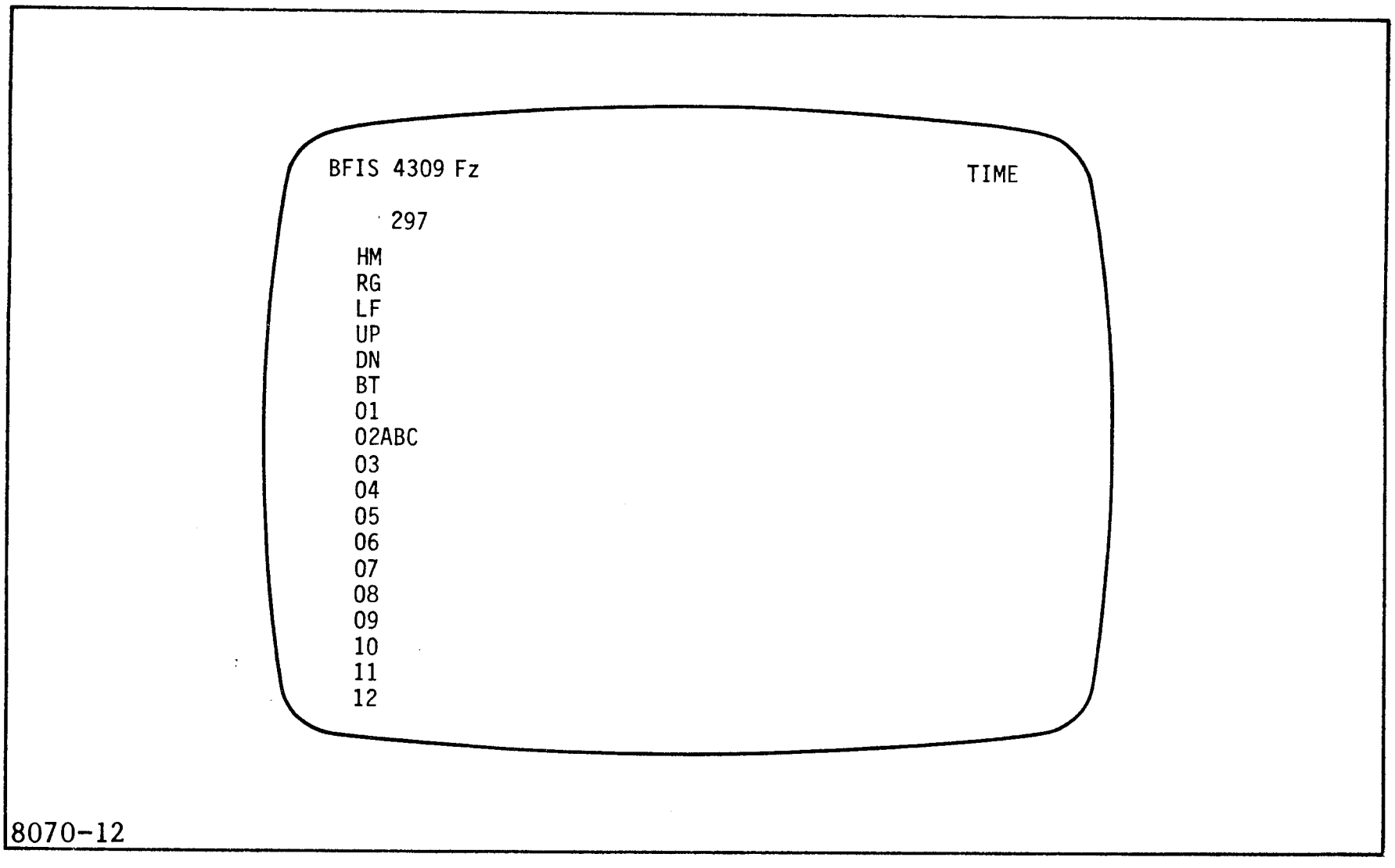


Figure 2-10. [FUNC] with [EXAM F] Display

21. Type [ESCAPE/CLEAR] ; press and hold [SHIFT] and type [V] . Press and hold [CTRL] and type [G] ; observe that B_L is displayed on the screen and that no audible tone is sounded. Press and hold [CTRL] while typing [H] [I] [J] ; observe that B_S, H_T, and L_F are displayed on the screen.

2.9 EVDT OPERATION

The following paragraphs provide detailed information on the various operating modes and control codes used by the Model 4309 EVDT. Programming information is provided in paragraph 2.10.

2.9.1 Keyboard Overview

Figure 2-11 shows the layout and describes the functions of the domestic EVDT keyboard. Figures 2-12 thru 2-18 illustrate the various international keyboard layouts according to nationality. It should be noted that although the international keyboards differ in their keycap designations, the keyswitch layout for all keyboards is identical. Furthermore, those displayable characters peculiar to each of the international keyboards are derived from translation of the standard ASCII code, as performed by a programmable, universal character generator. (Programming of the character generator is performed while the EVDT is in the Setup Mode, paragraph 2.7.) Finally, those keyswitch functions captioned in figure 2-11, and all of the keyboard operations described in the following paragraphs, apply equally to both domestic and international keyboards.

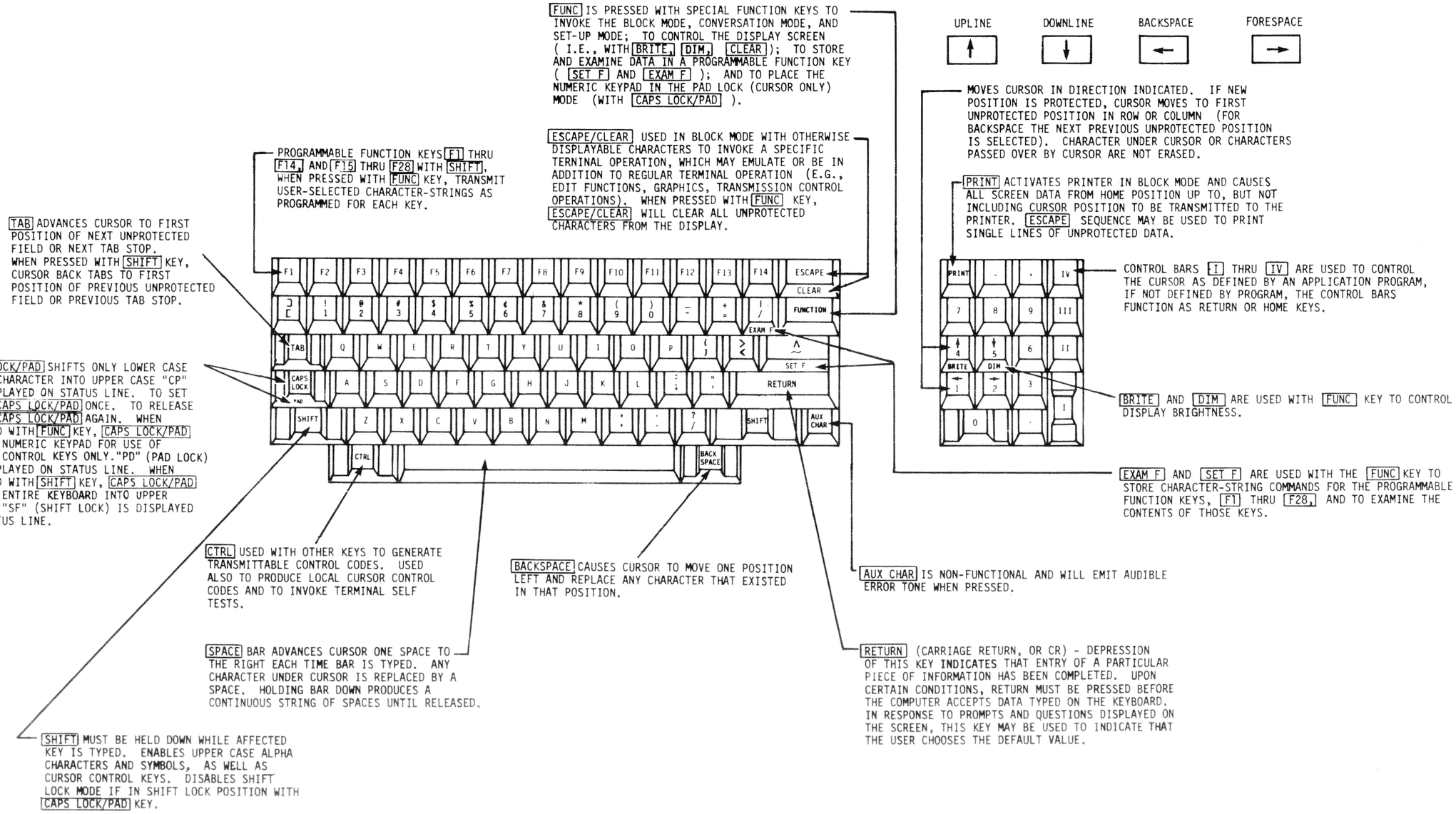
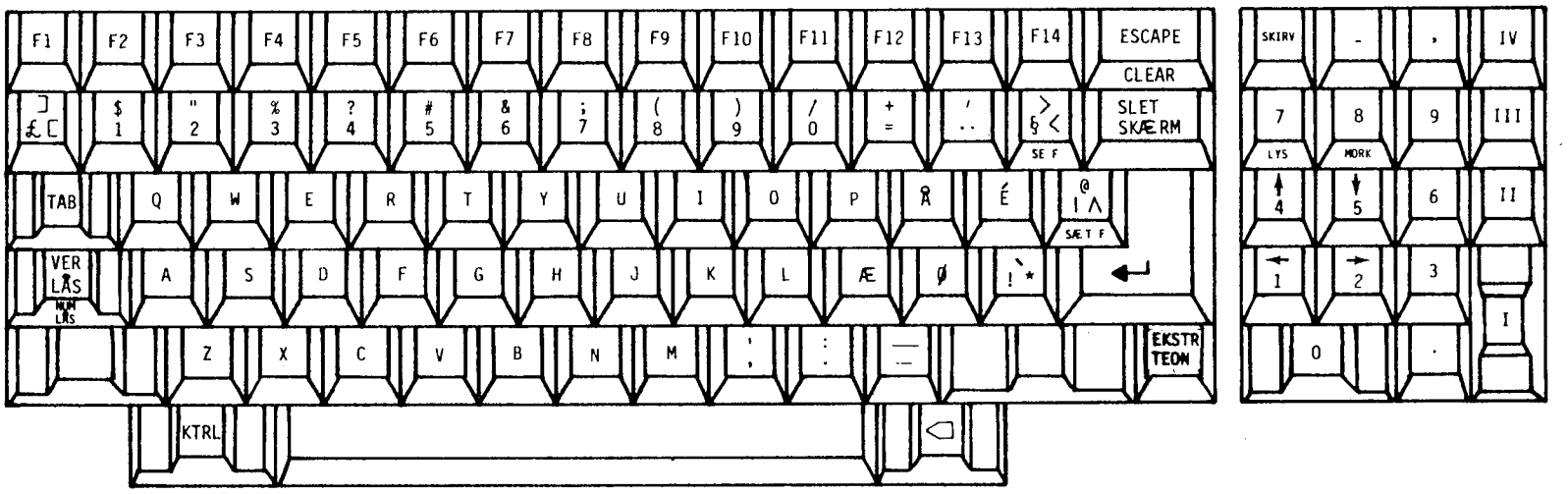
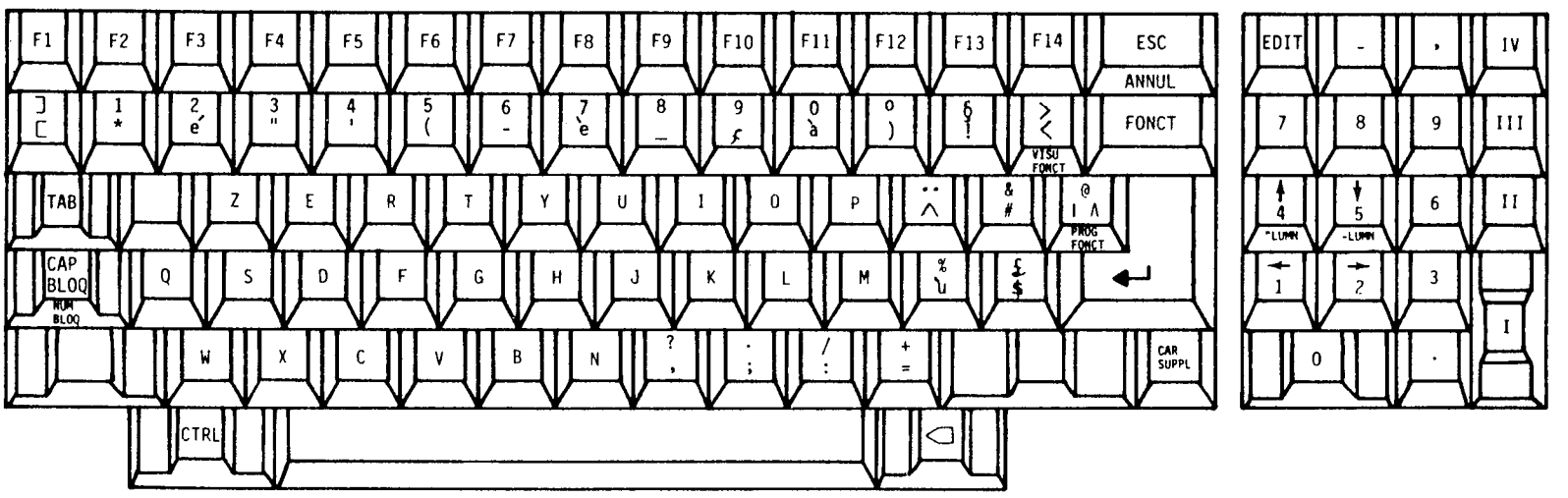


Figure 2-11. Layout, and Keyswitch Functions, Domestic Keyboard



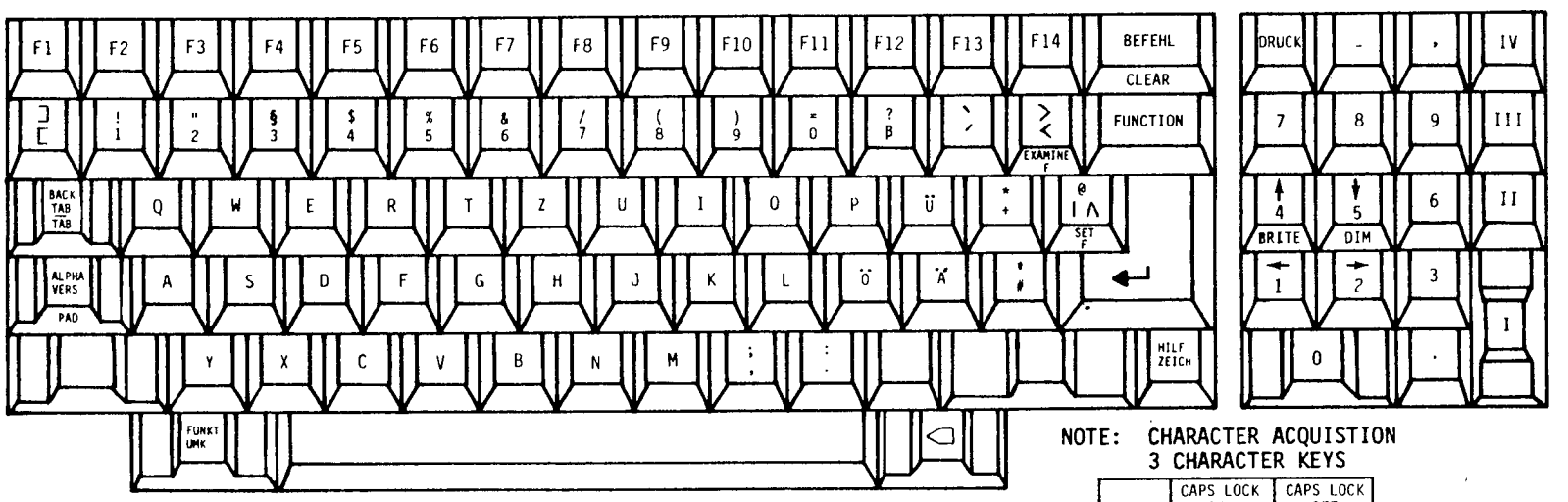
8070-14

Figure 2-12. Keyboard Layout, Danish



8070-15

Figure 2-13. Keyboard Layout, French

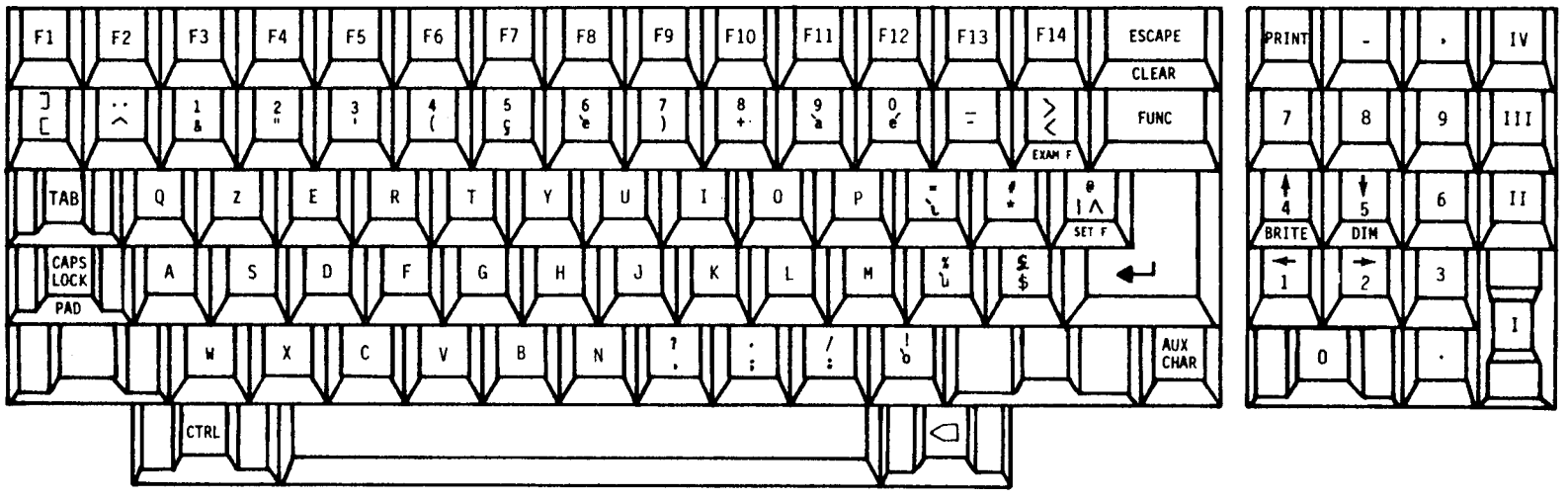


NOTE: CHARACTER ACQUISTION
3 CHARACTER KEYS

	CAPS LOCK ON	CAPS LOCK OFF
SHIFT ON	@	@
SHIFT OFF	!	"

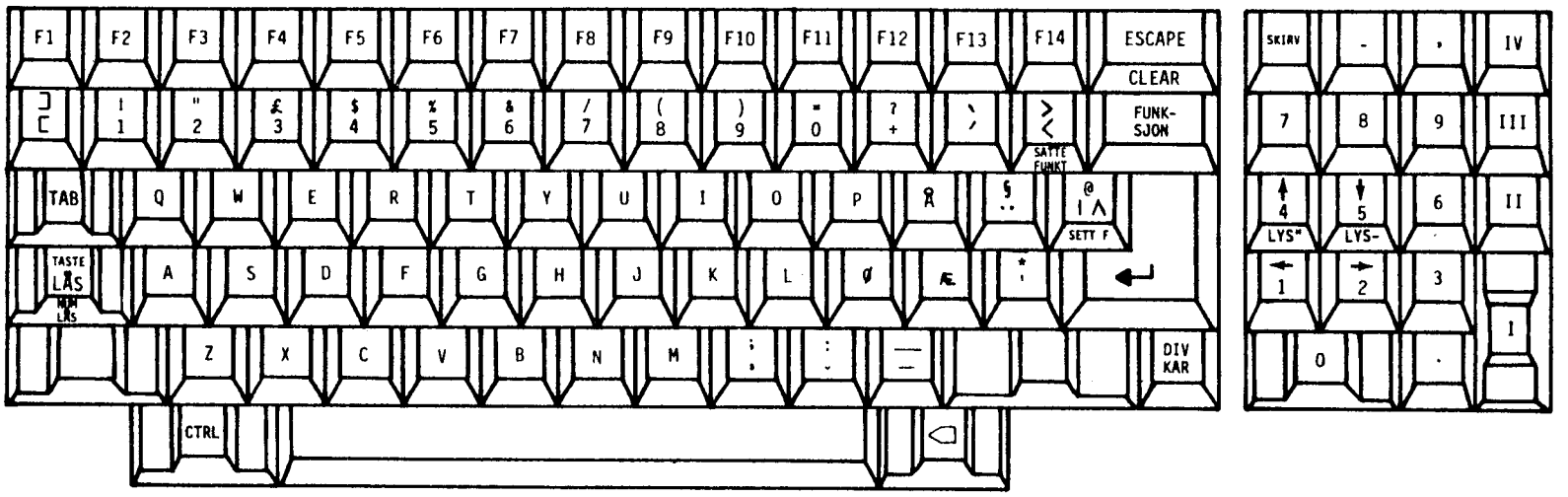
8070-16

Figure 2-14. Keyboard Layout, German



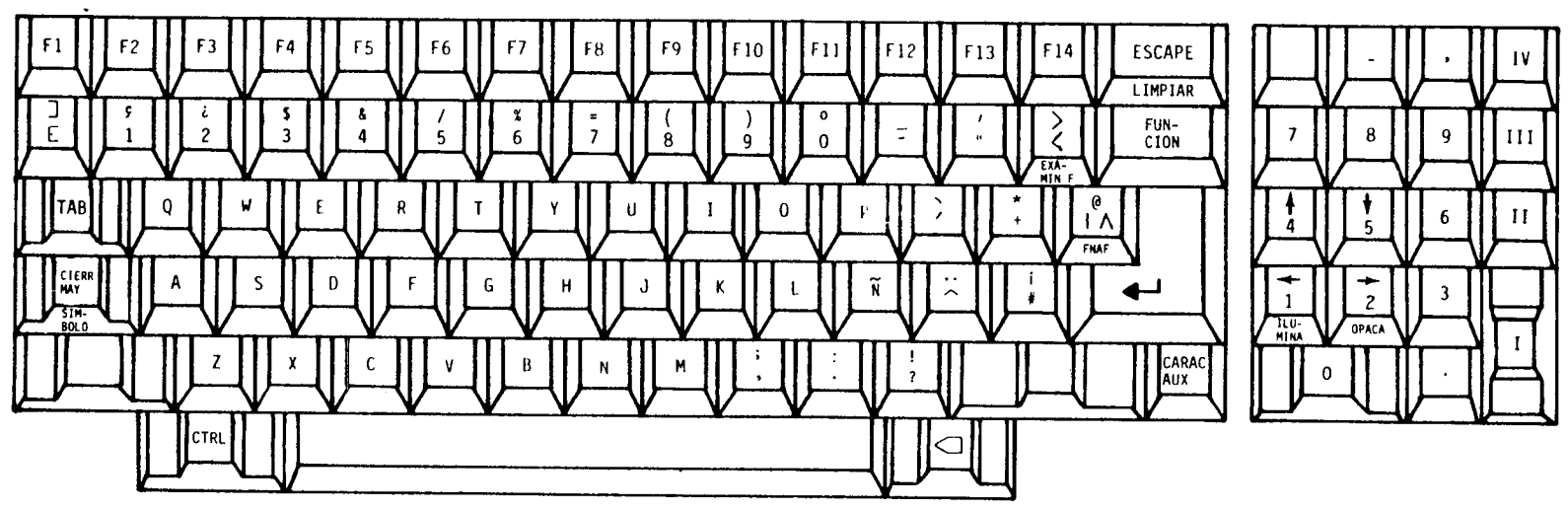
8070-17

Figure 2-15. Keyboard Layout, Italian



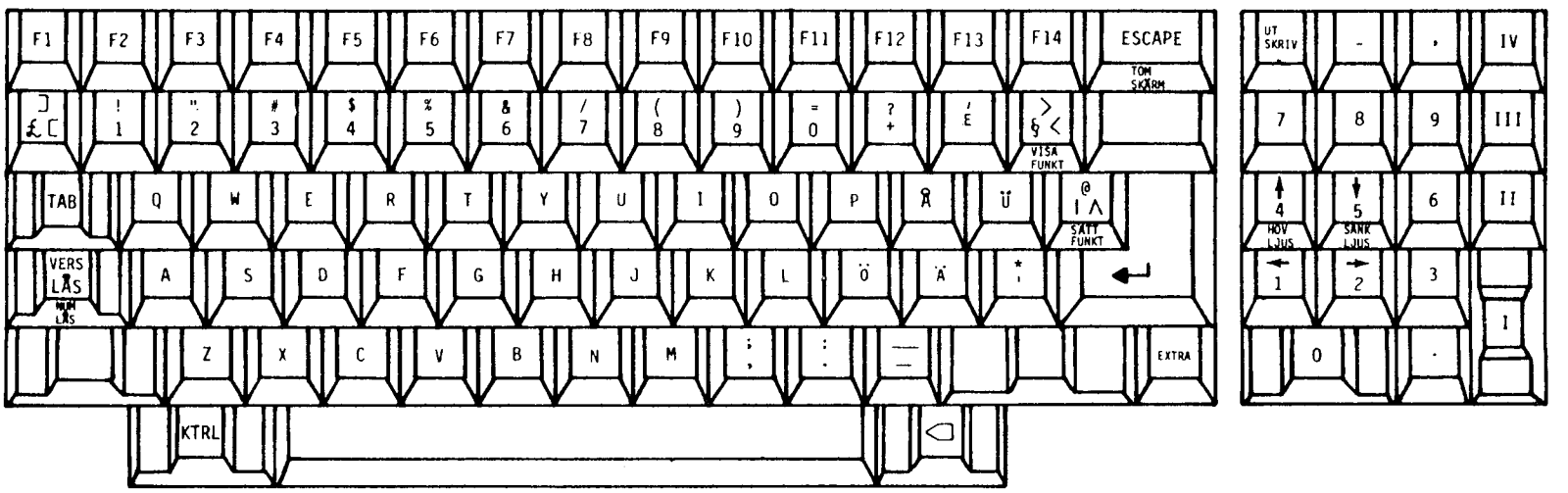
8070-18

Figure 2-16. Keyboard Layout, Norwegian



8070-19

Figure 2-17. Keyboard Layout, Spanish



8070-20

Figure 2-18. Keyboard Layout, Swedish

2.9.2 Standard Control Codes

The machine-type operations executed by the EVDT (carriage return, backspace, horizontal tab, etc.) are controlled by ASCII control codes. The control codes may originate at the host CPU or at the EVDT keyboard. All of the 32 standard control codes may be generated at the keyboard, but only those control codes highlighted in figure 2-19 and listed in table 2-4 are recognized by the EVDT as operational control codes. Non-operational control codes, when generated, are displayed as reversed video characters. Operational control codes are not displayable unless preceded by an ESCAPE character or unless the Enter Mode is set (paragraph 2.10.6). Whenever a control code is displayed, it will not be acted upon by the EVDT.

	CONTROL CHARACTERS		DISPLAYABLE CHARACTERS					
MSD / LSD	0	1	2	3	4	5	6	7
0	NUL	DLE		0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEEP	ETB	'	7	G	W	g	w
8	BS (←)	CAN	(	8	H	X	h	x
9	(SKIP) HT	EM	)	9	I	Y	i	y
A	LF (↓)	SUB	*	:	J	Z	j	z
B	VT (↑)	ESC	+	;	K	[	k	{
C	FF (→)	FS	,	<	L	\	l	¦
D	CR	GS	-	=	M	]	m	}
E	SO	(HOME) RS	.	>	N	^	n	~
F	SI	(NEW LINE) US	/	?	O	_	o	

EVDT CONTROL CODES

USE CTRL KEY WITH DISPLAY-ABLE CHARACTER KEYS TO PRODUCE EVDT CONTROL CODES

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Figure 2-19. Displayable Character Set (Standard Domestic) and EVDT Control Codes

Table 2-4. Operational Control Codes

CONTROL CODES		HEX CODE	OPERATION
FROM KEYBOARD	FROM HOST		
CTRL G	BEL	07	BEEP - Generates audible tone.
CTRL H or ←	BS	08	Back Space - Moves cursor left to next unprotected position on same line or on previous line, moving from right to left.
CTRL I or TAB	HT	09	Horizontal Tab - Skips cursor to next tab set position, when Protect Mode is set. If no such position, cursor moves to "HOME" (or next unprotected position) on screen.
CTRL J or ↓	LF	0A	Line Feed - Moves cursor to next lower line in same column position or to next unprotected position in new line or next line, if necessary.
CTRL K or ↑	VT	0B	Up Line - Moves cursor to previous line in same column position or to next unprotected position (moving from left to right) in new line or next line, if necessary.
CTRL L or →	FF	0C	Forespace - Moves cursor right to next unprotected position on same line or on next lower line, moving from left to right.
CTRL M or RETURN	CR	0D	Return - Moves cursor to first unprotected position in line containing the cursor. Indicates that data entry or data transmission is complete. Turns line over to host.
ESCAPE/CLEAR or CTRL [	ESC	1B	Escape - EVDT code extension character; must be followed by otherwise displayable character(s) to invoke a specific terminal operation. Also used preceding a control code to cause the control code to be displayed instead of acted upon.
CTRL ^	RS	1E	HOME - Moves cursor to first character position on screen. If "HOME" is protected, cursor moves to first unprotected positon on screen.
CTRL _	US	1F	New Line - Causes a combined Return (CR) and Line Feed (LF) to be executed. Moves cursor to first unprotected position on next line.

2.9.3 Self-Test Control Codes

The EVDT uses some otherwise-standard control codes as internal self-test control codes. The self-test control codes may be generated at the keyboard only, and only when the EVDT is in the Block Mode. The Self-Test Mode is entered by typing the escape sequence [ESCAPE/CLEAR] [U] . The specific self-test is executed following keyboard entry of the corresponding control code.

- [CTRL] [A] - ROM Checksum Test
- [CTRL] [B] - MPU Scratchpad RAM Test
- [CTRL] [C] - Display Memory RAM Test
- [CTRL] [D] - LSI Devices Register Test
- [CTRL] [G] - Tests Audible Tone

The successful completion of each test is indicated by an audible tone or "beep." Any other key pressed in the Self-Test Mode will cause the corresponding character to be displayed at every location on the display matrix, thus testing the character generator. The Self-Test Mode is terminated by pressing [ESCAPE/CLEAR] .

2.9.4 Escape Sequences

An escape sequence is formed by entering [ESCAPE/CLEAR] (or [CTRL] [[]) and one or more normally displayable ASCII characters. Each escape sequence controls a specific EVDT operation. Escape sequences can also be used to control the operation of a printer that is connected to the EVDT.

Many escape sequences emulate EVDT operations that are normally controlled by the host CPU. Other escape sequences are peculiar to local operations and effect only keyboard and/or display characteristics. Some escape sequences control EVDT operations that are one-time-only operations, while others remain functional for as long as power is applied, or until terminated by another escape code. Finally, there are certain escape sequences that may be initiated only from the host CPU and others that may be initiated only at the EVDT keyboard.

Figure 2-20 shows the escape sequences recognized by the EVDT, along their corresponding operations. Escape sequences are immediately acted upon by the EVDT, unless preceded by an additional ESC character or unless the Enter Mode (paragraph 2.10.6) is set. These exceptions will cause the escape-sequence code to be displayed, and not acted upon.

LSB	MSB 0	1	2	3	4	5	6	7
0	NUL	DLE		0 CLEAR ALL TABS	@ PRINT PAGE	P PRINT PAGE ALL	`	p UNFORMATTED PRINT
1	SOH	DC1	!	1 SET TAB	A PRINT BYPASS ENABLE	Q INSERT CHAR	a PRINT LINE	q SET INSERT
2	STX	DC2	" ENABLE KEYBOARD[2]	2 CLEAR TAB	B PRINT BYPASS DISABLE[2]	R DELETE LINE	b BLOCK MODE	r RESET INSERT
3	ETX	DC3	# DISABLE KEYBOARD[2]	3 SET TABS 8	C CONV MODE	S PARTIAL SEND	c	s SET SPLIT SCREEN[1]
4	EOT	DC4	$ ENABLE ALL FUNCTION KEYS	4 SEND LINE UNPROTECT	D TERMINAL ID.	T ERASE LINE FROM CURSOR (UNPROTECTED)	d	t CLEAR LINE FROM CURSOR (UNPROTECTED)
5	ENQ	NAK	% ENABLE SELECTIVE FUNCTION KEYS	5 SEND PAGE UNPROTECT	E INSERT LINE	U SET SELF TEST	e SET BRIGHTNESS LEVEL	u
6	ACK	SYN	& SET PROTECT MODE	6 SEND LINE ALL	F CHAR SIZE ATTRIBUTES[1]	V ENTER MODE	f RESET CHAR ATTRIBUTE	v RESET ENTER MODE
7	BEL	ETB	' EXIT PROTECT MODE	7 SEND PAGE ALL	G CHAR ATTRIBUTE[1] LINE	W DELETE CHAR	g CHAR ATTRIBUTE[1] PAGE	w
8	BS	CAN	(NORMAL INTENSITY RESET WRITE PROTECT	8 SMOOTH SCROLL ENABLE	H CHAR ATTRIBUTE[1] ALL	X	h CLOCK CONTROL[1]	x SETUP ENABLE
9	HT	EM	) REDUCED INTENSITY SET WRITE PROTECT	9 SMOOTH SCROLL DISABLE	I BACK TAB	Y ERASE PAGE FROM CURSOR (UNPROTECTED)	i TAB	y CLEAR PAGE FROM CURSOR (UNPROTECTED)
A	LF	SUB	* CLEAR ALL TO SPACES	: CLEAR ALL TO SPACES	J	Z RESET MODES	j EXAMINE FUNCTION KEYS	z RESET TERMINAL
B	VT	ESC	+ CLEAR TO SPACES (UNPROTECTED)	; CLEAR TO SPACES (UNPROTECTED)	K	[CURSOR MOVEMENT[1]	k SET FUNCTION KEYS	{
C	FF	FS	,	< ENABLE BUSINESS GRAPHICS	L	\ INVOKE FUNCTION KEY	l	|
D	CR	GS	-	= LOAD CURSOR ADDRESS[1,2]	M	] LOAD STATUS LINE[1]	m DOUBLE HEIGHT	}
E	SO	RS	SET PERSONALITY	> DISABLE BUSINESS GRAPHICS	N	^ READ CURSOR DATA	n READ STATUS LINE	~
F	SI	UT	/	? READ CURSOR ADDRESS[2]	O	_	o DISPLAY PERSONALITY	

1 Multiple Characters Required
2 Initiated From Host Only

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Figure 2-20. EVDT Escape Sequences

2.9.5 Special Function Codes and Operating Modes

Special function codes are those modified ASCII codes (or control signals) generated when using the [FUNC] key with any key designated as a special function key. Several of the special function keys bear legends according to their special, additional function. These include PAD, EXAM F, SET F, CLEAR, BRITE, and DIM (as described in figure 2-11). Other special function keys bear no legend as such. These include the numeric keypad [0] key, used to invoke the Setup Mode; the [A] key, used to invoke the Block Mode; and the [S] key, used to invoke the Conversation Mode (default condition at powerup). The operating modes selected through use of special function keys are summarized in table 2-5. Additional special function keys that bear no legend are those keys used for data editing, transmission, and printing operations. These operations, each of which is described in subsequent paragraphs, use the special function codes listed in tables 2-6 thru 2-8.

NOTE

The use of the special function keys listed in tables 2-6 thru 2-8 is enabled by the escape sequence [ESCAPE/CLEAR] [$] . To enable only those special function keys discussed in paragraph 2.9.5, enter [ESCAPE/CLEAR] [%] . (See figure 2-20.)

Table 2-5. Summary of Special Function Key Operating Mode Selection

MODE	KEYBOARD OPERATION	STATUS LINE DISPLAY
Conversation	[FUNC] [S] (Power-up Default Mode)	None
Block	[FUNC] [A]	Bk
Pad Lock	[FUNC] [CAPS LOCK/PAD]	Pd
Freeze	[FUNC] [F]	Fz
Setup	[FUNC] [0] (Numeric Keypad Zero Key)	N/A

Table 2-6. Data Editing Control Operations (Block Mode)

OPERATION	FROM KEYBOARD	FROM HOST	HEX CODE	DESCRIPTION
Clear Unprotected Display	FUNC | ESCAPE/CLEAR	ESC + or ESC ;	2B 3B	Unprotected data is cleared from display and replaced with space codes. Moves cursor to HOME or first unprotected positon.
Erase Line	FUNC | L	ESC T	54	All unprotected data, from cursor position to end of line (or current field if Protect Mode is set), are cleared to spaces. Write Protect Mode is reset.
Erase Page	FUNC | ;	ESC Y	59	All unprotected data, from cursor position to end of screen, is cleared to spaces. Write Protect Mode is reset.
Delete Line	FUNC | V	ESC R	52	Inactive in Protect Mode. Deletes all data on line in which cursor rests. All subsequent lines are moves up one line. Write Protect Mode is reset. Cursor position does not change.
Insert Line	FUNC | C	ESC E	45	Inactive in Protect Mode. Line in which cursor rests and all subsequent lines are moved down one line to create blank line. Data on bottom line is lost. Cursor position does not change. Write Protect Mode is reset.

Table 2-6. Data Editing Control Operations (Block Mode) (continued)

OPERATION	FROM KEYBOARD	FROM HOST	HEX CODE	DESCRIPTION
Delete Character	FUNC | X	ESC W	57	Deletes character under cursor and moves all unprotected characters located on right of cursor one positon to left. Protected characters under cursor and those following a Protected character are not affected. Write Protect Mode is reset.
Insert Character	FUNC | Z	ESC Q	51	All unprotected characters, from cursor position to end of line (or current field if Protect Mode is set), are moved one positon to right. Any character in last position of line (or field) is lost. Protected characters under cursor and those following a protected character are not affected. Write Protect Mode is reset.
Set Tab	FUNC | Q	ESC 1	31	Sets tab stop for column where cursor is positioned.
Clear Tab	FUNC | W	ESC 2	32	Clears tab stop from column where cursor is positioned.
Set Tabs Every Eighth Column	ESCAPE/CLEAR | 1	ESC 1	33	Sets tab stops for entire screen at every right column.
Clear All Tabs	FUNC | E	ESC 0	30	Clears all tab stops for all columns.

2.9.6 Data Editing Control Operations

The EVDT special function keys permit Block Mode editing of displayed data before transmission to the host CPU or local printer. Table 2-6 lists and describes the data editing operations that may be controlled from the EVDT keyboard, along the escape sequences permitting their control from the host CPU.

2.9.7 Data Transmission Control Operations

Special function codes and escape sequences permit selective transmission of displayed data when operating in the Block Mode. Table 2-7 lists and describes the data transmission operations that may be controlled from the EVDT keyboard, along with the escape sequences permitting their control from the host CPU. (Additional information on data transmission is provided in Section III.)

2.9.8 Print Transmission Control Operations

Table 2-8 lists and describes the print transmission operations that may be controlled from the EVDT keyboard, as well as the escape sequences permitting their control from the host CPU. (Additonal information on print transmisssion is provided in Section III.)

2.9.9 Business Graphics Mode

The escape sequence [ESCAPE/CLEAR] [<] from the keyboard (or ESC < from the host CPU) will place the EVDT in the Business Graphics Mode. While in this mode, the keys that normally produce alphabetical characters and certain punctuation characters will instead produce the graphics characters listed in table 2-9. [ESCAPE/CLEAR] [>] will disable the Business Graphics Mode.

2.10 EVDT PROGRAMMING

Several features of the EVDT are software controlled and require keyboard programming to establish or further define their characteristics. Examples are display attributes, which are established through keyboard programming, and the time-of-day clock display, which is further defined through keyboard programming (after Setup Mode selection of the AM/PM or 24-hour clock.)

Table 2-9. Business Graphics Characters

ASCII CHAR	GRAPHICS CHAR	HEX CODE		ASCII CHAR	GRAPHICS CHAR	HEX CODE
@	1/12 th —	00		f	└	61
A	2/12 th —	01		g	┴	62
B	3/12 th ▬	02		h	┘	63
C	4/12 th ▬	03		i	|	64
D	5/12 th ▬	04		j	─	65
E	6/12 th ▬	05		k	•	66
F	7/12 th ▬	06		l	ROW 1 AND 3	67
G	8/12 th ▬	07		m		68
H	9/12 th ▬	08		n		69
I	10/12 th ▬	09		o		6A
J	11/12 th ▬	0A		p		6B
K	12/12 th ▬	0B		q		6C
L	7/8 w ▬	0C		r		6D
M	6/8 w ▬	0D		s		6E
N	5/8 w ▬	0E		t		6F
O	4/8 w ▬	0F		u	┌	71
P	3/8 w ▬	10		v	┬	72
Q	2/8 w ▬	11		w	┐	73
R	1/8 w ▬	12		x	├	74
S	6/12 th ▬ up 1	13		y	┼	75
T	5/12 th ▬ up 2	14		z	┤	76
U	4/12 th ▬ up 3	15		!	¤	77
V	3/12 th — up 4	16		"	¥	78
W	2/12 th — up 5	17		$	µ	79
X	2/12 th ▬ up 6	18		%	©	7A
Y	3/12 th ▬ up 6	19		&	®	7B
Z	4/12 th ▬ up 6	1A		'	¶	7C
a	4/8 w ▬ RT 1	1B		(		7D
b	3/8 w ▬ RT 2	1C		)		7E
c	2/8 w ▬ RT 3	1D		*		
d	2/8 w ▬ RT 4	1E				
e	3/8 w ▬ RT 4	1F				

2.10.1 Setting AM/PM or 24-Hour Clock Display

Use the following procedure to program (set) the AM/PM (12-hour) or 24-hour (military time) clock display.

1. Place EVDT in Block Mode by entering [FUNC] [A] at the keyboard.
2. Enter [ESCAPE/CLEAR] [h] to enable Clock Control Mode.
3. If necessary, increment clock display by the hour from AM to PM (or from PM to AM) by repeatedly entering [2] from the list of codes in table 2-10. If AM/PM change is not required, proceed to step 4.
4. Enable setting of hours display by entering [5] from list of codes in table 2-10.
5. Set value of hours display by entering appropriate ASCII character from list in table 2-11 (e.g., [+] for 11:00 AM or PM).
6. Repeat procedure to set value of minutes display and seconds display (using codes 6 and 7 in table 2-10 and the ASCII characters in table 2-11).
7. The following notations summarize the clock setting procedure.
   - [FUNC] [A] (Block Mode)
   - [ESCAPE/CLEAR] [h] (Clock Control Mode)
   - [2] [2] [2] . . . . (increment hours for AM/PM) or
   - [5] [ASCII] (set hours)
   - [6] [ASCII] (set minutes)
   - [7] [ASCII] (set seconds)

Table 2-10. Clock Set Command Codes

CODE	COMMAND	DESCRIPTION
0	Time Indicator On	Displays Time Indicator
1	Time Indicator Off	Does not display Time Indicator
2	Increment Hour	Advances Hour Display 1 Hour
3	Increment Minute	Advances minute display 1 minute
4	Real Time Indicator	Four bytes are sent to the host computer when this command is invoked. They represent hour, minute, second, and carriage return. The hour, minute, and second are actual values plus 20 hex.

Table 2-10. Clock Set Command Codes (continued)

CODE	COMMAND	DESCRIPTION
5	Write Hour	The value entered is loaded into the hour display digit minus 20 (Refer to table 2-11.)
6	Write Minute	The value entered is loaded into the minute display digit minus 20 (Refer to table 2-11.)
7	Write Second	The value entered is loaded into the second display digit minus 20 (Refer to table 2-11.)

Table 2-11. ASCII Code Conversion, Clock Display Values

CLOCK DISPLAY VALUE	ASCII CHAR	HEX CODE	CLOCK DISPLAY VALUE	ASCII CHAR	HEX CODE
0	SPACE	20			
1	!	21	31	?	3F
2	"	22	32	@	40
3	#	23	33	A	41
4	$	24	34	B	42
5	%	25	35	C	43
6	&	26	36	D	44
7	'	27	37	E	45
8	(	28	38	F	46
9	)	29	39	G	47
10	*	2A	40	H	48
11	+	2B	41	I	49
12	,	2C	42	J	4A
13	-	2D	43	K	4B
14	.	2E	44	L	4C
15	/	2F	45	M	4D
16	0	30	46	N	4E
17	1	31	47	O	4F
18	2	32	48	P	50
19	3	33	49	Q	51
20	4	34	50	R	52
21	5	35	51	S	53
22	6	36	52	T	54
23	7	37	53	U	55
24	8	38	54	V	56
25	9	39	55	W	57
26	:	3A	56	X	58
27	;	3B	57	Y	59
28	<	3C	58	Z	5A
29	=	3D	59	[	5B
30	>	3E	60		5C

2.10.2 Establishing Protected Fields

Protected fields are those areas on the EVDT display that cannot be overwritten, deleted, erased, or cleared. Any type of form appearing on the display, especially when originating at the host CPU, will usually have its characters, attributes, and graphics set in protected fields. These fields are easily identified by their reduced intensity characters, and by the fact that the cursor cannot be located upon any protected character in the field. When protected fields are present, "Pr" (Protect Mode) is displayed on the status line and the insert line, delete line, and scrolling functions are disabled.

Protected fields are established through a four-step process. First, the Write Protect Mode is set (from host or keyboard) by executing ESC). The characters forming the protected field are then entered and are displayed at reduced intensity. Next, the Write Protect Mode is disabled by executing ESC (. Finally, the Protect Mode is set by executing ESC &. "Pr" is displayed on the status line and all characters displayed at reduced intensity are established as a protected field.

The Protect Mode is disabled by the escape sequence ESC '. All characters are displayed at full intensity and may be overwritten.

2.10.3 Selecting Display Attributes

Display attributes are those visual characteristics assignable to a character, line, or entire display. The selection and assignment of display attributes is accomplished through a three character escape sequence: [ESC] [Assignment Code] [Attribute Code] . The codes for assigning an attribute to a character, line, or an entire screen are listed in table 2-12. The codes for selection of the desired display attribute are listed in table 2-13.

An example of assigning and selecting a display attribute is: [ESC] [G] [4] ; where "ESC G" assigned the attribute to an entire line and "4" selected the reverse video attribute.

Table 2-12. Display Attribute Assignment Codes

CODE	DESCRIPTION
g (character)	Assigns the Attribute from the cursor position to all characters which follow. No display positions are used to store the attribute.
f	Clears the character (g) Attribute.
G (line)	Assigns the Attribute to characters from the cursor position to the end of the line. A blank protected character is stored where the Attribute is invoked and where it is reset or altered using G.
H (page)	Assigns the Attribute to the entire screen.

Table 2-13. Display Attribute Selection Codes

CODE	ATTRIBUTE
0	No attributes (normal display)
1	Underlined
2	Blinking
3	Underlined, blinking
4	Reverse video
5	Reverse video, underlined
6	Blinking, reverse video
7	Reverse video, blinking, underlined
8	Reduced intensity
9	Underlined, reduced intensity
A	Blinking, reduced intensity
B	Underlined, blinking, reduced intensity
C	Reverse video, reduced intensity
D	Reverse video, underlined, reduced intensity
E	Blinking, reverse video, reduced intensity
F	Reverse video, blinking, underlined, reduced intensity

2.10.4 Selecting Character Size Attributes

The available character size attributes, and the escape sequences required for their implementation, are listed and described in table 2-14.

Table 2-14. Character Size Attributes

ATTRIBUTE	ESCAPE SEQUENCE	HEX CODE	DESCRIPTION
Double-High, Double-Wide Line	ESC F 7 (Top Half) ESC F F (Bottom Half)	(46,37) (46,46)	The escape sequence ESC F 7 or ESC F F causes the line with the active cursor position to become the top or bottom half, respectively, of a double-high, double-wide line. The escape sequences must be used in pairs on adjacent lines, as the same character output is sent to both lines to form the double-high, double-wide character. The use of this feature reduces the number of characters per line by half.
Double-Wide Line	ESC F 3	46,33	The escape sequence ESC F 3 causes the line with the active cursor position to contain double-wide, single-height characters. The use of this feature reduces the number of characters per line by half.

Table 2-14. Character Size Attributes (continued)

ATTRIBUTE	ESCAPE SEQUENCE	HEX CODE	DESCRIPTION
Double-High Line	ESC F 5 (Top Half) ESC F D (Bottom Half)	(46,35) (46,44)	The escape sequence ESC F 5 or ESC F D causes the line with the active cursor position to become the top or bottom half, respectively, of a double-high line. The escape sequences must be used in pairs on adjacent lines, as the same character output is sent to both lines to form the double-high character.
Double-High Line (Alternate Method)	ESC m	6D	Double high characters can alternately be generated from normal size or double-wide characters, after the characters have been entered. The following sequence is an example of how to generate double-high, double-wide characters using the alternate method: ESCAPE F 3 (Double-Wide) then Desired Characters then ESCAPE "m" (Double-High).

2.10.5 Function Key Programming

The Programmable Function Keys, F1 thru F14 (and F15 thru F28 when SHIFTed), may be individually programmed to store user-selected commands in continuous memory. The stored commands are executed by pressing the key selected for each command.

The Programmable Function Keys are associated with a 300-character data buffer, which allocates a maximum of 77 characters to each key. Commands with character strings exceeding 77 characters may be stored under two or more function keys and linked together in continuous memory as a single string. The stored character-string commands may include, in addition to user BASIC commands, control codes and escape sequences for unique program applications.

The Special Function Keys [^ /SET F] and [↓ /EXAM F] are used to store and examine the character strings entered for each Programmable Function Key.

Program the function keys as follows:

1. Place EVDT in Block Mode ([FUNC] [A]).

2. Locate cursor in first column of any line.

3. Enter number of function key to be programmed (01 to 28).

4. Enter desired character string to be stored (77 characters maximum). Control codes may be entered by executing [ESCAPE/CLEAR] [CTRL] [ASCII]. Escape sequences may be entered by executing [ESCAPE/CLEAR] [ESCAPE/CLEAR] [ASCII].

5. Verify that cursor is one position to right of last character entered.

6. Enter [FUNC] [^ /SET F] to store character string. (ESC k from host CPU).

7. If the stored character string is to be linked with a continuation of that string in the next (or another) function key, or a set of commands are to be linked in sequence, enter [ESCAPE/CLEAR] [ESCAPE/CLEAR] [\] and the number of the function key to which the character string stored in step 6 will be linked.

8. Store the continuation of the character string, or the next command in the linked set, by repeating steps 4,5 and 6.

9. Enter [FUNC] [↓ /EXAM F] (ESC j from host CPU) to verify (view) the commands stored for function keys 01 thru 12. A display similar to that shown in figure 2-21 will appear on the screen. The commands stored for function keys 13 thru 28 may be viewed by entering [SHIFT] [FUNC] [↓ /EXAM F].

10. Edit the commands stored for any function key by overwriting the command as required. Store revised commands by moving cursor one position to right of last character in revised command and entering [FUNC] [^ /SET F].

11. To erase commands stored for any function key, enter number of function key in first two columns of display, move cursor one postion to right of numbers, and enter [FUNC] [^ /SET F] (ESC k from host CPU).

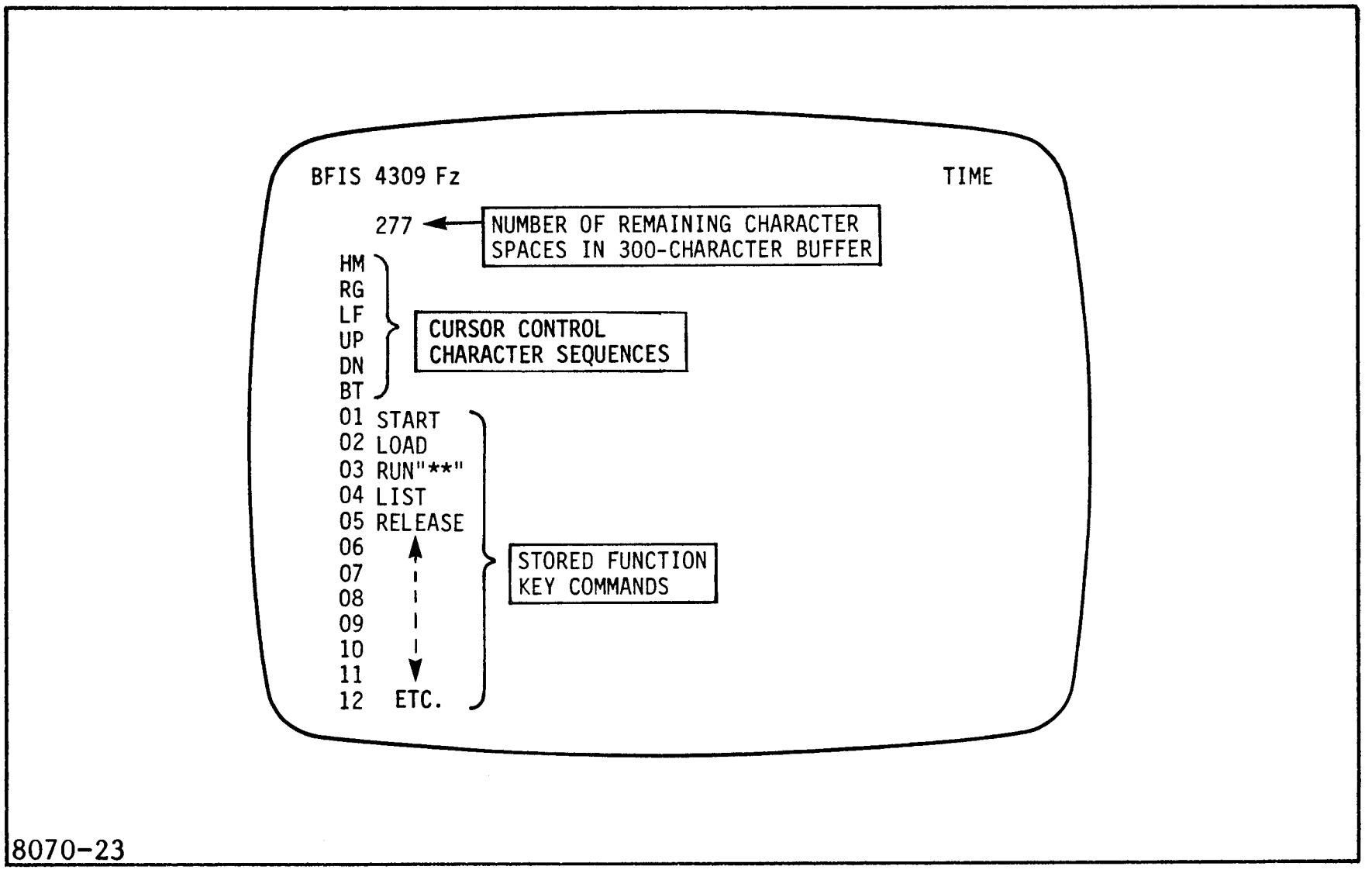


Figure 2-21. Display of Programmed Function Key Commands (Keys 01 thru 12)

2.10.6 Using the Enter Mode

The Enter Mode permits control characters to be displayed along with incoming data streams. This mode of operation is useful in debugging and troubleshooting situations, where it is desired to examine the incoming data without executing the control codes. The Enter Mode is also useful when entering control codes for the Programmable Function Keys, as the [ESCAPE/CLEAR] key need not be pressed before each control code is entered.

The Enter Mode is set with ESC V from the keyboard (in Block Mode) or host CPU. The Enter Mode is reset with ESC v (from keyboard or host).

2.10.7 Using the Insert Mode

The Insert Mode permits characters to be inserted without use of the Insert Character command (table 2-6). In this mode, all unprotected characters, from the cursor positon to the end of the line, are moved one position to the right after a character is entered. If the line was full before the entry, the last character on the line is lost. If a protected field is encountered, and characters cannot be shifted to the right, the Insert Mode will not function.

The Insert Mode is set with ESC q from the keyboard (in Block Mode) or host CPU. The Insert Mode is reset with ESC r (from keyboard or host).

2.10.8 Setting the Limited Screen Mode

The Limited Screen Mode limits the number of active display lines available to the EVDT operator. The number of active lines to which the display is limited, and the location of the active lines on the display (top, middle, bottom) is at the user's discretion (or as commanded by system software).

To set the Limited Screen Mode, enter [ESCAPE/CLEAR] [s] (in Block Mode). Then enter the ASCII characters from table 2-15, which correspond to the starting and ending row numbers (1 to 24) of the active display lines. An example of setting this mode is: [ESCAPE/CLEAR] [s] [$] [+] . This escape sequence would establish lines 5 thru 12 as the active lines. The cursor would appear at the first character position of line 5, and (the cursor) would be restricted to movement within lines 5 thru 12.

Table 2-15. Row Select and Cursor Positioning Codes

ROW (Y) OR COL. (X)	ASCII CHAR	HEX CODE	COL. (X)	ASCII CHAR	HEX CODE	COL. (X)	ASCII CHAR	HEX CODE
1	SPACE	20	25	8	38	53	T	54
2	!	21	26	9	39	54	U	55
3	"	22	27	:	3A	55	V	56
4	#	23	28	;	3B	56	W	57
5	$	24	29	<	3C	57	X	58
6	%	25	30	=	3D	58	Y	59
7	&	26	31	>	3E	59	Z	5A
8	'	27	32	?	3F	60	[	5B
9	(	28	33	@	40	61	\	5C
10	)	29	34	A	41	62	]	5D
11	*	2A	35	B	42	63	^	5E
12	+	2B	36	C	43	64	-	5F
13	,	2C	37	D	44	65	'	60
14	-	2D	38	E	45	66	a	61
15	.	2E	39	F	46	67	b	62
16	/	2F	40	G	47	68	c	63
17	0	30	41	H	48	69	d	64
18	1	31	42	I	49	70	e	65
19	2	32	43	J	4A	71	f	66
20	3	33	44	K	4B	72	g	67
21	4	34	45	L	4C	73	h	68
22	5	35	46	M	4D	74	i	69
23	6	36	47	N	4E	75	j	6A
24	7	37	48	O	4F	76	k	6B
			49	P	50	77	l	6C
			50	Q	51	78	m	6D
			51	R	52	79	n	6E
			52	S	53	80	o	6F

2.10.9 Remote Cursor Commands

Three remote cursor commands are available: Set Cursor Position, Read Cursor Position, and Read Cursor Content.

The Set Cursor Position command is executed upon reception of the four-character sequence [ESC][=][Y Coordinate] [X Coordinate] . Execution of the command causes the cursor to move to a specific location in the display matrix, which corresponds to the codes for the Y (row) and X (column) coordinates transmitted by the host. No distinction is made concerning protected fields. The codes for all possible cursor positions are shown in table 2-15.

The Read Cursor Position command is executed upon reception of the sequence ESC ?. Execution of the command causes the codes for the Y (row) and X (column) coordinates of the current cursor positon, followed by a carriage return, to be transmitted to the host CPU.

The Read Cursor Content command is executed upon reception of the sequence ESC ^ . Execution of the command causes the character content at the current cursor position, followed by a carriage return, to be transmitted to the host CPU.

2.10.10 Terminal ID/Answer-Back Message

The Terminal ID/Answer Back Message is transmitted to the host CPU upon reception of the sequence ESC d. The ID/Answer Back Message consists of eight characters followed by a carriage return. The eight characters in the identifying answer-back message provide the following information.

CHARACTER SEQUENCE	CODED INFORMATION	ASCII CHARACTER	HEX CODE
1	VDT Type	F	46
2,3	Firmware Rev. Level (Example: V0.09.0)	0,9	30,39
4	Language in Use:		
	Standard	0	30
	French	1	31
	Italian	2	32
	Swedish	3	33
	Spanish	4	34
	Norwegian	5	35
	German	6	36
	Danish	7	37
5,6,7,8	Reserved	SPACE	20
9	Carriage Return	CR	OD

2.10.11 Changing Personality Attributes

The codes for the personality attributes exhibited by the EVDT are shown in figure 2-22. These codes may be displayed on the screen by entering ESC o from the keyboard (in Block Mode) or host CPU. The displayed codes are hex codes indentifying the ASCII character that represents a given attribute. When the displayed hex code is 00, it represents NULL or a NO-OP condition.

Temporary modifications may be made to personality attributes through the use of personality change codes. Any modification made to a personality code will be reset to its default value following a Keyboard Master Reset or power-off/ power-on sequence.

Personality change codes are entered from the keyboard (in Block Mode) or host CPU by the sequence [ESC] [.] [Control Code from figure 2-21] [Selected ASCII Replacement Character] . For example, a sequence of [ESCAPE/CLEAR] [.] [CTRL] [H] [*] would replace the ERASE/CLEAR replacement character (SPACE or hex 20) with an asterisk (*). When the personality change is verified by entering [FUNC] [ESCAPE/CLEAR] , all 1920 positions in the display matrix would be filled with asterisks.

Another example of a personality change sequence would be [ESCAPE/CLEAR] [.] [CTRL] [@] [ ]] . This would add the character] to the standard EVDT escape lead-in character. The EVDT would then respond to either escape character. During Send All transmisssions, however, the character] would be sent instead of ESC.

A final example of a personality change sequence is [ESCAPE/CLEAR] [.] [CTRL] [F] [0] [0] . This would change the standard SOH function lead-in character to NUL.

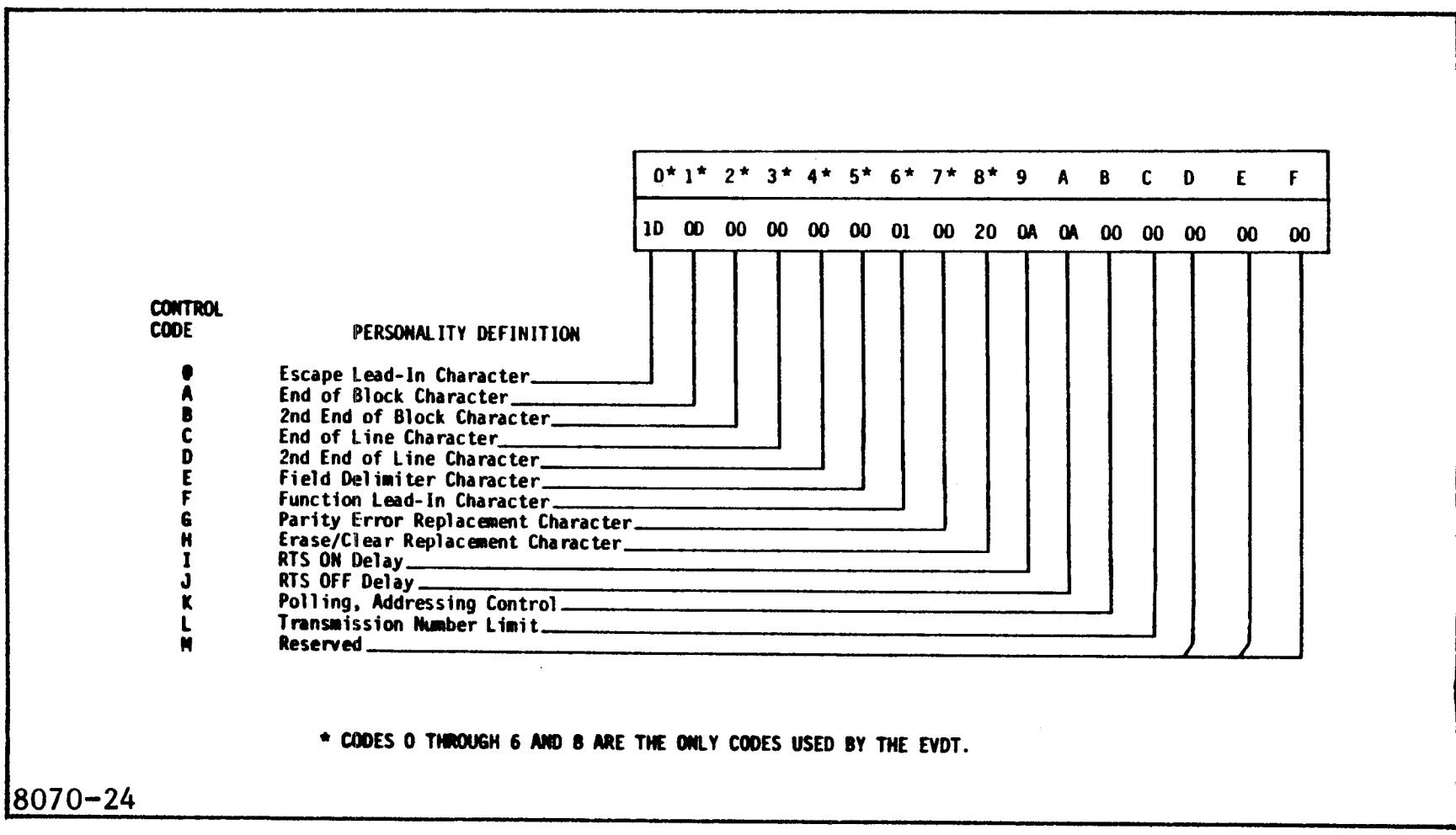


Figure 2-22. Personality Attribute Codes

Table 2-7. Data Transmission Control Operations (Block Mode)

OPERATION	FROM KEYBOARD	FROM HOST	HEX CODE	DESCRIPTION
Send Line Unprotected	FUNC | N	ESC 4	34	Sends line of unprotected data, followed by carriage return (CR) character, to host CPU. Transmission starts at beginning of line and ends at cursor postion.
Send Line All	ESCAPE/CLEAR | 6	ESC 6	36	Sends line of unprotected and protected data, followed by a carriage return (CR) character, to host CPU. Transmission starts at beginning of line and ends at cursor position. ESC) and ESC (are transmitted to set and reset Write Protect Mode.
Send Page Unprotected	FUNC | M	ESC 5	35	Sends all unprotected data on screen, followed by a carriage return (CR) character, to host CPU. Transmission starts at HOME position and ends at cursor postion.
Send Page All	ESCAPE/CLEAR | 7	ESC 7	37	Sends all unprotected and protected data on screen, followed by a carriage return (CR) character, to host CPU. Transmission starts at HOME position and ends at cursor position. ESC) and ESC (are transmitted to set and reset Write Protect Mode.
Partial Send	ESCAPE/CLEAR | S	ESC S	53	Writes FS code at cursor positon and backspaces cursor to previous FS code or HOME position. Transmission starts at beginning of first line following first FS code or at first unprotected character following HOME. CR is transmitted at end of message and cursor is returned to position where ESC S was entered.

Table 2-8. Print Transmission Control Operations

OPERATION	FROM KEYBOARD	FROM HOST	HEX CODE	DESCRIPTION
Print Line Unprotected	[FUNC] [.]	ESC a	61	Sends line of unprotected data, followed by a carriage return (CR) character, to serial printer. Transmission starts at beginning of line and ends at cursor postion.
Print Page Formatted/Print Page All	[PRINT]	ESC P	50	Sends all data on screen, line for line, to serial printer. Transmission starts at HOME position and ends at cursor position. If initiated by host (ESC P), seven byte status message is returned to host following print operation.
Print Page Unprotected	[FUNC] [-]	ESC @	40	Send all unprotected data on screen to serial printer. Transmission starts at HOME position and ends at cursor position. Protected data is sent as spaces.
Print Page Unformatted	[ESCAPE/CLEAR] [p]	ESC p	70	Send all data on screen, including nulls with no carriage returns or line feeds, to serial printer. Transmission starts at HOME position and ends at cursor position.
Display Bypass Print	[ESCAPE/CLEAR] [A] (Disabled by host only)	ESC A	41	All characters received from host CPU are passed on to serial printer and are not displayed on screen. All characters received from printer are passed on to host CPU. EVDT keyboard does not respond in Display Bypass mode - mode disabled by ESC B from host only.

2.10.12 EVDT Reset Operations

Two EVDT reset operations are available: Reset Terminal and Keyboard Master Reset.

Reset Terminal is executed upon reception of ESC z from the host CPU or by entering [CTRL] [FUNC] [ESCAPE/CLEAR] at the keyboard. This reset operation causes all data on the screen and in the input data buffer to be lost.

Keyboard Master Reset is executed by entering [CTRL] [SHIFT] [FUNC] [ESCAPE/CLEAR] at the keyboard. This reset operation not only causes all data on the screen and in the input data buffer to be lost, but also erases the content of all Programmable Function Keys and resets all Personality attributes and Setup Mode parameters to their default values.

2.10.13 Keyboard Enable/Disable

Keyboard disable is executed upon reception of the sequence ESC # from the host CPU only. All key presses are ignored. "Kl" (keyboard lock) will appear on the display status line.

Keyboard enable is executed upon reception of the sequence ESC " from the host CPU only. "Kl" will be removed from the display status line.

2.10.14 Title Indicator Modification

A user-definable title with 1 to 10 double-width, single-height characters may be displayed at the left side of the display status line. When shipped from the factory the EVDT displays its model number in the title area (see figure 2-21). This title may be changed as described in the following paragraphs.

To write a new title on the status line, enter ESC] , then the new title, from the keyboard (in Block Mode) or host CPU. If fewer than 10 characters are entered, fill the remaining positions with spaces to clear previous data.

To read the title (transmit to host), enter ESC n from keyboard (in Block Mode) or host CPU. (Read title is terminated by a carriage return only when the EVDT is connected to the host or another terminal.)

SECTION III

FUNCTIONAL DESCRIPTION

3.1 INTRODUCTION

This section provides a functional description of the Model 4309 EVDT. Included are a discussion of the general design principles; functional descriptions, written to the block diagram level; detailed descriptions, written to the logic diagram level; and a brief description of firmware operation.

3.2 GENERAL DESIGN PRINCIPLES

The following paragraphs briefly describe the display screen with respect to the display matrix and the display storage. Character formation and generation are also described. This information is supplied as a prelude to the functional and detailed circuit descriptions to acquaint the service technician with some of the design requirements.

The size of the display, in accordance with standard industry practice, is expressed as a number of characters, which, in the case of the EVDT, is 24 rows X 80 columns (24 X 80 = 1920 characters). If the character positions are numbered sequentially from left to right, row by row, in normal reading order, the display matrix appears as shown in figure 3-1. The positional arrangement is fixed and is called a page. Each position may display a character or it may be blank, noting that a blank has a character code.

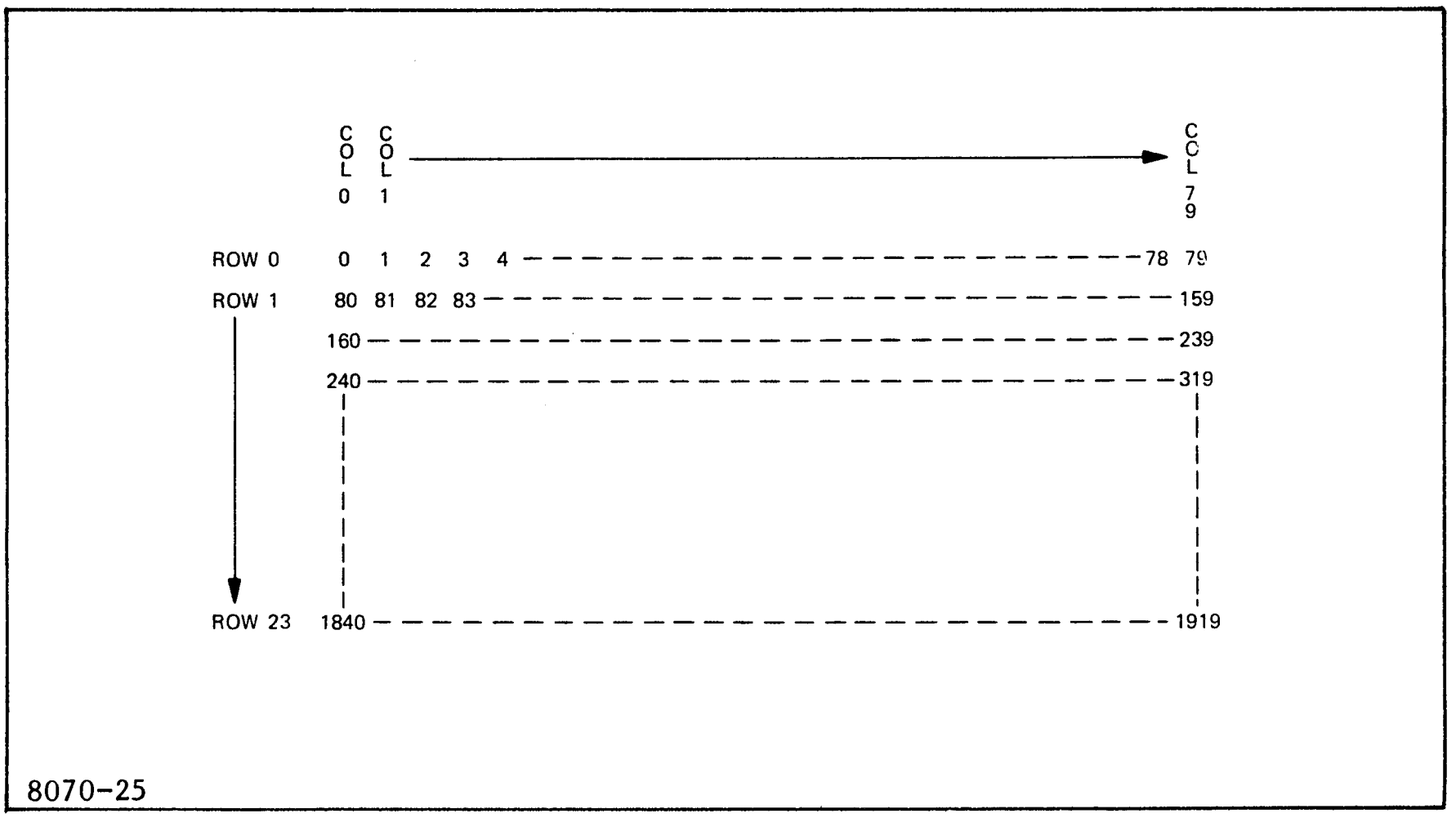


Figure 3-1. Display Screen Matrix (24 X 80)

In simple terms, each numerical position in the display matrix has a corresponding location in screen memory, such that the character code in the location whose address is 0 generates the character that is displayed in matrix position 0, and so on.

It follows that in a 24 X 80 display matrix, there must be 1920 locations in screen memory. It is impractical to devise a memory addressing scheme for 1920 locations, so the actual screen memory contains 2048 locations. In practice, the display is split in half in terms of screen memory, such that each segment contains 1024 locations, which corresponds to 2^{10} in binary notation, i.e., 10 binary digits (bits) are required to address 1024 memory locations.

In association with screen memory are two segments of screen attribute memory, each containing 1024 locations, which have a direct correlation with the corresponding addresses in screen memory. Screen attribute memory determines how the display is to appear for a particular character position, e.g. blinking or steady, or in reverse video (dark on a light background instead of the normal light character on a dark background).

Each character appears as a contiguous dot pattern, called the character matrix. The actual character matrix is 8 X 12 dot positions, and the normal character size is 6 X 10 dots, as shown in figure 3-2. Each character dot is assigned a row and column position in the matrix or character raster. Generation of the character matrix or raster is controlled by the character generator. The two unused rows and columns in the matrix provide line spacing and character spacing respectively. Figure 3-2 represents the display of an upper case H.

The MPU synchronizes the vertical sync pulse (or retrace period).

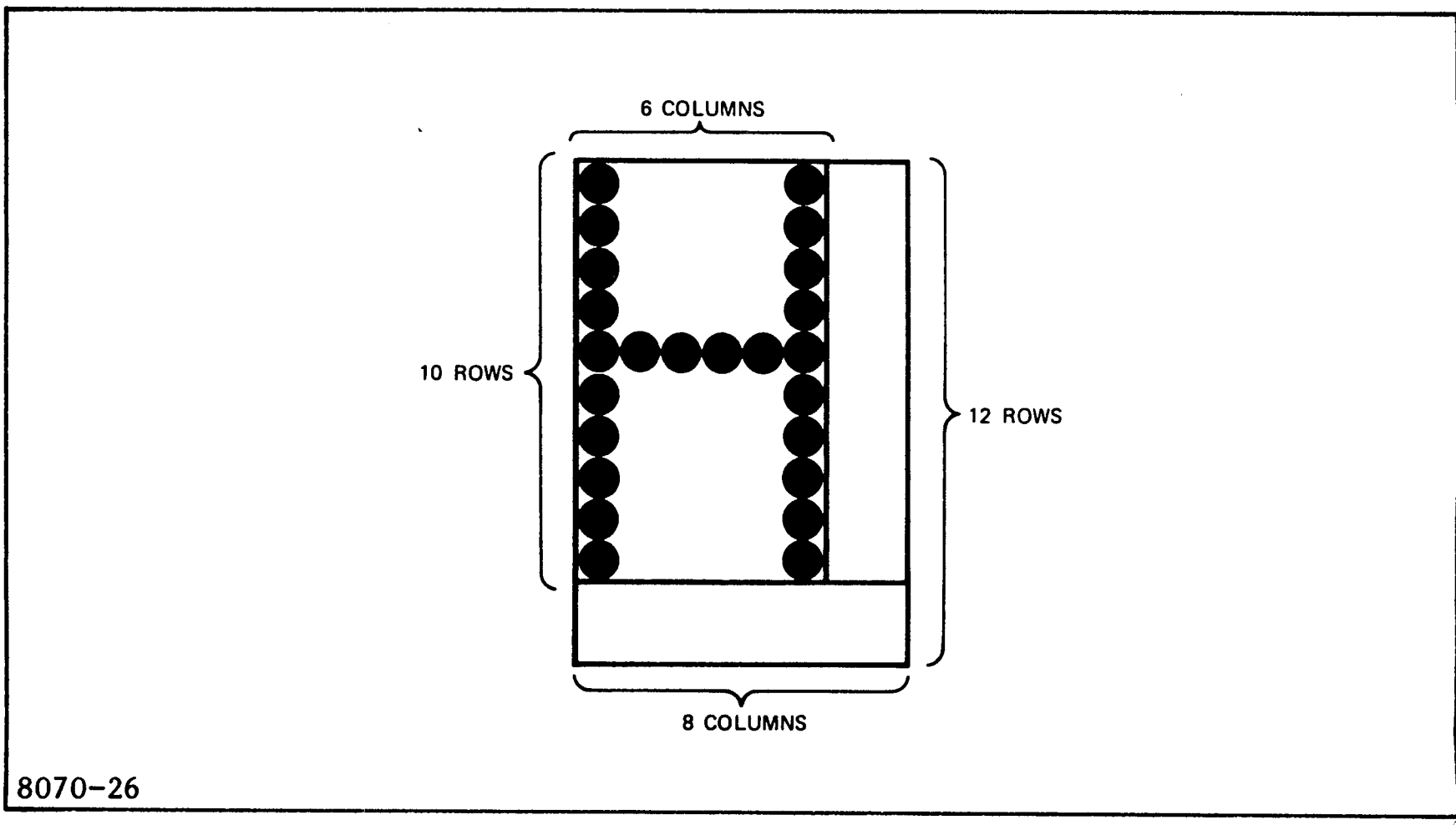


Figure 3-2. Character Matrix

3.3 BLOCK DIAGRAMS

Section III contains two block diagrams, figures 3-3 and 3-4, which depict the Main Logic Board and the keyboard, respectively, in terms of the principal logic elements and circuits.

Figure 3-3 shows the MPU with its address and data bus, the main memory, screen memory, CRT controller, character generators and character control logic, communications interface, and keyboard interface. For the sake of clarity, certain logic circuits are not shown in figure 3-3. These include the clock generator and clock signals, memory and I/O address decoders, and the individual control signals. Some blocks in the diagram have sheet numbers for ease of reference (i.e., "SH5" means Logic Board Diagram, Sheet 5, in Section VI).

Figure 3-4 shows the keyboard matrix, with its column select and row scanner, the timing control logic, the deserializer (serial-to-parallel converter), and the output latch. The keyboard logic diagram is a single drawing in Section VI, such that no sheet number references are required on the block diagram.

3.4 MAIN LOGIC BOARD

The following functional descriptions of the Main Logic Board are referenced to figure 3-3.

3.4.1 Microprocessor Unit

The Microprocessor Unit (MPU) is a Zilog Z-80A (Z-80A is a trademark of Zilog, Inc.). It executes the instructions contained in the Read Only Memory (ROM) segment of main memory. The instructions form the operating system program, referred to as the firmware.

The MPU controls, synchronizes, and sequences the events that take place in the terminal. It communicates with all of the other logic devices, including main memory, over the 8-bit bidirectional data bus. The particular device is addressed (selected) by means of a unique bit pattern appearing on the 16-bit address bus. Once the device is selected (by address recognition), the MPU either sends data to the device (write) or takes available data from the device (read).

When a particular device requires service from the MPU, the device interrupts the MPU. The MPU acknowledges the interrupt, then determines which device caused the interrupt, and responds to the interrupt device. The response may be to take a character from the device, or to send a character to the device, as in the case of the communications interface.

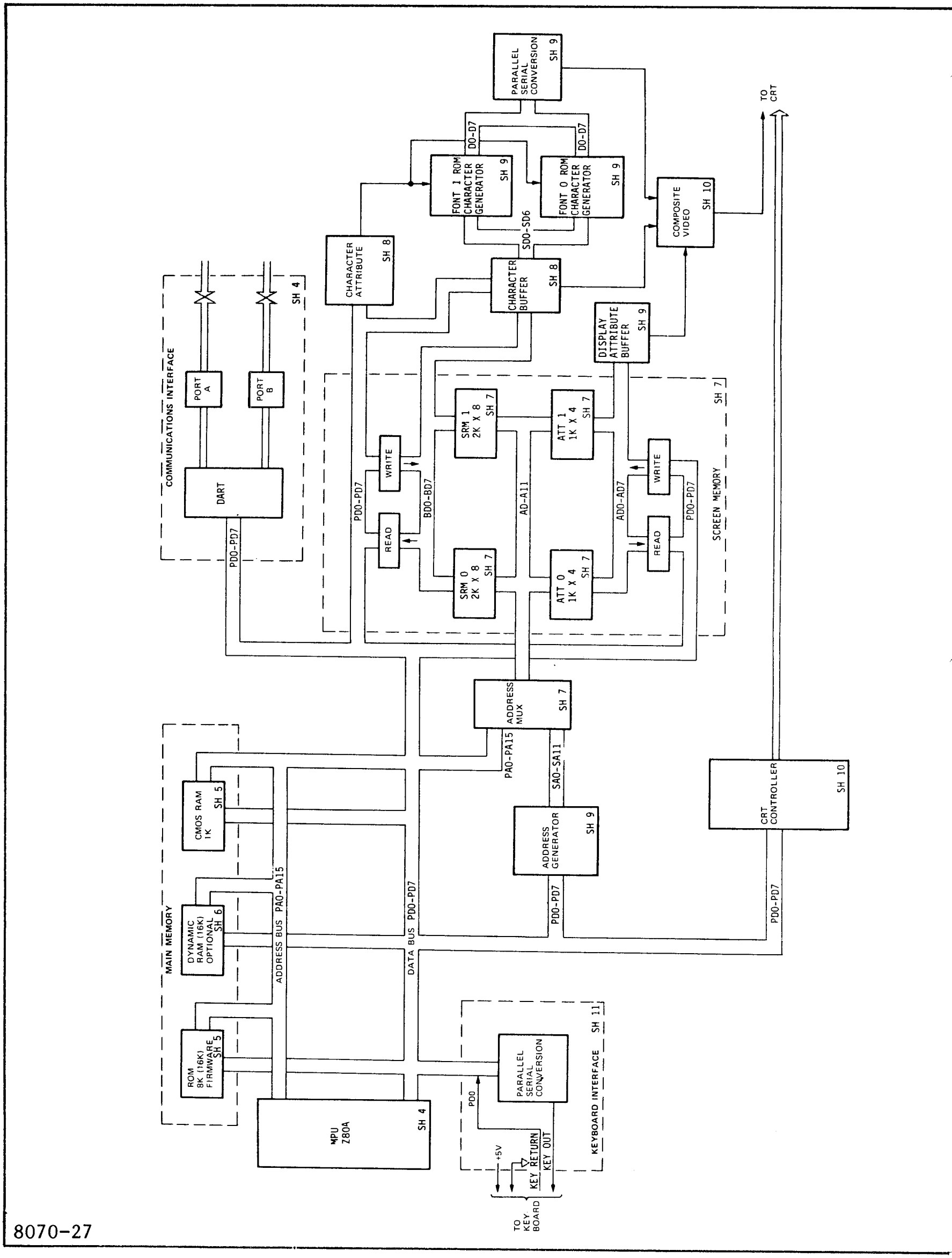


Figure 3-3. Block Diagram, Main Logic Board

3.4.2 Main Memory

Main memory, as distinguished from screen memory, consists of the operating system program, stored in 8K of ROM, the data memory provided by 2K of CMOS Random Access Memory (RAM) and the optional 16K dynamic RAM, which expands data memory to 19K. The term K normally expresses 1000 decimal, but in binary notation is equivalent to 1024 decimal.

Information can only be read from ROM, whereas information can both be written into and read from RAM and can therefore be changed, as is the case with screen memory.

Any logic device on the data bus, other than main memory or display memory, is addressed as an Input/Output (I/O) device.

3.4.3 Screen Memory

Screen memory, as described in paragraph 3.2 and as shown in figure 3-3, consists of two segments. Each segment comprises 1K of display information and 1K of attribute information for a total of 2048 storage locations. The screen memory consists of RAM elements and therefore can be written into and read from.

Screen memory is the storage for character codes that eventually are generated into the characters which appear on the screen. The MPU receives character-coded data from either the communications interface or the keyboard and writes the data into screen memory. From screen memory the data is displayed on the screen. The coded data remains in screen memory until it is overwritten by new or fresh data, or it may be transferred to the data segment of main memory.

Once the information has been displayed on the screen, that same information must continue to be displayed until it is altered or is performed automatically by screen memory. The address generator generates a series of screen memory addresses in sequence, reading the information (character code and attribute) and effectively displaying it from position 0 to position 1919. Refreshing occurs periodically, as determined by the MPU, so that displayed information appears to be steady. The address multiplexer is controlled to select either the screen memory address generated by the MPU or the refresh address from the address generator.

The CRT controller is pre-programmed by the MPU according to the display format and the chacter format, and it determines the generation of horizontal and vertical sync pulses. Note that the MPU has access to the address generator via the data bus; this allows the MPU to load the address generator with a binary number, corresponding to any character position in the display matrix (screen memory address).

3.4.4 Character Generation

The character generators, generator 1 and generator 2, provide the character code that is displayed on the screen. Each generator consists of a 2K ROM, which functions as a reference table. The ROMs store all the character codes in the character repertoire, in all of the possible dimensions from single height/single width to double height/double width.

A particular location in ROM is addressed in part by the coded data read from screen memory. The remaining location data is from information generated by the character control logic. The character control logic is itself controlled by the MPU and determines character dimension and brightness.

The character code (8 bits) is read from one of the character generators in parallel and then converted to serial data and fed into the composite video circuit. Other inputs to the composite video circuit are derived from the display attribute logic and the character control logic.

The display attribute logic determines the manner in which each character is displayed, as determined by the attribute segment of screen memory. The character contorl logic converts a binary number (digital) into an analog voltage (D/A coversion) and uses the analog voltage to control amplification of the video signal (brightness) in the composite video circuit.

3.4.5 CRT Controller

The CRT controller provides the control interface between the MPU and the CRT display. The CRT controller generates the vertical sync and horizontal sync pulses. Time positioning of both sync pulses and the respective pulse widths are controlled (programmable) by the MPU. The cursor signal, also generated by the controller, is used to indicate when the scan coincides with the cursor position.

The DISPLAY signal (display enable) is used to indicate when the controller is generating active display information, and is synchronized by the control logic to signify the beginning of a character row. The DISPLAY signal is inactive during horizontal and vertical flyback periods.

The screen memory refresh "test" address is generated by the CRT controller; the start address is programmable and the end address is determined by the size of the display matrix, i.e., the number of characters in a row and the number of rows in a frame. The MPU informs the controller as to the size of the display; the display size is one of the programmable features of the controller.

The MPU can read the status of the controller by addressing the controller and performing a read operation from the controller.

3.4.6 Keyboard Interface

The MPU scans the keyboard by polling each key position in the keyboard matrix to determine if the particular key has been pressed. The keys are arranged in an 8 X 10 matrix; this is a functional, not a physical, arrary.

The keyboard interface converts an 8-bit matrix code (matrix address) into serial data and sends it to the keyboard logic. The keyboard re-converts the serial data back to 8-bit code. The 8-bit code is used to select a column and row in the matrix and thereby select a particular key position. When a key has been pressed, a voltage is induced in the key's auto transformer. The induced voltage is detected by the matrix output circuit (latch). The output circuit is connected to the interface circuit in the main logic board and the signal is sampled by the MPU to determine if the particular key had been pressed. Note that the key does not initiate transmission of a code to the MPU; it merely signifies "pressed" or "not pressed."

When a key has been pressed, the MPU is aware of which key it was by means of the matrix code. The MPU then generates the code from a look-up table. If the key was a control key, such as the SHIFT key, the MPU reads the corresponding character code from the look-up table and writes that code into its screen memory. The subtlety of keeping track of the cursor is a function of the firmware by having the MPU interrogate the CRT controller.

3.4.7 Communication Interface

The communications interface consists of a Dual Asynchronous Receiver Transmitter (DART) and two Input/Output ports. The DART is programmed from the MPU, which determines line protocol, character format, number of stop bits and whether or not a parity bit is used, and if so, whether odd or even parity is enabled. One of the ports can be transmitting while the other is receiving.

One of the I/O ports is usually connected via a communications line to a host computer. The other port is usually connected to an output device, such as a printer, which can provide hard copy of displayed data. However, the second port may be connected to any device which interfaces to a communications line.

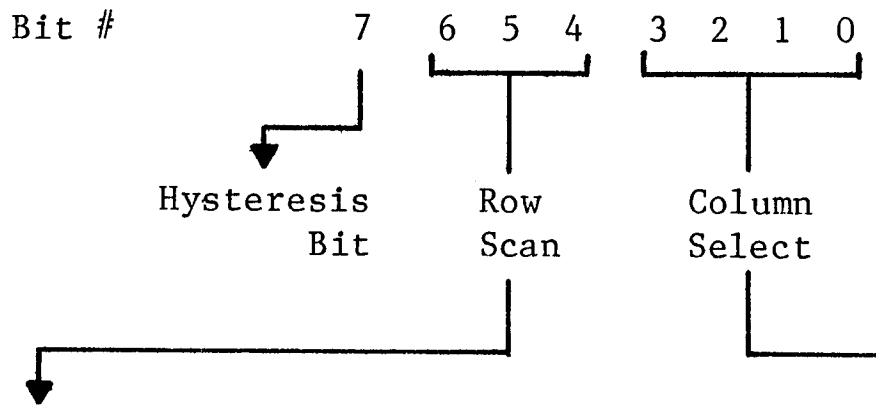
The DART receives data from each line serially. It assembles a character and interrupts the MPU to signify that a character is available. The MPU in turn relieves the DART of the character, which is then free to receive a subsequent character. The DART verifies the received character according to the format in use and logs any errors in a status register, which is accessible by the MPU. The MPU verifies that reception is error-free before processing the character. If errors are detected, the MPU can wait until the port goes idle and then ask the transmitting device (usually the host) to retransmit the message or information.

When the terminal has data from transmission, the MPU places the first character into the transmit buffer of one port in the DART and the DART transmits a formatted character down the line, bit by bit. On completion of character transmission, the DART interrupts the MPU to request replenishing the transmit buffer, and transmission continues. If the MPU is communicating with the host, it turns the port around and waits for a response. If the MPU is communicating to an output device, it interrogates the device by asking for the device status. In this way the MPU can determine if the information was received by the device and if the device malfunctioned.

3.5 KEYBOARD LOGIC

The keyboard logic is represented in block diagram form in figure 3-4. The keyboard is functionally arranged as an 8 X 10 matrix, as figure 3-4 shows. The keys are inductively coupled by means of an auto transformer to the output circuit. When a key is pressed, a magnetic core is inserted into the coupling such that if a current is flowing through the transformer, a current is induced in the pick-up winding. The induced current is detected as an induced voltage by the output circuit and registered (latched) as one bit. If a key has not been pressed, there is no induced voltage and a zero bit is registered by the output circuit.

The matrix code sent by the MPU to the keyboard, via the keyboard interface, consists of 8 bits as follows:



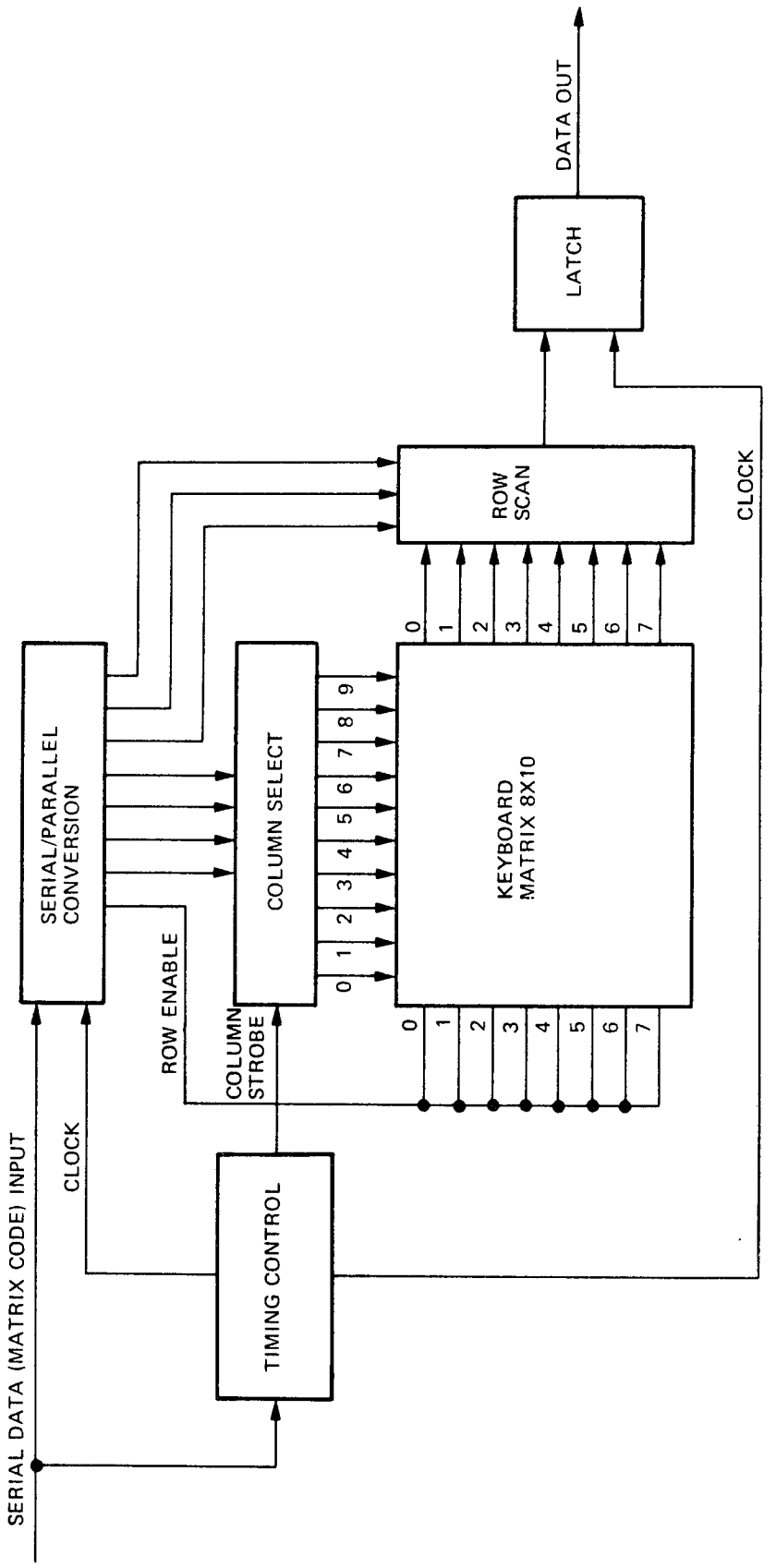
Row 0	0	0	0
Row 1	0	0	1
Row 2	0	1	0
Row 3	0	1	1
Row 4	1	0	0
Row 5	1	0	1
Row 6	1	1	0
Row 7	1	1	1

Column 0	0	0	0	0
Column 1	0	0	0	1
Column 2	0	0	1	0
Column 3	0	0	1	1
Column 4	0	1	0	0
Column 5	0	1	0	1
Column 6	0	1	1	0
Column 7	0	1	1	1
Column 8	1	0	0	0
Column 9	1	0	0	1

The matrix code is shifted into a serial/parallel converter. As each bit is being shifted in, a timing input is provided to the timing control logic, which generates the clock for the serial/parallel converter and the output latch. The timing logic also generates the column strobe, which occurs when all 8 bits of the matrix code have been shifted into the serial/parallel converter.

Bits 0, 1, 2, and 3 according to their binary-coded decimal significance, scan a particular column. Bits 4, 5, and 6, according to their binary significance, select a particular row. Bit 7 enables all the rows simultaneouly. Assuming the key with a matrix address 00 (row 0, column 0) has been pressed, then when row 0 was scanned by the row scanner a one bit would be detected. The hysteresis bit and column select signals energize the auto transformer at position 00, thereby enabling an induced voltage to be generated when the key is presssed.

A complete scan of all 80 positions in the matrix occurs within 12 milliseconds, which is considerably faster than an operator making successive key strokes.



8070-28

Figure 3-4. Block Diagram, Keyboard Logic

3.6 DETAILED LOGIC DESCRIPTION

3.6.1 Microprocessor Unit

The Microprocessor Unit (MPU) is a Zilog Z-80A. A block diagram of the MPU architecture is provided in figure 3-5. The pin-out table is given in table 3-1. Details of the internal functions of the MPU can be found in the Z-80A Component Data Catalog.

The MPU is shown on Sheet 4 of the Main Logic Board diagram in Section VI. The signal names and pin numbers are as shown and may be referenced to table 3-1 for functional descriptions.

Logic Diagram Sheet 4 shows that the address bus drivers (8C and 8E) are enabled by the inverse of -BUSAK, such that when -BUSAK is high the address bus drivers are enabled. The data bus driver 7E is bidirectional. One of the enables is tied to digital ground, the other is generated from 11G-6, being low for Read operations (PD7-PD0 to D7-D0) and high for write operations (D7-D0 to PD7-PD0). Since -BUSAK is considered high (-BUSREQ is tied to 5V), one permanent enable is provided to AND gate 11G-5. The remaining input is high when RD is low (write operation), when the counter timer (CTC) is enabled (-CTCE = 0), when the DART is enabled (-SIOE = 0), when Program Memory is selected (-PMSEL = 0), as in an instruction fetch.

The internal logic devices do not use the Bus Request input to the MPU (-BUSREQ). Consequently -BUSREQ remains high since it is tied to +5V and -BUSAK cannot be activated. However, the Bus Request and Bus Acknowledge signals are connected to the Expansion Connector J4, such that if an external device, for example a DMA Controller, were to share control of the buses, the signals would be activated accordingly.

A non-maskable interrupt (NMI) occurs when -NMI goes low (Sheet 9). This occurs at the start of each character line (raster line), when so enabled by the MPU (LINTEN=1=line interrupt enable). It is inhibited during the frame flyback period (retrace) by VSYNC and when the line scan counter overflows, i.e., when it produces a ripple carry output.

The MPU is interrupted (-INT goes low) by either the CTC (5C) or the DART (4C). Both devices are shown on schematic Sheet 1. The interrupt priority is determined by the daisy chain configuration. In this case the CTC has higher priority, since it is the first device to have its Interrupt Enable In (IEI) line tied to +5 volts. In turn, its Interrupt Enable Out (IEO) line provides the IEI line to the DART, which is the next lower priority device. The DART IEO line is routed to the expansion connector J4 (Sheet 12).

When an interrupt condition occurs in the CTC, its -INT output goes low and its IEO line goes low, preventing the DART from generating an interrupt.

The MPU samples the -INT input at the end of each instruction cycle. If -INT is low, the MPU acknowledges the interrupt during the next M1 cycle by forcing -IORQ low at the same time as -M1 is low, in similar manner to an OP code fetch cycle except that -MREQ remains high.

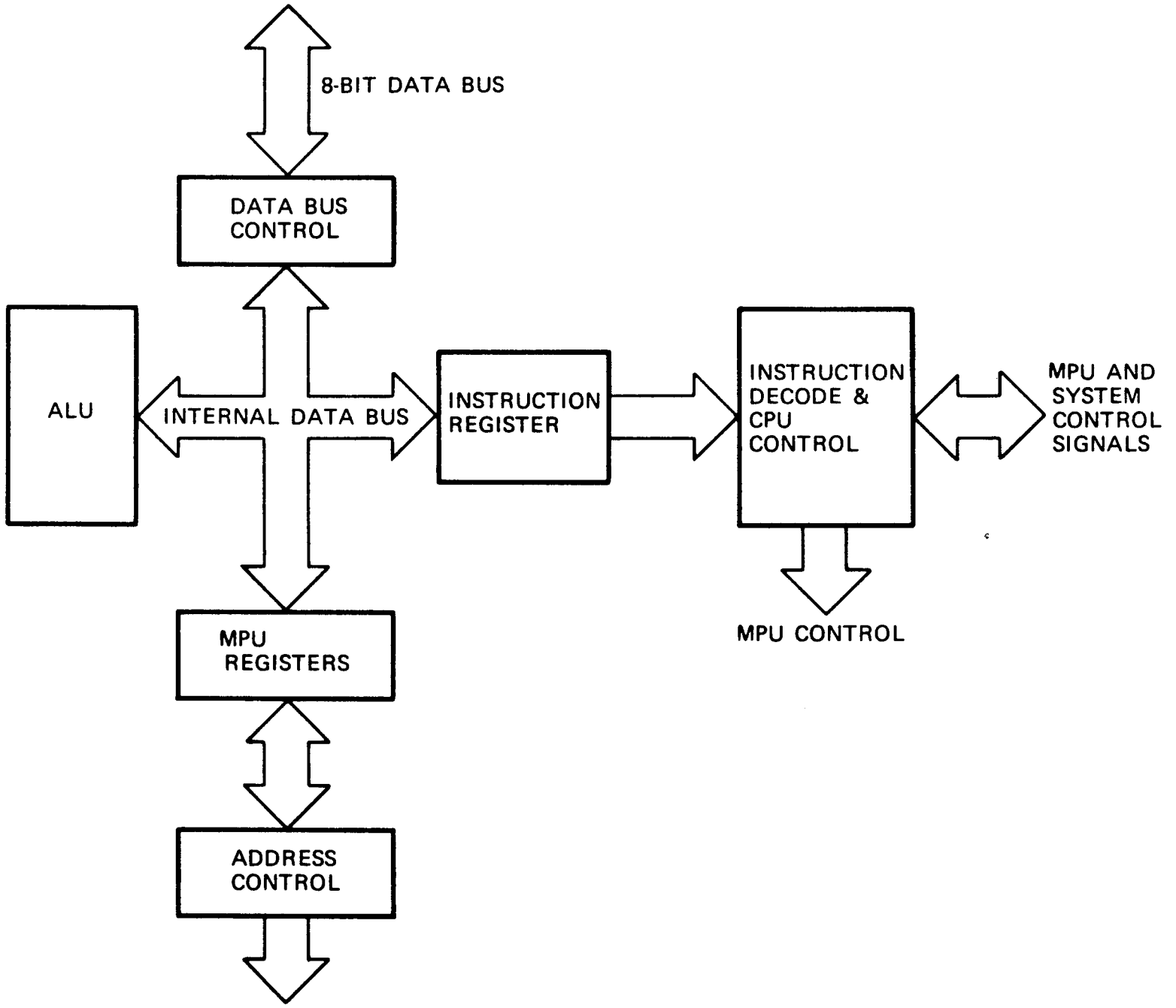


Figure 3-5. MPU Block Diagram

Table 3-1. MPU Pin-Outs

SIGNAL	CHARACTERISTICS
A0-A15 (Address Bus)	A0-A15 constitute a 16-bit address bus. The address bus is tri-state, active high. The bus provides the address for memory references (main memory) and the address for I/O data exchanges. A0 is the least significant address bit. I/O addressing uses the 8 lower address bits (A0 to A7). The lower address bits also contain a valid row address during memory refresh time used by dynamic memory.
D0-D7 (Data Bus)	D0-D7 constitute an 8-bit bidirectional data bus. The data bus is tri-state, active high. The data base is used for all data exchanges with main memory and all devices classified as I/O, which includes all logic devices served by the data bus other than main memory and display memory.
M1 (Machine Cycle One)	Active low output, which signifies that the current machine cycle is the Op Code Fetch cycle of an instruction execution. -M1 also occurs with -IORQ to indicate an interrupt acknowledge cycle. During execution of 2-byte op-code -M1 is generated as each op-code byte is fetched from program memory.
MREQ (Memory Request)	Active low, tri-state output. -MREQ = low signifies that the address bus holds a valid address for main memory or screen memory.
IORQ (Input/ Output Request)	Active low, tri-state output. -IORQ = low, signifies that the lower half of the address bus (A0-A7) holds a valid I/O address for an I/O read or write operation. -IORQ is also generated with -M1 when an interrupt is being acknowledged, to signify that an interrupt response vector can be placed on the data bus. Acknowledge operations occur during M1 time, while I/O operations never occur during M1 time.
RD (Memory Read)	Active low, tri-state output. -RD = low signals that the CPU wants to read data from memory or an I/O device. -RD is used to enable the transfer of data from the addressed memory or I/O onto the data bus.
WR (Memory Write)	Active low, tri-state output. -WR = low signifies that the data bus holds valid data to be stored in memory or transferred to the device.
-RFSH (Refresh)	Active low output. -RFSH = low signifies that the lower address bits (A0-A7) hold a refresh address for dynamic memories and that the current -MREQ = low signal is to be used to perform a refresh read to such memories.

Table 3-1. MPU Pin-Outs (continued)

SIGNAL	CHARACTERISTICS
-HALT (Halt State)	Active low output. -HALT = low signifies that the MPU has executed a halt instruction and is waiting for a non-maskable or maskable interrupt (with the mask enabled) before MPU operation can resume. While halted the MPU executes NOPs to maintain memory refresh activity.
-WAIT (Wait)	Active low input. -WAIT = low notifies the MPU that the addressed memory or I/O device is not ready for data transfer. The MPU will continually enter the wait state for as long as this signal is active. WAIT allows memory or I/O devices of any speed to be synchronized to the MPU.
-INT (Interrupt Request)	Active low input. The interrupt request signal is generated by the I/O devices. A request will be honored at the end of the current instruction, if interrupts are enabled and if the -BUSRQ signal is not active (high). When the MPU accepts the interrupt, an acknowledge signal (-IORQ during M1 time) is sent out at the beginning of the next instruction cycle.
-NMI (Non-Maskable Interrupt)	Negative edge triggered input. The non-maskable interrupt request line has higher priority than -INT and is always recognized at the end of the current instruction, even if the interrupt state is disabled. -NMI forces MPU to restart location 0066 (hex) in program memory. The program counter is saved, so that a return can be made to the program that was interrupted. Continuous WAIT cycles can prevent the current instruction from ending. A bus request will override a non-maskable interrupt.
-RESET	Active low input. -RESET forces the program counter to zero and initializes the MPU. During reset time the address and data buses go to high impedance state and all control output signals go to the inactive state.
-BUSRQ (Bus Request)	Active low input. The bus request signal is used to request the MPU to relinquish control of the address bus, data bus, and output control signals, which go to the high impedance state as soon as the current machine cycle is terminated. When this occurs, other devices can control the buses.
-BUSAK (Bus Acknowledge)	Active low output. Bus acknowledge is used to notify the requesting device that the MPU has relinquished control of the address and data buses and the control signals. The external device is then free to use the buses.
-Ø	Single phase TTL level clock which requires only a 330 ohm pull-up resistor to +5V to meet all clock requirements.

When the interrupting device detects both -M1 and -IORQ low, it places the low order byte of a vector address on the immediate data bus inputs to the MPU (D7-D0). The high order byte of the vector address is held by the MPU in the I (Interrupt) register. Once this response has been made by the interrupting device, the MPU goes into the interrupt service routine. When the interrupting device has been serviced, it reactivates its IEO line.

The Reset input to the MPU is derived from the Power On Clear signal -POC. Logic Diagram Sheet 5 shows that -POC is generated from the RC circuit consisting of R3 and C71, configured as an integrator. When power is first applied C71 draws maximum current, such that -POC goes low. C71 then charges towards +12V, but is limited to 8.6V by Zenor diode CR4. The time constant determines how long -POC is low, but once C71 is charged -POC is high and the MPU reset condtion is removed.

3.6.2 Memory and I/O Address Decode

The memory address decode logic is shown on Logic Diagram Sheet 6, and the I/O address decode logic is shown on Sheet 3. The logic is quite simple and therefore does not warrant a block diagram.

In both cases the decode is effected by a 256-bit ROM, configured as 32 eight-bit words. The output of the ROM is determined by the 5 address inputs, which include conditional inputs.

3.6.2.1 Memory Address Decode

Memory, as a whole, consists of program memory, screen memory, data memory, and the addition of optional data memory - four memory segments in all, each of which is described in later paragraphs. Program memory can only be selected when -PMREQ is low (-MREQ from the MPU).

Logic Diagram Sheet 5 shows the Memory Address Decoder or Memory Select Rom as device 9C. The ROM enable is tied to digital ground so that the outputs are permanently enabled. The five-bit address is made up from -PMREQ and the four most significant bits from the MPU address bus. If -PMREQ is low program memory is selected; accordingly -PMSEL will be low (Program Memory Select) and one of the associated four select signals (-MSEL3, -MSEL4, -MSEL1, -MSEL0) will also be low. If -PMREQ is high, then a memory segment other than program memory is selected, as follows:

-XMSEL = Extra Memory (optional data memory)

-SMSEL = Screen Memory

-DMSEL = Data Memory

Note that the high order 4 bits of the MPU address specify memory when -PMREQ is low and the low order 8 bits specify an I/O device when -PIORQ is low. An I/O address cannot be specified in the high order 8 bits of the MPU address bus.

3.6.2.2 I/O Address Decode

A valid I/O address appears on the low order half of the address bus (PA7-PA0), when -PIORQ is low. -PIORQ and -PM1 are both low when the MPU acknowledges and interrupt, so to distinguish between an I/O operation and an interrupt acknowledge, PM1 must be high when -PIORQ is low to signify an I/O operation.

The I/O decode logic is shown on Logic Diagram Sheet 3. It consists essentially of the 256-bit ROM device 13D. As shown the output enable of the ROM (pin 15) is tied to digital ground, such that the outputs are permanently enabled. Only five of the data outputs are used, and not all of the 32 eight-bit locations are used, since the A4 address input must be low (zero bit) and the A1 address input must also be low (-IORQ=0) for the decode to be effective. This reduces the actual number of used locations to eight; however the use of a Rom is much more economical than using a complex gating structure employing multiplexers and decoders. The ROM is functionally labelled IOCE for I/O Chip Enable, which is true in all cases of the ROM outputs; each one is a chip enable of one degree or another, as follows:

-RDST - Read Status: It enables the bit configuration of DIP switch 6L onto the data bus in bit positions PD7-PD2 and as shown on Sheet 11 enables the KEYRET signal onto PD0 and the RETRACE signal onto PD1.

-CTCE - Counter Timer Circuit Enable: Provides the -CE input to the Z80A CTC (Sheet 4), when the MPU communicates with the device.

-SIOE - Serial I/O Enable: Provides the CE input to the Z80A DART (Sheet 4), which contains two serial I/O ports. The MPU activates -SIOE when it outputs configuration information to either port or transfers data to or from either port.

-CRTE - CRT Controller Enable: Provides the -CE input to the CRT Controller (Sheet 10) when the MPU communicates with the controller during transfers of control and status information.

-D01 - Unlabelled ROM Output: Provides one of three enables to the octal decoder 9D.

Note that the conditional requirements for effective decode are that -PM1 is high in conjunction with PA7, PA6, and PA5, i.e., the cycle is not an M1 cycle, and that -IORQ is low. That is, it is an I/O operation and not a MPU interrupt acknowledge.

The octal decoder 9D decodes the eight possible combinations of the three least significant address bits PA2, PA1, and PA0 during I/O Write operations as determined by -PIORQ and -PWR both being low. The significance of the decodes are as follows:

PA2	PA1	PA0		
0	0	0	-RST	Reset Row Attribute Registers and Line Attribute Registers (Sheet 9).
0	0	1	-KEYLD	Key Load enables transmission of key matrix code.
0	1	0	-LINELD	Line Load loads an 8-bit value into one of the Row Attribute registers.
0	1	1	-BRITLD	Brightness Load loads an 8-bit value into the Analog/Digital converter.
1	0	0	-LATTLD	Line Attribute Load loads an attribute value into registers 10E on Sheet 9.
1	0	1	-LSCNLD	Line Scan Load loads an 8-bit value into a second Row Attribute register, four bits of which are transferred to the line scan counter.
1	1	1		Not used.
1	1	1		Unlabelled Decode. Loads or clocks an 8-bit value into register 10D (Sheet 3).

Register 10D determines which of two banks in optional Data Memory is selected, whether 80 or 132 column display is selected, whether CTS is to be activated for certain communication protocols, and whether non-maskable line interrupts are to be enabled.

3.6.3 Main Memory

Main memory is shown on Logic Diagram Sheets 5 and 6, and consists of the following storage elements:

- Program Memory: consisting of four EPROMS, 1E, 2E, 3E and 4E.
- Data Memory: consisting of a single static RAM device 6E.
- Optional Data Memory: consisting of eight 16K X 1 bit dynamic RAMs, 4A 5A, 6A, 7A, 8A, 9A, 10A and 11A, configured as 16K X 8.

3.6.3.1 Program Memory

Program memory varies in size according to the required application. Four EPROMS are shown on the logic diagram (Sheet 5); each EPROM may be a 4K X 8 (2732) or 8K X 8 (2764), such that program memory may be 4K in total (one 2732) or 32K in total (4 - 2764s).

Thirteen address bits are used (A12-A0) to specify one of a possible 8K locations in one of four EPROMS, as selected by the individual address decodes -MSEL0, -MSEL1, -MSEL2, and -MSEL3, respectively, as described in paragraph 3.6.2.1. The Output Enable (-OE) input to each EPROM is derived from the Read signal (PRD) from the MPU. When -PRD is low an instruction is read from the addressed location in the selected EPROM and placed onto the direct data bus inputs to the MPU (D7-D0) and not PD7-PD0. The -WE input -PWR has no effect on either 4K or 8K EPROM devices.

3.6.3.2 Data Memory

Data Memory (6E) is selected by the address decode -DMSEL. As shown -DMSEL=0 is inverted by Hex inverter 1G to turn on transistor Q2, which then provides a logic low level to the -CE input.

The Output Enable (-OE) input is derived from the MPU Read output PRD. When PRD is low (Read) the contents of the addressed location are placed on the direct data inputs to the MPU (D7-D0) and not PD7-PD0. The Write Enable (WE) input is derived from the MPU Write output -PWR. When PWR is low (Write) the data appearing on the direct outputs from the MPU is written into the addressed location.

The memory device is a 4K X 8 RAM, with provision for future design to accommodate an 8K X 8 RAM.

3.6.3.3 Optional Data Memory

Optional Data memory, when installed, provides for the storage of up to 16K bytes of information. Information from the host may be temporarily stored and then transferred to the display screen, or information may be transferred into data memory from screen memory, then transferred to the host or a hardcopy device (printer).

This memory consists of eight 16K X 1 dynamic RAMS, configured as 16K X 8. The RAMS are connected in parallel so that the same single bit cell in each RAM is addressed simultaneously. The Data Input (DI) and Data Output (DO) are wire-ORed together and tied into the MPU data bus PD7-PD0.

To address 16K locations fourteen address bits are required, as specified by PA0-PA13 from the address bus (BANK0 and BANK1 are for future expansion of data memory to 64K). A RAM location is selected by first selecting a 7-bit row address, then by selecting a 7-bit column address. The determination to read from or write into the addressed location is made by the Write Enable (-WE) input, which is derived from RD (the inverse of -RD from the MPU). If RD is high a read operation takes place, and conversely a write operation takes place.

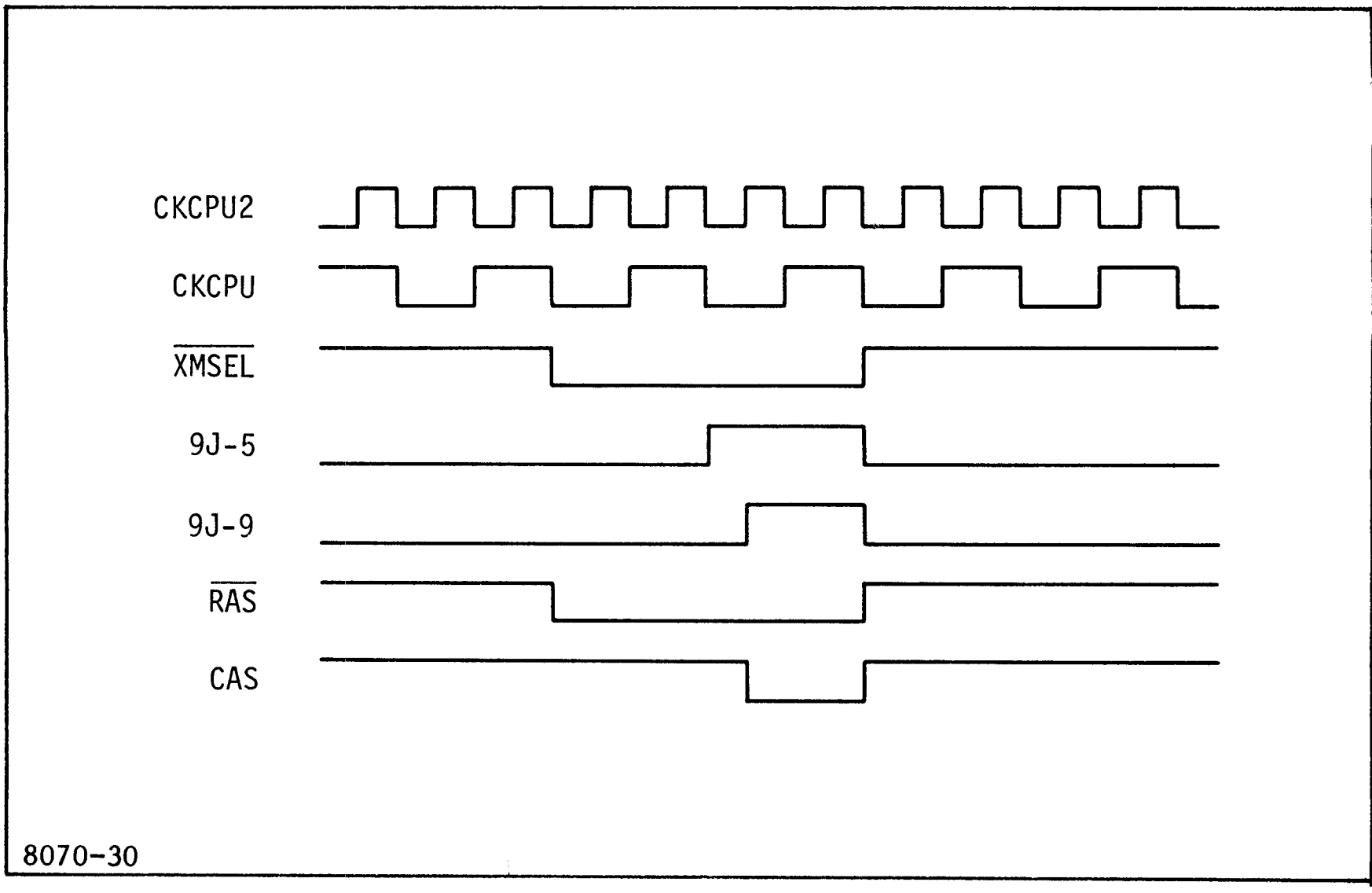


Figure 3-6. Dynamic RAM Row/Column Address Sequence

A0-A6 select the row and A7-A13 selection the column. The timing sequence is determined by two D-type flip-flops 9J, and the row and column addresses are selected by multiplexers 5B and 8B. The timing is shown in figure 3-6, which depicts normal access timing (-PRFSH is assumed to be high).

Prior to selection of Optional Data Memory, -XMSEL is high and its inverse holds both flip-flops in the clear state (reset). When -XMSEL goes low the first flip-flop is primed for the set state, which occurs at the leading edge of the next CKCPU clock as shown. The second flip-flop clocked set at the leading edge of the next CKCPU2 clock. When -XMSEL goes high, its inverse clears both flip-flops and they are held in that state until -XMSEL goes low again.

When the first flip-flop is in the reset state the A inputs to multiplexers 5B and 8B appear as A0-A6, the address inputs to data memory. When -XMSEL goes low, -RAS goes low and A0-A6 represent the row address. When the first flip-flop is clocked, set the B inputs to the multiplexers appear as A0-A6 to become the column address when the second flip-flop is clocked set and -CAS is activated. As stated both flip-flops are cleared and the sequence ends when XMSEL goes high.

During a memory refresh cycle, the MPU activates -PMREQ and -PRFSH and places a refresh address on PA6-PA0. -XMSEL is not activated, so that the two flip-flops are held in the reset state. Since the first flip-flop is held reset, the A inputs to the multiplexers (the refresh address) appears as A6-A0. -PRFSH and -PMREQ activate -RAS while -CAS cannot be activated. In other words, only the row address is generated during a memory refresh cycle.

3.6.4 System Clock Generation

The system clock generator is shown on Logic Diagram Sheet 3. It consists of a crystal oscillator 5G, a 4-bit binary counter 5J, two quad 2-1 line multiplexers 7J and 8J, and associated gates. Also shown is the optional 132-column clock generator and its associated counter 6J. In the following description, 80-column display operation is assumed (-WID80=low) and the character clock is for normal width characters (DBLW=low), so that the multiplexers select the A inputs. The timing relationship is shown in figure 3-7.

The oscillator output is counted down to provide CKCPU2 at 7.3728 MHz, CKCPU at 3.6864 MHz, CKC80 at 1.8432 MHz and CKCTC at 921.6 KHz. CKCPU provides the phase clock input to the MPU and is selected by multiplexer 7J to appear as CKD3. The multiplexer also selects CKCPU2 to appear as CKD2 and CKC80 to appear as SMCYC (Screen Memory Cycle). Both multiplexers 7J and 8J select the oscillator output to appear as -DOTCLK (the inverse of Dot Clock). Multiplexer 8J selects SMCYC, which is inverted to provide CHRCLK (Character Clock), and also selects CKD3 and CKD2. The output of Nand gate 9F generates -CHRLD (Character Load), which is effectively the inverse of every fourth CKCPU2 clock, and occurs once during every eighth dot clock period. Other principal timing sequences are discussed when the associated logic operation is described.

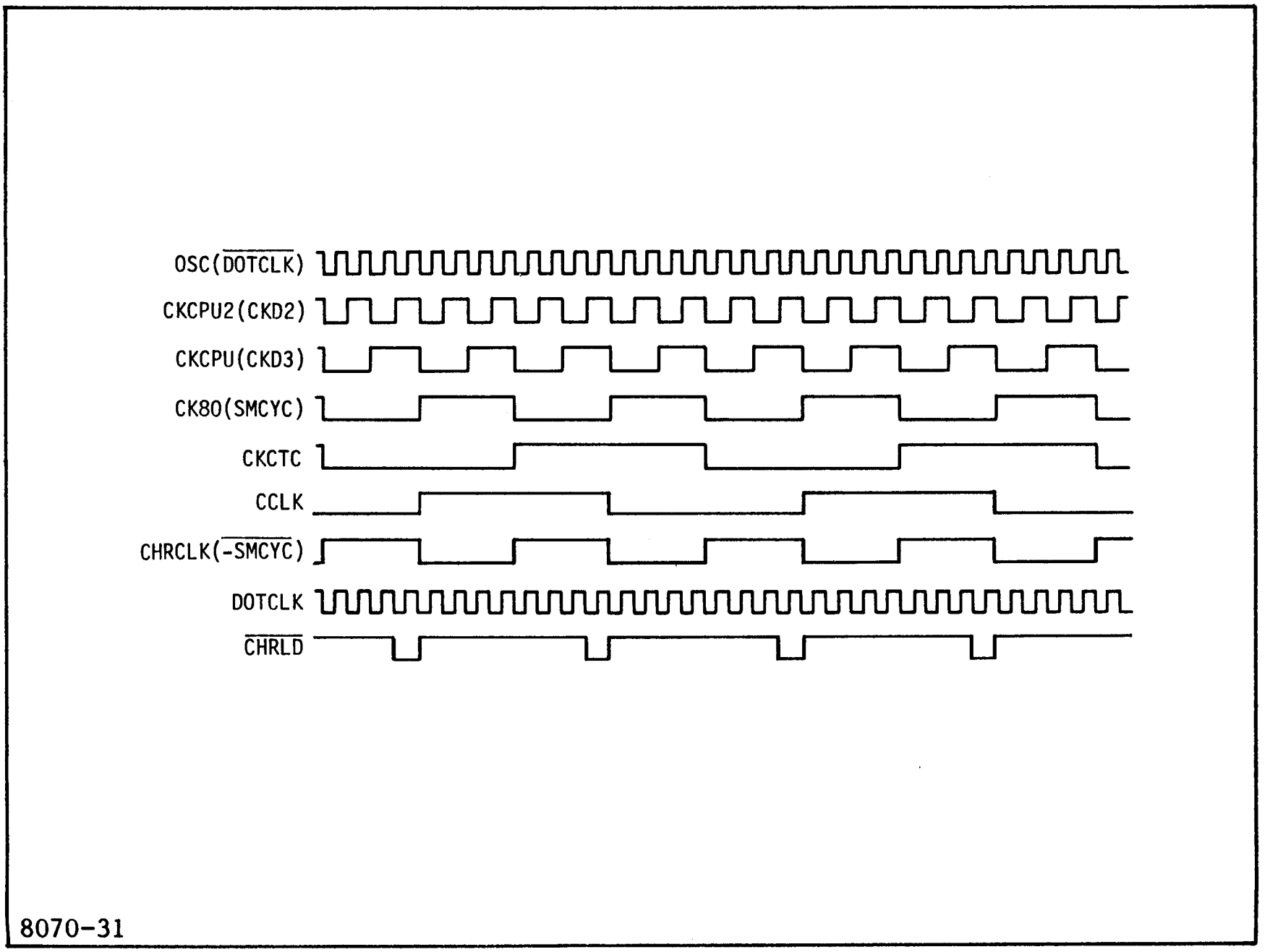


Figure 3-7. Clock Timing - Dot Clock Timing Clock and Character Load

3.6.5 Screen Memory

Screen Memory is shown on Logic Diagram Sheet 7 and is shown in block diagram form in figure 3-8. It is functionally divided into two segments - data and attribute. To accommodate a display matrix of 132 X 24 (3,168 characters) a 4K data memory and a corresponding 4K attribute memory is required in the formaton of screen memory.

Each memory segment is divided in half. One half corresponds to the upper half of the display screen, and the other half corresponds to the lower half of the display screen. In the block diagram the two halves are identified as SRM0 (data) and ATT0 (attribute) corresponding to the upper half and SRM1 (data) and ATT1 (attribute) corresponding to the lower half. The memory devices are 2K X 8 RAMs, four of which are required - two for data storage and two for attribute storage. One data and one attribute RAM are assigned to the upper half of the screen and the remaining two are assigned to the lower half of the screen.

Twelve address bits (A0-A11) are required to address 4K memory locations. The twelfth bit (A11) is a pointer to either the upper or lower 2K of screen memory and is used in combination with other signals to generate the appropriate chip enable (CE) input to the addressed RAM. Since each RAM is 2K X 8, only 11 address bits (A0-A10) are needed to address a particular location in the enabled RAM.

Character coded information is written into screen memory by the MPU. The information may be derived when the MPU interrogates the keyboard matrix, or it may be received from the communications interface by way of data memory (optional data memory).

Character coded information is read from Screen Memory by either the MPU, or automatically by the control logic during a screen refresh operation. The MPU reads the information to effect its transfer to (a) the host computer via the communications interface (b) optional data memory for temporary storage (c) a peripheral device, such as a printer, via the communications interface.

A screen refresh operation does not occur in one full scan of the screen to the exclusion of MPU operations into or out of screen memory. The operations are time shared under the control of the arbitration logic, which gives precedence to the MPU. The MPU addresses screen data memory and attribute memory separately, while during a screen refresh they are addressed simultaneously.

The control logic generates the chip enable signals and the read/write control signals.

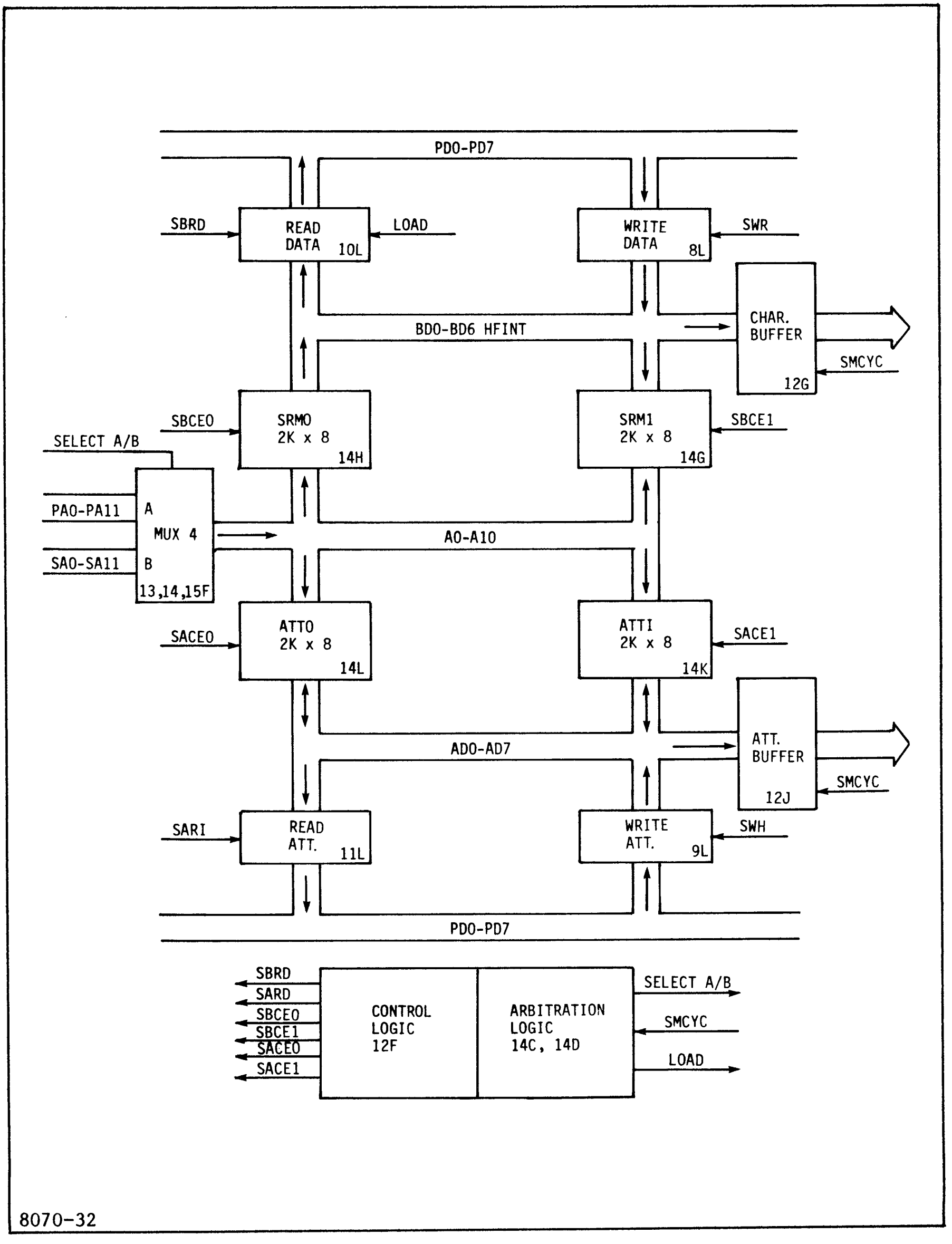


Figure 3-8. Block Diagram - Screen Memory

3.6.5.1 Control Logic

The control logic functions are performed by 32 X 8 ROM (12F), whose outputs are determined by the state of the address bits. -SMSEL determines if the MPU is addressing screen memory, such that if -SMSEL is low a screen refresh is taking place. Since the MPU may write into and read from screen memory, -PRD is used to determine the flow of information and will also determne the state of -SWR. PA12 and A11 determine which one of the four 2K RAMs is being addressed. The significance of the control ROM outputs is as follows:

Pin 5: -SBRD = Screen Buffer Read (data)
Pin 4: -SARD = Screen Attribute Read
Pin 3: -SBCE0 = Screen Buffer Chip Enable Zero
Pin 2: -SBCE1 = Screen Buffer Chip Enable One
Pin 1: -SACE0 = Screen Attribute Chip Enable Zero
Pin 9: -SACE1 = Screen Attribute Chip Enable One
Pin 6: -low = Write (high output = read)

Note that the ROM is represented functionally as a gating structure to give the reader some idea as to the content of the addressed location.

3.6.5.2 Arbitration Logic

The Arbitration Logic consists of the dual J-K flip-flop 14C and various gates, 14D and 11G. The logic gives priority to the MPU for access to screen memory; if the MPU is not addressing Screen Memory, then a screen refresh operation is automatically taking place.

The timing sequence is shown in figure 3-9 with respect to a MPU memory reference operation. When the address specifies screen memory, SMSEL goes high and the first of the two flip-flops 14C is clocked into the set state. If 132 columns are specified (-WID80 = 1), a Wait condition is imposed (SMWAIT = 1) and a wait period is inserted between T1 and T2. Then when -SMCYC goes low, the second flip-flop is clocked set. If 80 columns are specified, the second flip-flop is preset when -SMCYC goes low. In either case, 14C-7 goes low to select the A inputs to the Address Multiplexer (13F, 14F, 15F) and the MPU address lines select a memory location. At the same time the first flip-flop is cleared and registers 10L and 11L are clocked to load in the data read from the selected location. In the case of a Write operation, -SWR is activated by the control ROM and information on the Data Bus (PD7-PD0) is written into the selected location.

When SMCYC goes low, the second flip-flop is cleared and MPU access operation terminates.

The default condition is with both flip-flops cleared, in which case, screen memory is addressed from the outputs of the Address Generator (SA11-SA0). The -Q output of the second flip-flop is now high and remains high until the MPU selects Screen Memory again. In this condition -SWR cannot be generated, since the control ROM does not activate a write enable (pin 6 = low). During screen refresh operations only read cycles are enabled. When SMCYC goes high, the information read from the addressed location is clocked into buffer registers 12G and 12J.

Both data and attribute memory are read simultaneously during a refresh operation, such that SBCE0 and SACE0 or SBCE1 and SACE1 are activated by the control logic. SMCYC loads the data and attribute information into the two registers 12G and 12J.

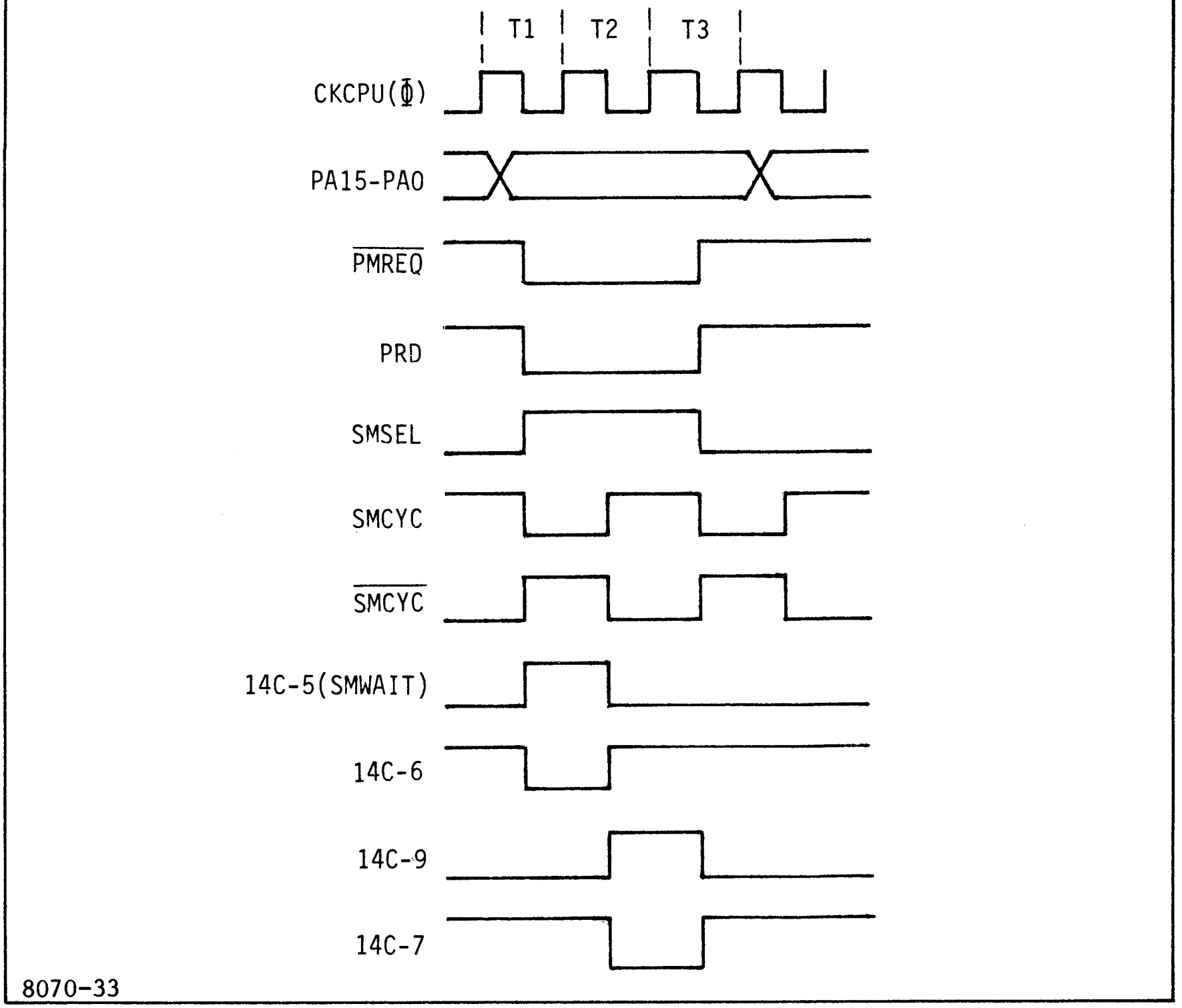


Figure 3-9. Screen Memory Arbitration Logic - MPU Access Timing

3.6.6 CRT Controller

The CRT Controller (CRTC) is a Model 6845 CRTC manufactured by Motorola. The pin-out list is provided in table 3-2, and the CRTC is shown on Logic Diagram Sheet 10.

The CRTC is used in a limited operational capability in the EVDT, in that only some of the functions are used. Unused functions are not discussed in the following paragraphs.

Table 3-2. CRT Controller Pin-Outs

PIN	SIGNAL	DESCRIPTION/FUNCTION
1	GND	Ground
2	-RESET	Active low input used to initialize all internal scan counter circuits. When -RESET is low, all internal counters are stopped and cleared, all scan and video outputs go to the low state; control registers are unaffected. All scan timing is initiated when -RESET goes high. -RESET can be used to synchronize display frame timing with line frequency.
3	LPSTB	Light Pen Strobe - not used.
4-17	MA0-MA13	Memory Address Lines - not used.
18	DISP	Display Enable. Active high output used to indicate when the controller is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters is programmable and are used to generate the DISPLAY signal.
19	CURSOR	Cursor Position - not used.
20	V_{cc}	+5V input.
21	CLK	Timing Clock. Used as the time base for all internal count/control functions.
22	R/$\overline{W}$	Read/Write Control. Derived from A1 (address bus), when -CRTE is low. When this bit is logic one the requested information is placed on the MPU data bus by the controller in the execution of a read operation. When this bit is logic zero, the information on the MPU data bus is written into the selected internal register.
23	E	Enable. Active positive going transition, which triggers all data transfers between the MPU and the data controller. Active when both -IORQ and -CRTE are low.
24	RS	Register Select. Used to access internal registers. Derived from A0 (address bus) when CRT SEL is low. When A0 is low (RS = low) writes are permitted into the address register and the status register. The contents of the address register is the identity of the register accessed when RS is high.
25	-CE	Chip Enable. The CRTC is enabled when the CE input is low, which is the case when -CRTE is low from I/O address decode.

Table 3-2. CRT Controller Pin-Outs (continued)

PIN	SIGNAL	DESCRIPTION/FUNCTION
26-33	D7-D0	Data Bus. The D7-D0 pins are the eight data lines used for transfer of data between the MPU and CRTC. D7-D0 correspond to PD7-PD0.
34-38	RA4-RA0	Raster Address Lines - not used.
39	HSYNC	Horizontal Sync. Active high output (pulse) used to determine the horizontal position of displayed text. HSYNC time, position, and width are fully programmable.
40	VSYNC	Vertical Sync. Active high output (pulse) used to determine the vertical position of displayed text. VSYNC position and width are fully programmable.

3.6.6.1 CRTC Internal Registers

There are eighteen registers in the CRTC (R0-R17), accessible to the MPU, that is, they may be written into and read from and are therefore defined as programmable. The address register is excluded from the eighteen registers because of its special function. Of the remaining registers only R0-R7 are used. The following text briefly describes the function of each utilized register.

Address Register - This is a 5-bit register used as a source/destination reference to direct transfers between the MPU and CRTC. When RS is low, this register may be loaded; when RS is high, then the internal register selected is the one whose binary identity (00000-00111) is stored in this register.

R0 - Horizontal Total (00000) - This 8-bit register contains the total number of characters, minus one, per horizontal line. The total is the sum of displayed and non-displayed characters as depicted in figure 3-10. The frequency of HSYNC is thus determined by this register.

R1 - Horizontal Displayed (00001) - This 8-bit register contains the number of displayed characters per horizontal line (reference figure 3-10), which in the case of the EVDT is 80 single-width characters, or 130 characters (option).

R2 - Horizontal Sync Position (00010) - This 8-bit register contains the position of HSYNC on the horizontal line, in terms of character location number on the line. The position of HSYNC determines the left-to-right location of the displayed text on the screen as a means of adjusting the side margins.

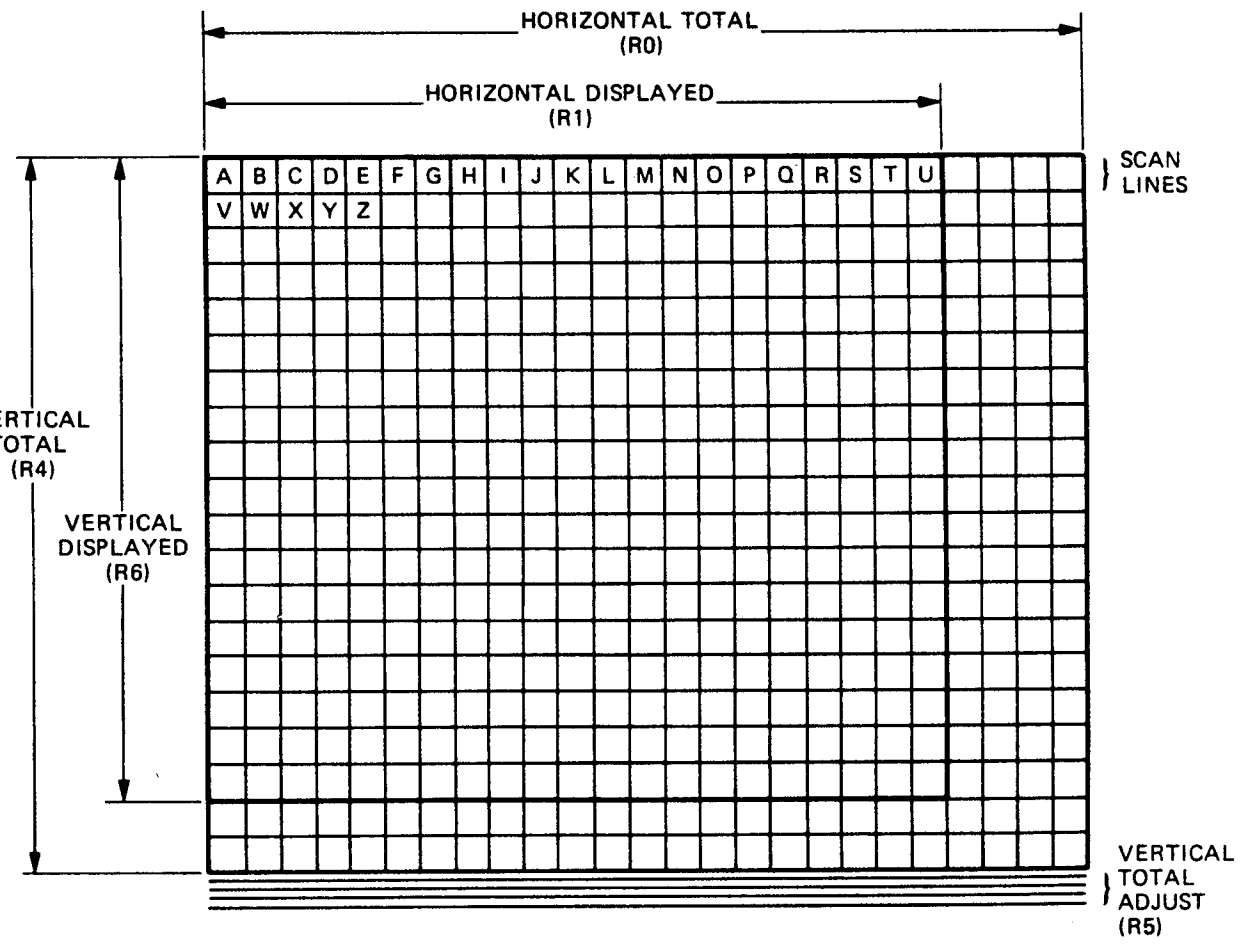
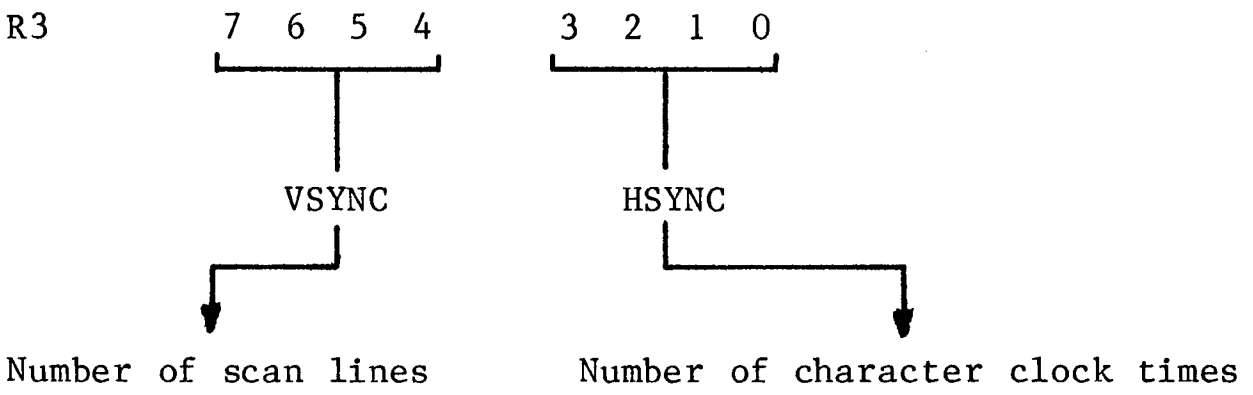


Figure 3-10. Typical Video Display Format

R3 - Horizontal and Vertical SYNC Widths (00011) - This 8-bit register contains the widths of both HSYNC and VSYNC as follows:



VSYNC, being a wider pulse, is expressed as being as wide as the time it takes to complete N horizontal scans. HSYNC, which occurs once for each character row, is of much shorter duration and its width is expressed as the duration of N character clock periods.

R4 - Vertical Total (00100) - The vertical total register is a 7-bit register containing the total number of character rows, minus one, in the display matrix (figure 3-10). This register, in conjunction with R5, determines the overall frame rate, which is usually close to the line frequency to ensure flicker-free appearance.

R5 - Vertical Total Adjust (00101) - This is a 5-bit, write-only register containing the additonal number of scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time (figure 3-10).

R6 - Vertical Displayed (00110) - This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

R7 - Vertical Sync Position (00111) - This 7-bit register is used to select the character row time at which VSYNC is to occur, and is thus used to position the displayed text in the vertical direction (top margin).

3.6.6.2 Vertical and Horizontal Timing

The vertical and horizontal timing relationship is shown in figure 3-11. The timing is not drawn to scale and the frame does not reflect the actual dimensions of the display matrix. The timing diagram is intended as an aid to understanding the internal clocking and synchronization of the HSYNC and VSYNC pulse outputs.

Although the raster line outputs RA0-RA4 are shown in relationship to scan line generation, they are not used. The number of scan lines per character row is a function of the character generator cirucits, and is discussed in later text.

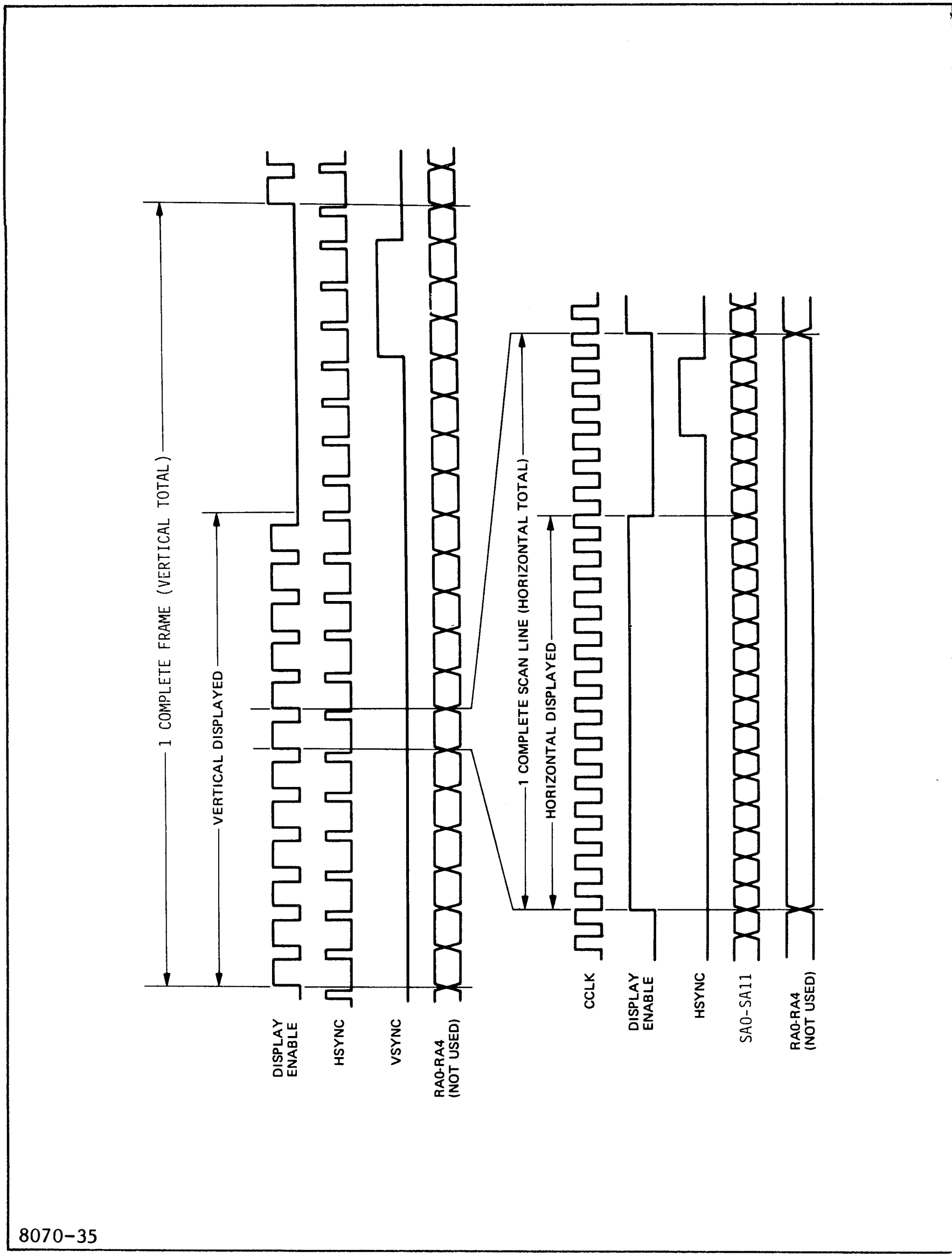


Figure 3-11. Vertical and Horizontal Timing Relationship

3.6.7 Refresh Address Generation

The refresh address generation circuit is shown on Logic Diagram Sheet 9. It consists of the individual binary counters 13E, 15E and 14E, and buffer registers 10C, 15C, 11D and half of 11E.

The counters 13G, 15E and 14E are connected in series to form a 12-bit counter, whose outputs SA0-SA11 represent a 12-bit screen memory address. The counter has a count cycle of 4096 counts, corresponding to 4096 RAM locations in screen memory (to accommodate 3120 characters and the associated attributes for a 130 X 24 display matrix). SA11 points to the upper or lower half of the display and SA0-SA10 (11 bits) select one of 2K locations.

The counter is clocked by CHRCLK, which, as shown in figure 3-7, provides a positive going transition once in every 8 dot clock periods, i.e., every time a character row is scanned and when the next character row is to be displayed. The two most significant stages of the counter (15E and 14E) are parallel loaded from buffer register 15C on the trailing edge of -ROWLD. As shown on Sheet 10, -ROWLD is derived from the Attribute Control Register 11J and represents the state of the DISP signal from the CRTC, sampled at the SMCYC clock rate delayed one SMCYC clock period from ROWCLK, which represents the state of DISP as sampled at the SMCYC clock rate. This simply means that ROWCLK and -ROWLD are generated in synchronization with HSYNC to denote the start of a new horizontal scan (see figure 3-11). The least significant stage of the counter is parallel loaded from one half of buffer register 11E coincident with ROWCLK.

The buffers, 10C, 1D, 15E, 11E, and 10E are octal D-type flip-flops. Buffer 10C is loaded from the MPU data bus when the I/O address decode -LINELD is activated. This correctly implies that the screen refresh starting address can be controlled by the MPU and that refreshing can occur from any physical location in screen memory and not necessarily from the first character position. Similarly, buffer 11D is parallel loaded from the data bus when the I/O decode -LSCND is activated.

The information in buffers 10C and 11D is transferred to buffer 15C (from 10C) and to one half of 11E and counter 11C (from 11D) coincient with the end of the last or bottom line of the character row. This synchronization is derived from the output of gate 4B pin 13, occurring when a carry output is generated by counter 11C, which in effect counts the horizontal lines in a character row. It also occurs at the end of the VSYNC period to denote the first character row of a new frame. Note that when so enabled by the MPU (LINTEN=1), the foregoing conditions generate a non-maskable interrupt (-NMI=0). The interrupt service routine initiates the loading of the buffer registers.

Counter 11C is clocked by ROWCK, which is derived from the Xor output 2G-11. ROWCK is coincident with -ROWLD, but is not generated during the vertical flyback period as signified when VSYNC is low. When VSYNC is high, -ROWLD is gated through Xor gate 2G as ROWCK. Note that ROWCK is not the same as ROWCLK.

3.6.8 Character Generation

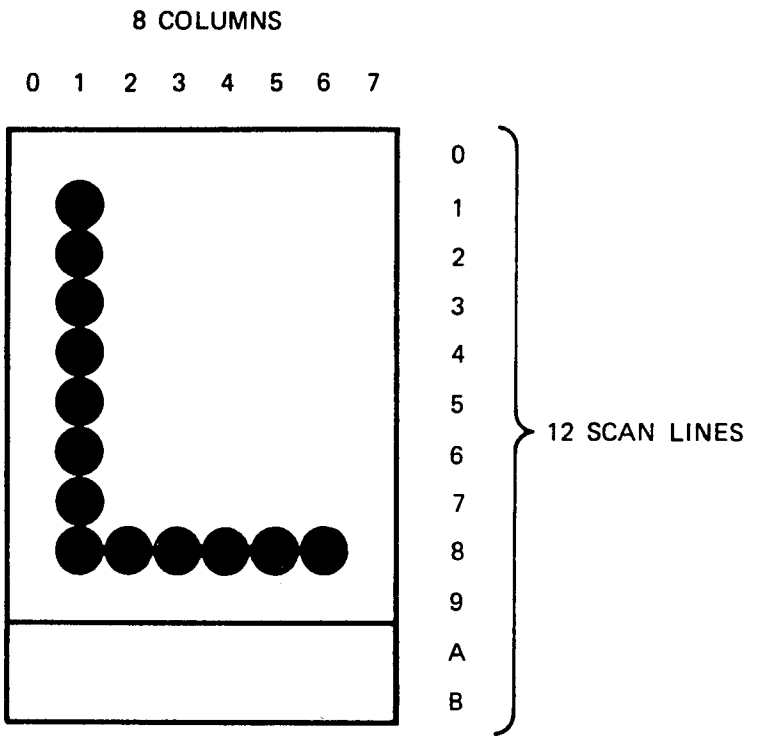
The character generation logic is shown on Logic Diagram Sheet 9. It consists of the following functional elements:

- Character Generator Font 0 (10G)
- Character Generator Font 1 (8G)
- Parallel-to-Serial Converter (7G)
- Character Line Scan Counter (10F)
- Line Attribute Buffer (one-half 11E)

Before discussing details of character generation, it is necessary to explain how a character is formed. Figure 3-12 depicts the generation of an upper case letter L. A character row occupies 12 scan lines. The lines are numbered 0-B (hexadecimal), which is equivalent to binary 0000-1011. It follows that a 4-bit binary counter will fulfill the requirement for counting character line scans. The line scan occurs across all 80 columns or one horizontal line scan. If the line scan counter is incremented at the beginning of each scan (or at the end of the previous scan), after 12 such scans, a complete character row will have been scanned. If the counter is re-initialized, the cycle will be repeated for the next character row and subsequent character rows, until vertical blanking takes place, at which time 24 character rows will have been displayed.

The character generator contains the data necessary to form a charcter on a line by line basis. This data is fed serially to CRT, so that as the scan passes a particular position in the character matrix the electron beam is intensified to illuminate that position, according to the character to be formed. The data is stored in the character generator as depicted in figure 3-12, example B.

The line scan number remains the same for one complete horizontal line scan. The data information changes for each character position as determined by the information supplied from screen memory.



A. DISPLAY MATRIX – UPPER CASE L.

```
00000000
01000000
01000000
01000000
01000000
01000000
01000000
01000000
01111110
00000000
```

B. CHARACTER ROM – UPPER CASE L

8070-36

Figure 3-12. Character Generation

3.6.8.1 Character Generators

The character generators 10G (Font 0) and 8G (Font 1) are 2K X 8 ROMs. The ROMs store the character information on a line basis. Font 0 provides all the standard letters (upper and lower case), the ten numerical digits, punctuation marks and symbols, while Font 1 provides foreign language letters and symbols, as well as special graphic symbols.

The address inputs to each ROM are derived from the outputs of the line scan counter (CA0-CA3) and from the outputs of the screen data buffer (SD0-SD6). Note that seven data bits are used, corresponding to 7-bit ASCII character code. The ROMs outputs are permanently enabled since the -OE pin is tied to digital ground. One or other of the ROMs is selected according to the logic state of Font 1 as follows:

Font 1 = 0 = select Font 0 ROM

Font 1 = 1 = select Font 1 ROM

The line scan counter bits CA0-CA3 are constant for the duration of a complete horizontal line scan, whereas the data bits SD0-SD6 from screen memory change eighty times during the same period, assuming the MPU is not accessing screen memory. As the ROM address changes, the new information appears at the ROM outputs, noting that the outputs of the ROMs are connected together on a bit-for-bit basis (OR connection). The information is transferred from the ROM outputs to the parallel-to-serial converter.

3.6.8.2 Parallel-To-Serial Conversion

The parallel data from the character generator (dot matrix code) is converted into a serial bit stream by the shift registers 7G and D-type flip-flop 4G.

The shift register is parallel loaded by -CWRLD = 0 coincident with the next -DOTCLK. When -CWRLD goes high, the register is enabled for shift operations, which ocur coincident with the positive going edge of -DOTCLK. The data bits are shifted out via pin 13 (Q). The serial input to the register is tied to ground, so that as data bit is shifted out, a zero bit is shifted out. The bits are shifted out in descending order, most significant first, least significant last, which happens to be the most significant output of the character generator (D7).

The output flip-flop 4G effectively inverts the data output from the shift register, noting that if the output is zero the flip-flop is immediately cleared and if the output is one the flip-flop is clocked into the set state one half clock period later by DOTCLK. This has the effect of elongating a one bit, which causes thickening of vertical character lines in keeping with the thickness of horizontal character lines. The timing data output is depicted in figure 3-13, for a dot matrix character consisting of alternate ones and zeros to emphasize the elongation of a one bit as it appears at VIDOUT.

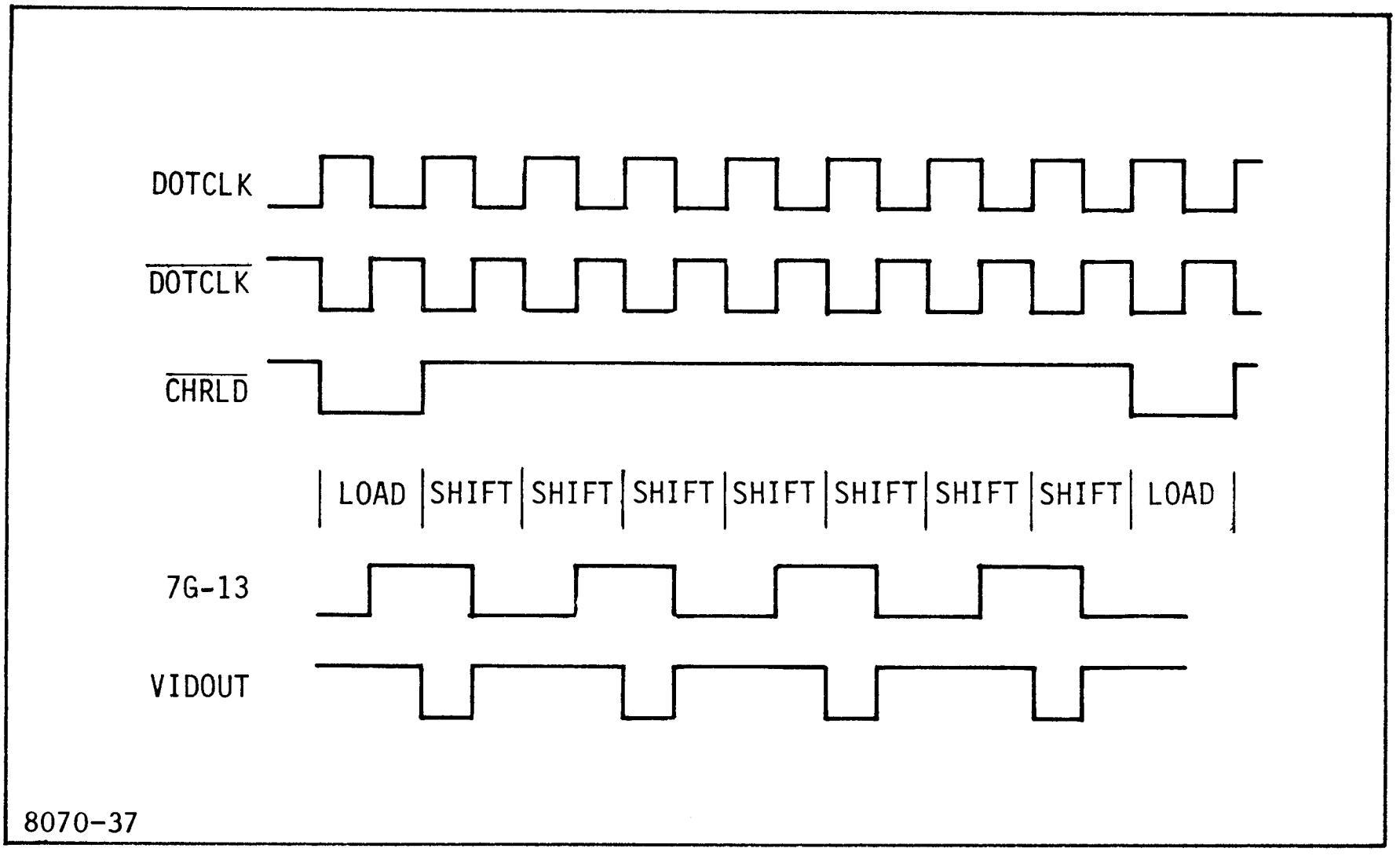


Figure 3-13. Parallel-To-Serial Conversion

3.6.8.3 Line Scan Counter

The line scan counter 10F is a 4-bit binary counter with synchronous loading. It is parallel loaded from the Line Attribute Buffer (four bits) whenever the Load input LD is forced low in concurrence with ROWCK. It is loaded when the output of gate 4B-13 goes low, which occurs each time the character row counter (11C) generates a carry output and when VSYNC occurs. Note that the character row counter generates a carry output when 12 line scans have been counted and that it also is loaded at the same time as the line scan counter 10F. The line scan counter has two counting modes; one for single height character generation and the other for double height character generation, as described in the following paragraphs.

Single Height Mode - In single height mode the line scan counter counts each -ROWLD clock appearing as ROWCK, i.e., it counts 12 rows and is then parallel loaded. Its outputs (CA0-CA3) determine the four address bits A0-A3 to the character generator. These four address bits represent a 4-bit binary number for the duration of one complete line scan, while the other address bits change as the scan passes each character position.

The line scan counter is enabled for counting in this mode by the QA output of the associated divide by two counter, which provides the P enable to the line scan counter. The divide by two counter is itself parallel load coincident with the line scan counter, so that the QA output is high. In this case the P enable to the divide by two counter is low (DBLW=low), so that it cannot count and the QA outputs remains high. Note that by default DBLH=low=single height.

Double Height Mode - To double the height of a character row the same line scan is repeated once, so that a character row consists of 24 line scans (12 identical pairs). To effect double height character the divide by two counter is enabled to count, so that the line scan counter counts alternate ROWCK clocks, so that CA0-CA3 are constant for the duration of two line scans. The character row counter still generates a carry output at the end of 12 line scans, but in effect counts two character rows for each couble height row displayed.

In this case the divide by two counter is parallel loaded as before, but DBLH=high to provide a P input enable, so that the output QA toggles with alternate ROWCK clocks.

The timing for each mode of operation is shown in figure 3-14 and figure 3-15.

3.6.8.4 Line Attribute Buffer

The line attribute buffer 10E is loaded from the MPU data bus when the I/O address decode -LATTLD is activated. The four least significant bits signify the value of the initial count to be loaded into the line scan counter 10F. The four most significant bits have the following significance.

PD7 = Load one into divide by 2 counter

PD6 = DBLH (1 = double height, 0 = single height)

PD5 = DBLW (1 = double height, 0 = normal width)

PD4 = DISLIN (0 = disable line, 1 = enable line)

The functions of loading one into the divide by two counter and single and double height timing have been discussed.

If DBLW = 1, Logic Diagram Sheet 3 shows that the B inputs to multiplexer 8J are selected as outputs. Assuming 80 column display is selected, the effect is as shown in figure 3-16. Character load still takes place on every eighth dot clock, but by comparison with figure 3-7, the time frame between consecutive -CHRLD pulses has been doubled and the dot clock period has been doubled. This has the effect of doubling the width of the displayed characters and horizontally lengthening the dot to twice the normal length.

If DISLIN = 0, the line is effectively erased. Logic Diagram Sheet 8 shows that DISLIN, when low, clears the screen data and attribute latches; i.e., an all zeros dot code is presented for the duration of the time DISLIN remains in the low state, and likewise no display attributes are presented.

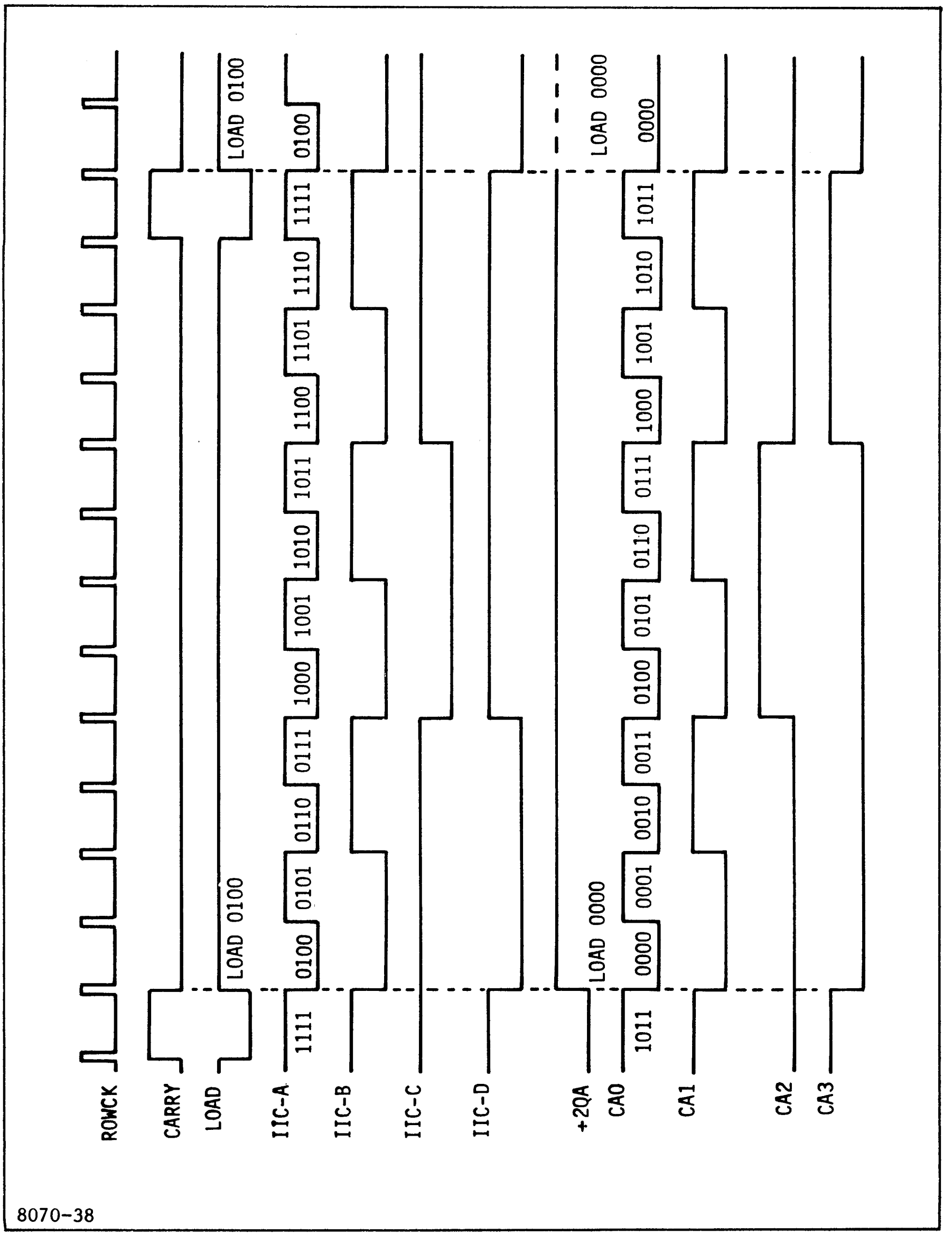


Figure 3-14. Single Height Character Timing

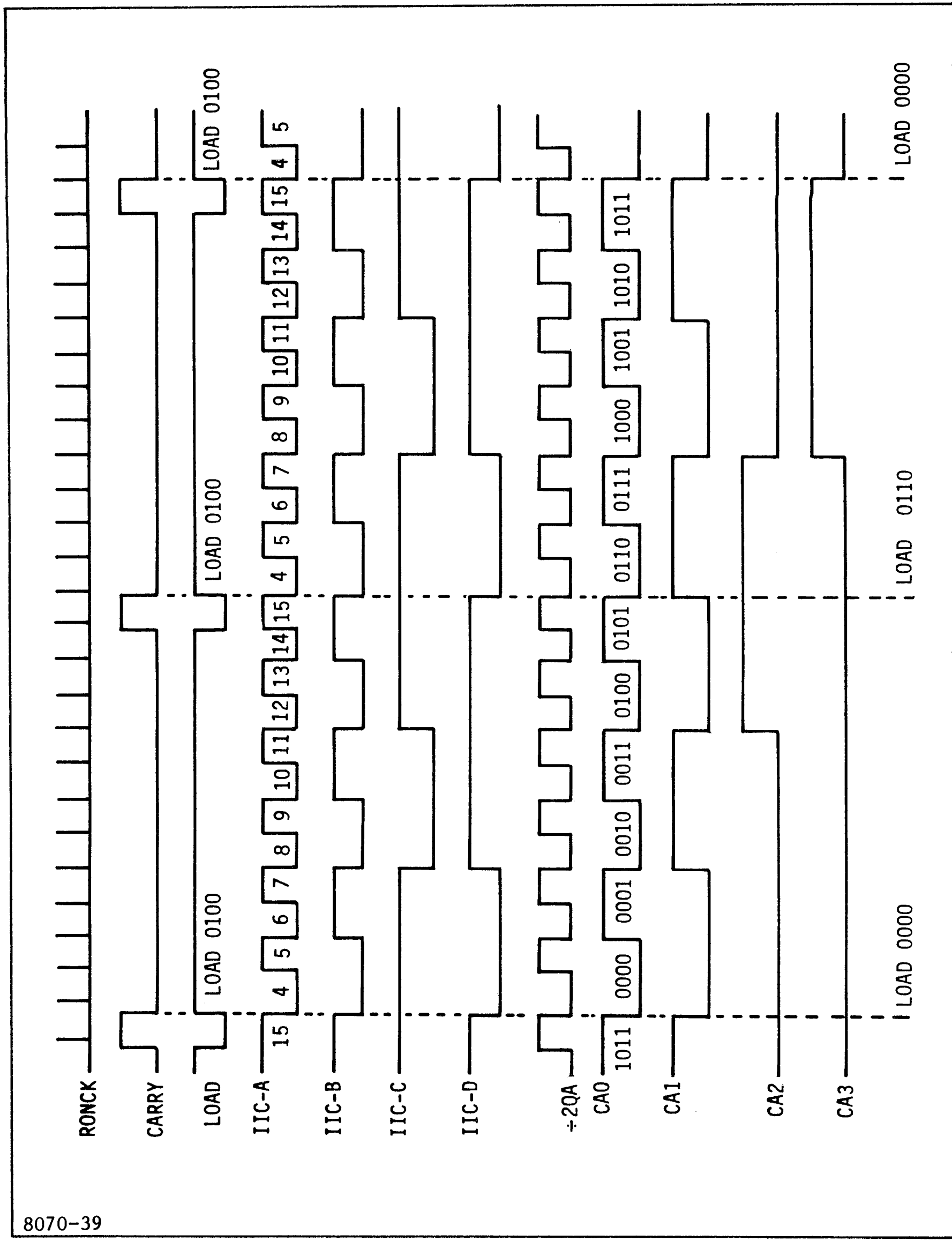


Figure 3-15. Double Height Character Timing

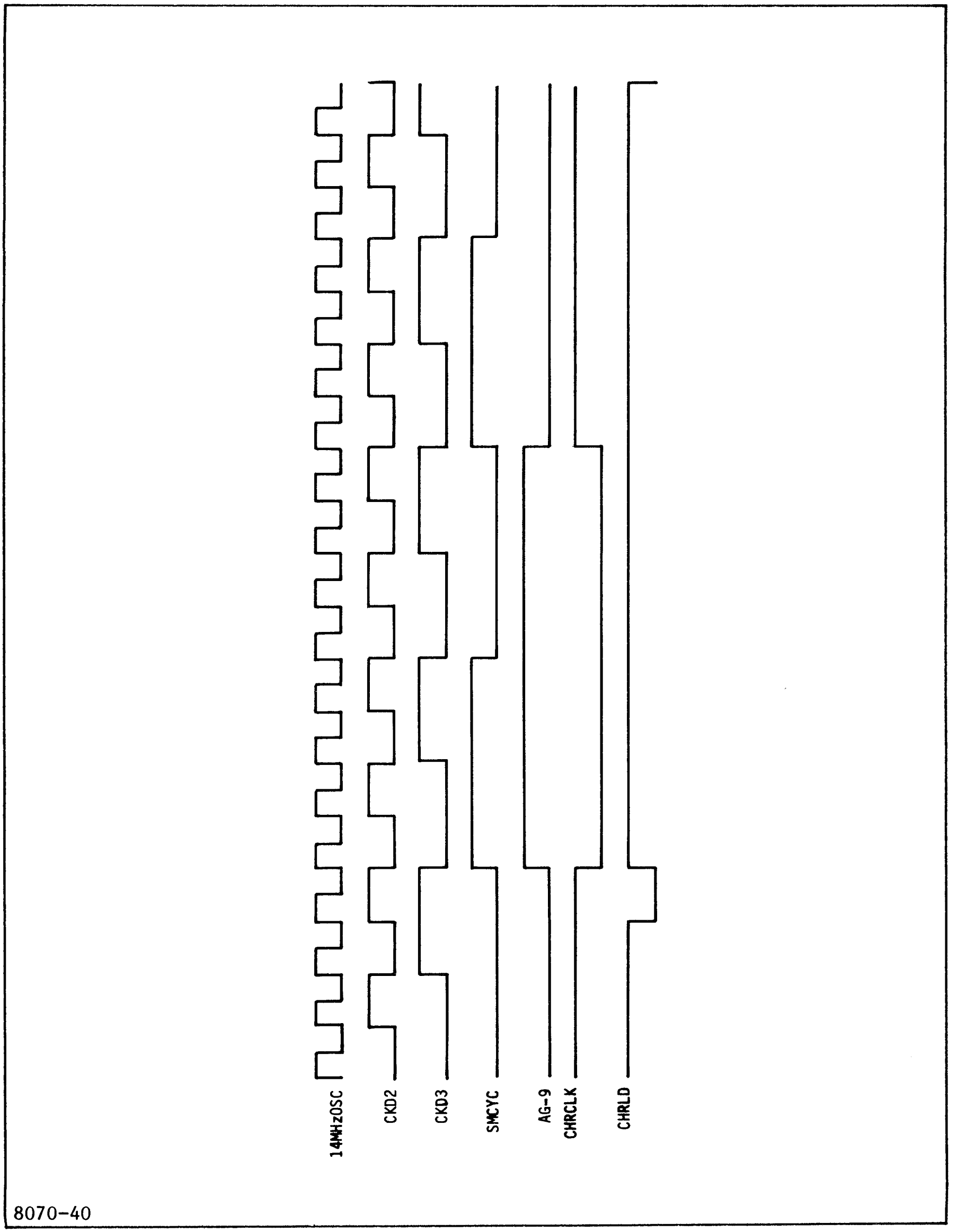


Figure 3-16. Double Width Timing

3.6.9 Composite Sync and Video Circuits

The composite video circuits are shown on Logic Diagram Sheet 10. The circuits consist of the buffer register 11J, the digital-to-analog converter 4L (the brightness control circuit), associated gates and drivers, and the Blink frequency generator.

The display attribute bits from Screen Memory, together with the DISP signal from the CRTC and the Half Intensity signal HFINT from the character data buffer are clocked into buffer register 11J coincident with the positive going edge of SMCYC. The buffer outputs provide the control signals that determine the manner in which characters are to be displayed. The only signal not buffered is the composite sync signal, which is the Xor of -HSYNC and VSYNC (-VDR) as shown in figure 3-17. The VSYNC latch 12E provides an output that converts the duration of VSYNC into a multiple of HSYNC pulses, and in so doing synchronizes the vertical drive pulse with the horizontal drive pulse. It appears from figure 3-17 that while the output from inverter 3G-10 is low, HSYNC is inverted; this is of no consequence, since the reference level is shifted by the bias circuit, such that all of the sync pulses are negative, i.e., below the visual threshold level. The composite sync signal is algebraically summed with the brightness level from the digital-to-analog converter and the half intensity signal from 11J. This combined signal, less video, is fed via CR3 to J3 pin 4 and from there to the monitor. It is also fed via emitter follower Q3, which also functions as a level converter, to BNC connector J2 and to J3 pin 8.

The brightness level is expressed as a digital value by the MPU, on demand from the keyboard. This digital value is placed on the data bus by the MPU when the digital-to-analog (D/A) converter 4L is addressed as an I/O device. The I/O address decode -BRITLD clocks the digital value into the internal D/A buffer. The digital value is converted to a corresponding alalog voltage level which is level converted by one half of the operational amplifier pair 2L. The output is then fed to the base of Q3, which acts as the voltage summing node for the brightness, intensity, and composite sync.

The Blink generator consists of the four bit binary counter 12C and the D-type flip-flop 5L, which are configured as a 5-bit counter. The counter is clocked by the vertical drive, such that each count signifies the duration of a complete frame. The counter output BLINKCK (Blink Clock) represents 32 frame periods. It is low for 16 frame times, then high for 16 frame times, approximately equivalent to a half second off and a half second on. When blinking is enabled (BLINK = 1), the Blink output of buffer 11J provides an enable to Nand gate 4J pins 1 and 2, which then inverts BLINKCK at its output 4J-12. This output provides an alternating enable to Nand gate 4J pins 9 and 10, which then alternately inverts VIDOUT and enables the Nand gate. In this way, the matrix code is displayed for 16 frame times, then inhibited for 16 frame times, which give it the appearance of flashing or blinking. Note that this function can be accurately controlled by the MPU to include any number of characters. If blinking is disabled (BLINK = 0), 4J pins 9 and 10 are held at the high level, so that VIDOUT appears inverted at 14J-8.

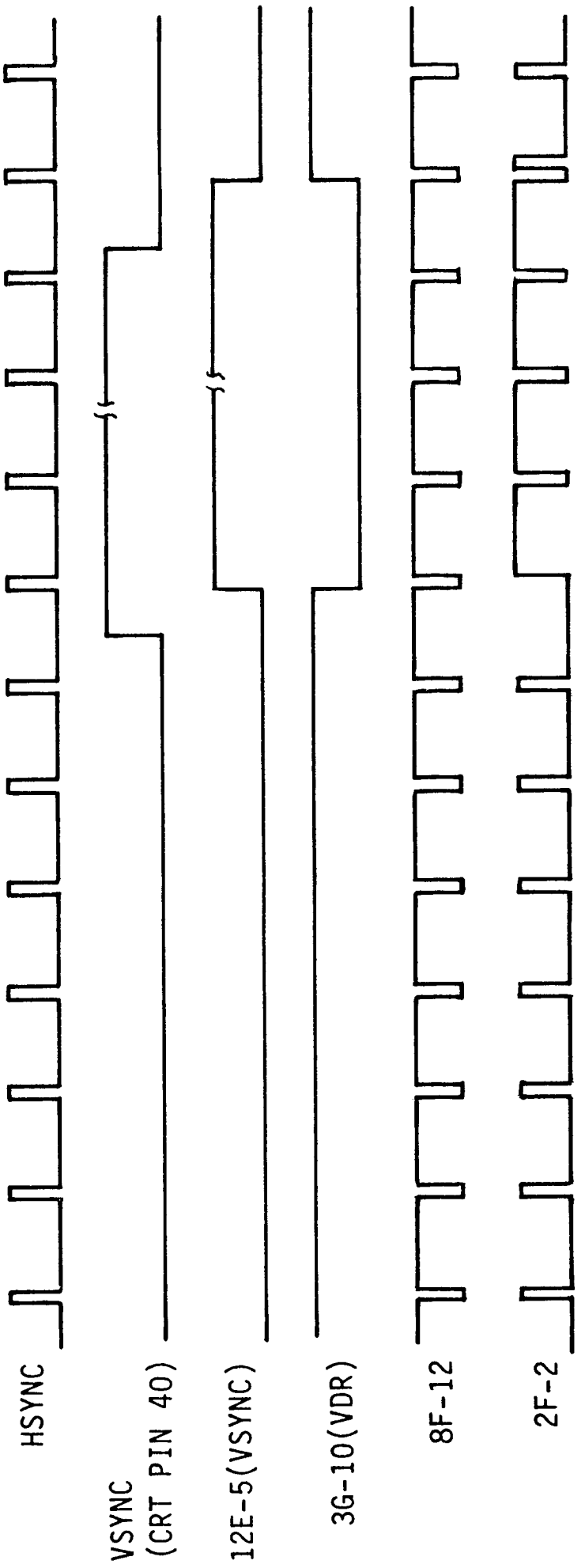


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Figure 3-17. Composite Sync

If Underlining is specified (ULINE = 1), the output of buffer 11J (pin 6) provides an enable at Nand gate 9F pin 1. The remaining three inputs to Nand gate 9F are derived from a selected combination of line scan counter outputs, either CA0, CA1, CA3, or CA1, CA2, CA3. Reference to figure 3-14 shows the first combination coincides with line 12, the last line in the dot matrix, which is normally blank (an all zeros dot matrix code). By inverting an all zeros code to an all ones code, a line would appear. This is the function of the first Xor gate 2G. The output of Nand gate 9F will be low during the scan of line 12 for the period ULINE is high, as controlled by the MPU from information received from the keyboard or the host. The output of Nand gate 4J-8 will then appear at 2G-3, remembering that 4J-8 is the inverse of VIDOUT, which is the inverse of the parallel-to-serial converter. If underlining is disabled, the Nand gate output 4J-8 appears inverted at 2G-3.

The second of the Xor gate 2G is the reverse video control gate. An Xor gate can provide two functions, first as a non-equivalence comparator (inverter) and second as a simple gate. Consider the truth table for a 2 input Xor gate:

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0

If reverse video is specified (REVID = 1), the output of buffer 11J pin 2 is high (2G-4), so that whatever appears at 2G-5 is effectively inverted at 2G-6. If REVID = 0, the output 2G-6 follows the input 2G-5; i.e., there is no inversion, remembering that the output of Nand gate 4J-8 represents the output of the parallel-to-serial converter of the true state of the dot matrix code.

The last gate in the video control circuits is the third Nand gate 4J (discounting inverter 3G), which is either enabled or disabled by the BLANK attribute bit. If BLANK is high, the output of buffer 11J pin 19 is held and is inverted to disable Nand gate 4J, such that its output goes high and 3G-8 goes low (VIDTTL = 0); i.e., there is no video (dot matrix) signal. If BLANK is low, Nand gate 4J-4 is enabled and the output from 2G-6 is inverted by -ROWLD (4J-5), which is in effect when the DISP (Display Enable) signal is low; i.e., video is inhibited for the period DISP is low, e.g., during horizontal and vertical flyback periods.

Note that VIDTTL is referenced to +5V (high) and OV (low) and represents the dot matrix code, in one or other of the attribute formats, whereas VIDIN is referenced to +12V and -12V and represents composite sync, brightness level, and intensity level. There is no signal combination that represents composite video.

3.6.10 Keyboard Interface

The keyboard code generator and interface logic is shown on Logic Diagram Sheet 11. It consists of the parallel-to-serial converter 10B, the clock counter 12C, the timing and synchronization flip-flops 13C, Nand gates 10J and two inverters 1G.

The MPU interrogates the keyboard by transmitting a matrix code to the keyboard logic. The matrix code effectively addresses one of 80 keys. If the addressed key has been pressed, the response from the keyboard is equivalent to a one bit or high level. If the addressed key has not been pressed, the response is a zero bit or low level. In this way, the MPU scans all 80 keys (matrix positions) in less than 12 milliseconds. The timing of a single key scan is shown in figure 3-18, which depicts a matrix code of alternate ones and zeros.

The MPU places the matrix code on the data bus and performs an I/O operation to the keyboard interface, whose address is decoded by -KEYLD. When -KEYLD goes low, the matrix code is parallel loaded into shift register 10B, which functions as a parallel-to-serial converter.

When -KEYLD goes high, the first of flip-flops 13C is clocked into the set state. The second flip-flop is held in the clear state during the time that counter output 12C-QD is low and cannot be clocked into the set state until 12C-QD goes high. When this occurs, the next positive going edge of counter 12C-QC sets the second flip-flop, which immediately clears the first flip-flop. The second flip-flop remains in the set state for the remaining period that 12C-QD is high. This allows 8 CKC80 clocks to be gated through And gate 11G-11, as shown in figure 3-18.

If the output of the shift register is a one bit (10B9 = 1), then Nand gate output 10J-6 goes low for one half CKC80 clock period, as shown. If the output of the shift register is a zero bit (10B-7-1), then Nand gate output 10J-12 goes low; otherwise 10J-8 is low. This output is inverted twice to provide KEYOUT, the serial data output to the keyboard logic. The first inversion is used to clock the shift register, which coincides with the negative or high to low transition of KEYOUT. The serial bit pattern shown in figure 3-18, which represents alternate ones and zeros, also depicts pulse width modulated data, where a one bit is double the width of a zero bit.

The response from the keyboard appears as KEYIN, which is a high level to signify that the addressed key was pressed, or conversely is a low level. KEYIN appears on the MPU data bus in bit position PD0, when the MPU activates -RDST (the read status decode). This is in response to an input operation addressed to the keyboard or CRTC. Note that the MPU determines if the display scan is in the vertical blanking period by examing the state of the RETRACE signal, which appears as PD1.

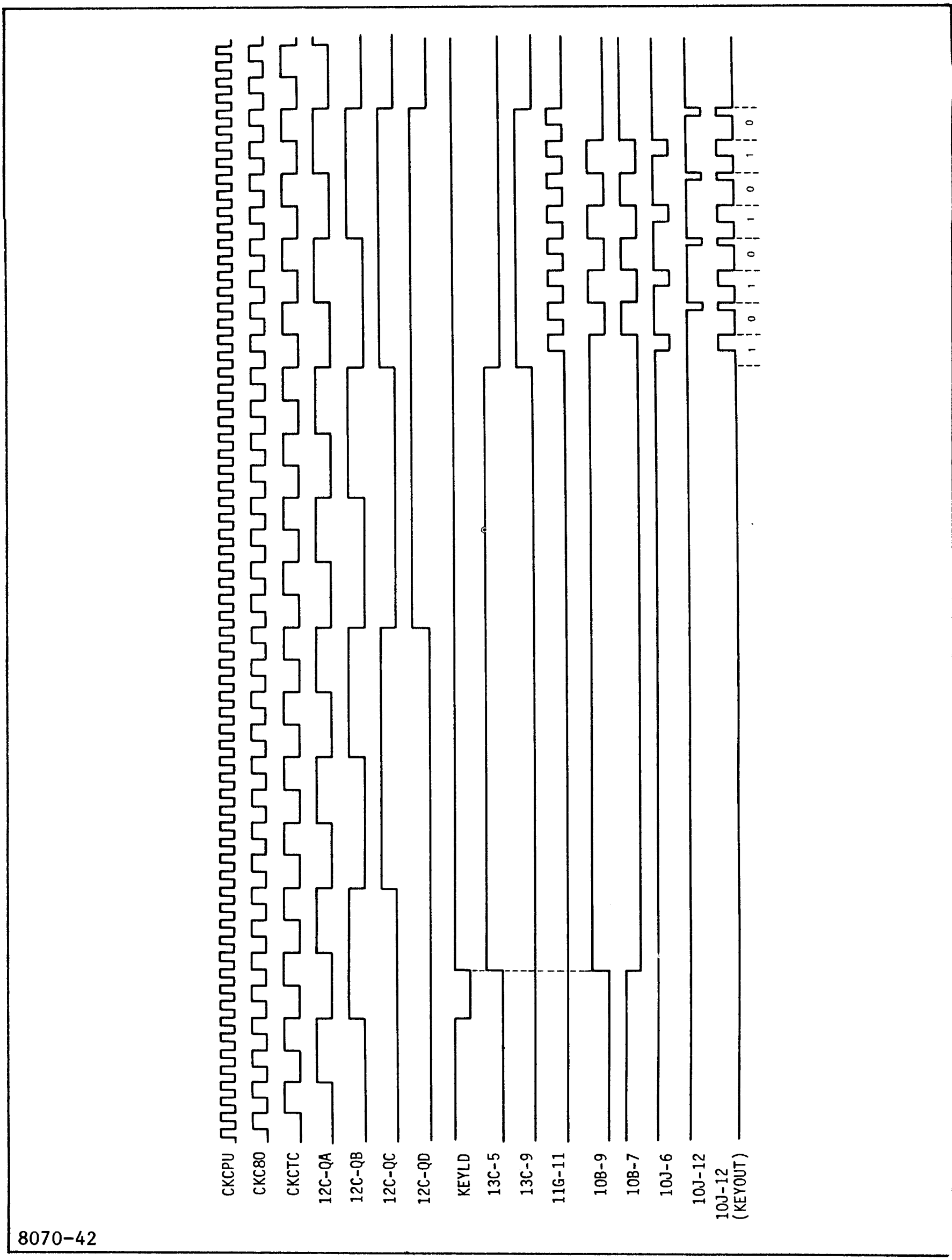

Figure 3-18. Keyboard Matrix Code Transmission

3.6.11 Counter Timer Circuit (CTC)

The CTC (5C) is shown on Logic Diagram Sheet 4. The CTC is a four channel counter/timer, programmed by the MPU to provide the baud rate clock for the two serial I/O ports in the DART (paragraph 3.6.12), and the clock train that drives the Bell latch 5L.

The CTC has four independent counter/timer channels (0, 1, 2 and 3). Each channel is individually programmed by two bytes; a control byte and a time constant byte. The control byte selects the operating mode (counter or timer), enables or disables the channel interrupt and selects certain other operating parameters. If timer mode is selected, the control byte also sets a prescaler, which divides the clock input ZCK (CKCPU) by either 16 or 256. The time constant byte is a binary value from 1 to 256.

During operation, the individual counter channel counts down from the preset time constant value. In counter mode, the counter decrements on each of the CLK/TRG input pulses until zero count is reache. When this occurs, the ZC output is activated and the down counter is automatically reloaded with the time constant value.

In timer mode, time intervals as small as the system clock period (CKCPU) can be determined. The time intervals are generated by dividing the clock (ZCK) with a prescaler that decrements a preset down counter. The time interval is an integral multiple of the clock period, the prescaler value (16 or 256) and the time constant that is preset in the down counter. A timer is triggered automatically when its time constant value is programmed, or by an external CLK/TRG input.

To communicate with the CTC, the MPU executes an I/O to the CTC and places the device address on the address bus. The address is decoded as -CTCE and the selected channel is determined by address bits A0, A1, as follows:

A1	A0	CHANNEL
0	0	0
0	1	1
1	0	2
1	1	3

The MPU also determines if data is being sent to the CTC or being read from the CTC by the state of the -RD signal: -RD = high = write to CTC (output), -RD = low = read from CTC (input). In the case of a write operation, the consecutive bytes are sent to the selected channel, the control byte followed by the time constant. In a read operation, the value in the down counter is returned to the MPU (time remaining to zero).

The significane of the control bytes is as follows:

D7 Interrupt: 1 = enable interrupt, 0 = disable interrupt

D6 Mode: 1 = counter, 0 = timer

D5 Prescaler: 1 = 256, 0 = 16 (timer mode only)

D4 CLK edge: 1 = rising edge, 0 = falling edge

D3 Timer Trigger: 1 = trigger when time constant loaded,
0 = trigger from CLK pulse

D2 Time Constant: 1 = time constant follows control byte,
0 = no time constant

D1 Reset: 0 = continued operation
1 = reset by MPU

D0 Control/Vector: 0 = vector value
1 = control byte

Channel 0 is controlled as a counter, counting CKCTC clocks. It counts down to zero and AC0 provides the baud rate clock to the first I/O port in the DART. Channel 1 is likewise controlled to count down CKCTC clocks; its output ZC1 provides the baud rate clock to the second I/O port in the DART. Channel 2 is controlled as a timer that is automatically triggered when the time constant is loaded. Its output provides the clock trigger to the Bev taken 5L. Channel 3 is used for internal control timing.

3.6.12 Dual Asynchronous Receiver/Transmitter (DART)

The DART contains two fully independent serial communications controllers, operating in half or full duplex mode. Each channel (A or B) contains six write registers that control operating parameters for the channel, and three read registers that provide status information for the channel. Each channel is programmed with set up parameters by the MPU, and each channel has the capability of activating a MPU interrupt for service during the execution of an operation, according to information in the status registers. A block diagram of the DART is given in figure 3-19, and a pin-out description is provided in table 3-3.

The Write Registers contain control information for asynchronous operation and permit selection of 5, 6, 7, or 8 data bits; one, one and one half or two stop bits; whether or not a parity bit is to be included and if so, whether even or odd parity is to be used. The Write Registers also contain control information specifying when and under what conditions an interrupt is to be generated, usually when the transmit buffer is emptied during transmission, and when a received character has been assembled and is available. One of the Write Registers contains the interrupt vector address. The Read Registers contain status information from which the MPU can determine if transmission or reception was successful, and if not the nature of the problem, e.g., parity error, transmitter underrun, receiver overrun, framing error, etc.

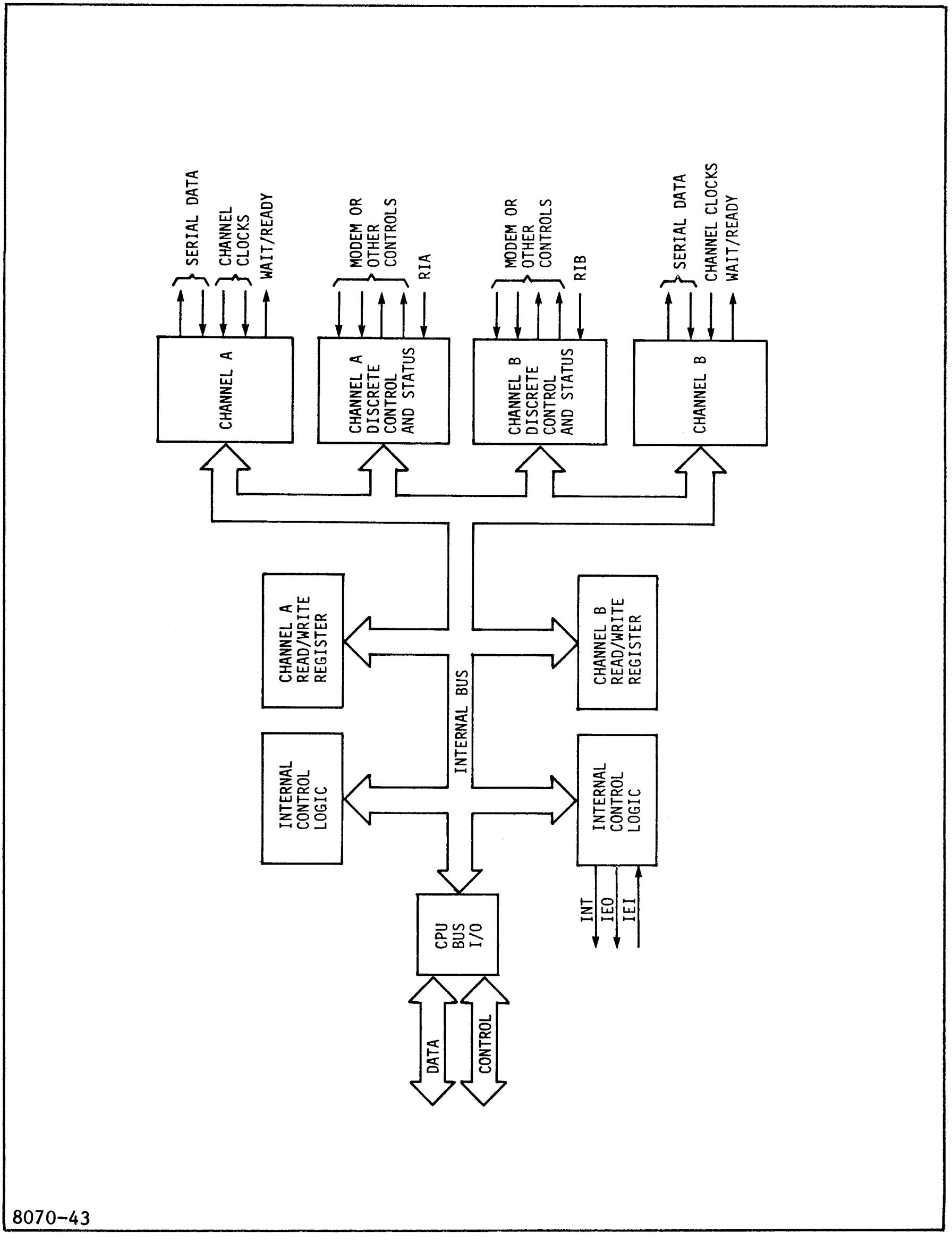

Figure 3-19. DART Block Diagram

Table 3-3. DART Pin-Out Description

PIN	MNEMONIC	DESCRIPTION
34	B/$\overline{A}$	Channel A or B Select. High selects B, low selects A. Controlled by address bit A1.
33	C/$\overline{D}$	Control or Data Select. High selects control, low selects data, with reference to information on the MPU data bus. Controlled by address bit A0.
35	-CE (-SIDE)	Chip Enable. Active low input. Low enables the DART to accept command or data input from the MPU during a write cycle, or to send data to the MPU during a read cycle.
20	CLK ($\overline{O}$)	System Clock Input. The DART uses the MPU clock ZCK (CKCPU) to synchronize internal functions.
18 23	-CTSA -CTSB	Clear to Send Inputs. Active low enables the respective transmitter.
40,1, 39,2, 38,3, 37,4	D0-D7	MPU Data Bus. Bi-directional, three state lines which carry data, commands, and status between the MPU and the DART.
19 22	-DCDA -DCDB	Data Carrier Detect. Active low inputs which serve as receive enables.
16 25	-DTRA -DTRB	Data Terminal Ready. Active low outputs which follow the state programmed into the DTR bit in Write Register 5.
6	IGI	Interrupt Enable In. Active high input forming part of interrupt daisy chain. High indicates DART can initiate an interrupt, low indicates high priority device (CTC) is being serviced. In this case, IGI is IEO from CTC.
7	IGO	Interrupt Enable Out. Active high output forming part of interrupt daisy chain. High notifies next device in daisy chain that it may initiate an interrupt; low notifies next device that the DART is being serviced. IGO is routed to the expansion connector.
5	-INT	Interrupt Request. Active low output notifies MPU that a device is requesting service.
8	-M1	Machine Cycle One. Active low input from MPU. When -M1 and -RD are both active, the MPU is fetching an instruction from memory. When -M1 and -IORQ are both active, the MPU is acknowledging an interrupt to the device with IEO low.

Table 3-3. DART Pin-Out Description (continued)

PIN	MNEMONIC	DESCRIPTION
36	-IORQ	Input/Output Request. Active low input from MPU. Used in conjunction with B/A, C/D, CE (-SIDE), and -RD to transfer commands and data between MPU and the DART. When -CE, -RD, and -IORQ are all active, the channel selected by B/A transfers data to the MPU. When -CE and -IORQ are active but -RD is inactive, the channel selected by B/A receives control information or data according to the state of C/D.
13 27	R X CA R X CB	Receiver Clocks. Inputs from CTC. Receive data is sampled on the rising edge of R X C. The clock inputs may be 16, 32, or 64 times the data rate. Note that R X CB (pin 27) is both the receive clock and transmit clock input for channel B.
32	-RD	Read Cycle. Active low input from MPU. If -RD is active, a memory or I/O read operation is in progress.
12 28	R X DA R X DB	Receive Data Inputs. High = one bit, low = zero bit.
21	-RESET	Reset input active low. Disables both receivers and transmitters, forces T X DA and T X DB marking (high). Forces modem controls high and disables interrupts.
11 29	-RIA -RIB	Ring Indicators. Not used.
17 24	-RTSA -RTSB	Request to Send. Active low outputs. When the RTS bit is set in the associated Write Register, -RTS goes low. It is used to interrogate the receiving device at the end of the communication line in notification of a pending transmission. If the outer device is ready, it activates its DTR output (Data Terminal Ready), which appears at the DART end of the line as CTS (Clear to Send).
14 27	T X CA T X CB	Transmitter Clocks. Inputs from CTC. Transmit data changes on the falling edge of T X C. Clocks may be 16, 32, or 64 times the data rate; however, they must be the same as the receive clocks. Note that T X CB (pin 27) is also the R X CB input.
15,16	T X DA, T X DB	Transmit Data Outputs. High = one bit or marking, low - zero bit or start bit.
10,30	-W/-RDYA, -W/-RDYB	Wait/Ready Outputs. Not used.

3.6.13 Keyboard Logic

The keyboard logic is drawn on a single diagram, which is provided in Section VI. The diagram shows the key matrix, consisting of eight rows (Y0-Y7) and 10 columns (X0-X9); two strobe (clock) generators U3; the timer U1; the serial/parallel converter U5; the BCD-decimal decoder U4; the row scanner U6; and the output latch U7.

Pulse width modulated data (matrix code) is fed serially to the serial/parallel converter U5 (shift register) and the positive edges trigger the first half of U3 (one-shot). The duration of this strobe (one-shot) is wider than a zero bit and narrower than a one bit. The positive trailing edge of the negative strobe effectively demodulates the signal input, as shown in figure 3-20. If a one bit is strobed, the serial input is high when the shift register is clocked and a one-bit is shifted in. The timer counts the number of times the demodulating one-shot is triggered. It follows that after eight serial shift operations, the matrix code character will occupy the shift register. The timer triggers the second strobe (U3) at this point, which then enables the gates U8, U9, U10, U11, and U12 to provide column selection.

The first four bits in the shift register represent the BCD value of the column (0-9); the four bits are decoded by the BCD-decimal decoder U4 to select the column. The next three bits scan the particular row by determining which of the inputs to multiplexer U6 will appear as the output. The last bit in the shift register is termed the hysteresis bit, as will be explained.

When the second one-shot expires, the multiplexer output is latched by U7 and the decoder output gating logic is disabled. As previously explained, when a key is pressed, there is an induced voltage inone of the auto-transformers T1A-T1B through T4A, T4B, according to the intersection of the row and column. The latch output is a level, whch is monitored by the MPU by means of the Read Status decode RD ST. If there is a change in the level, the MPU knows which key has been pressed because of the matrix code. The sequence of events is as follows.

The MPU sends the matrix code to the keyboard by means of the keyboard function and monitors the response. If the level denotes that the addressed key was pressed, the MPU sends the same matrix code again, but turns on the hysteresis bit. If the same response in level occurs from the output latch, the MPU is notified that a key was in fact pressed and that the response was not just a glitch. The MPU goes to a character look-up table and reads the character code corresponding to the matrix code and places the character code in display memory at the cursor address. If a control function is invoked, the MPU branches to the appropriate service routine.

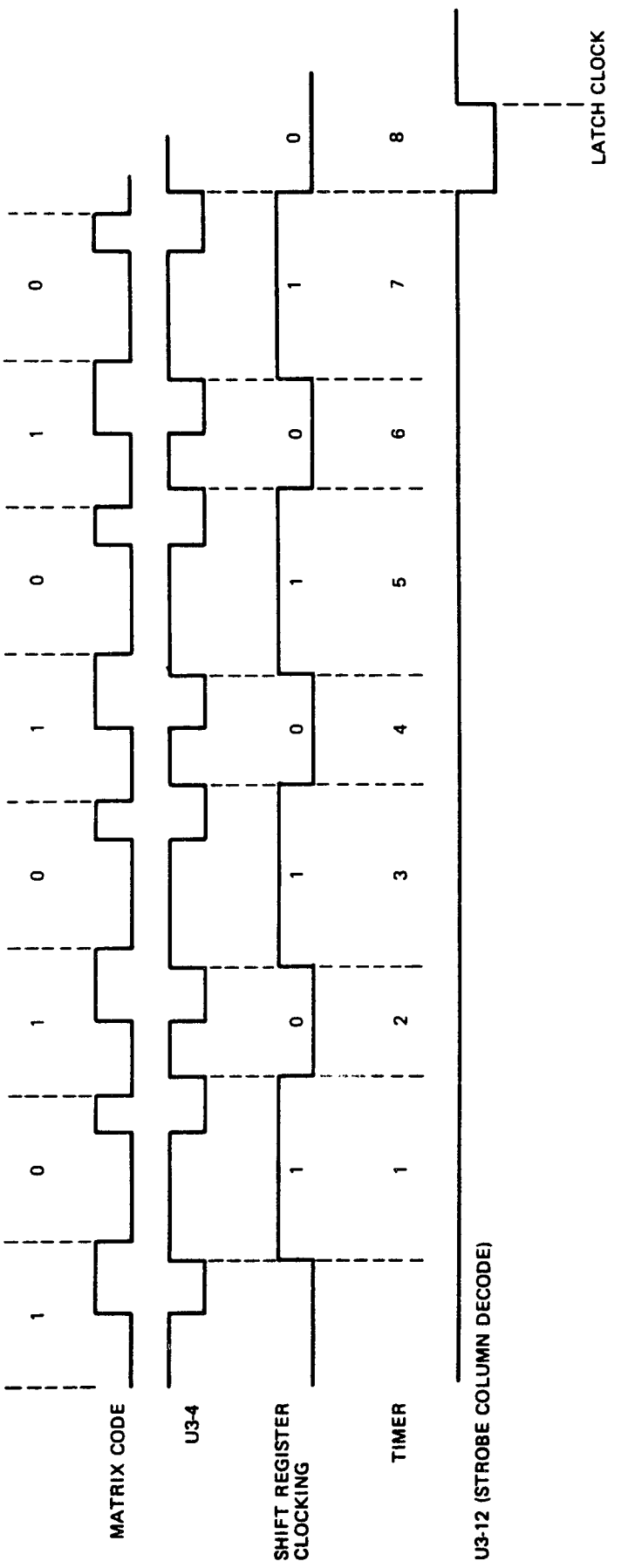

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Figure 3-20. Matrix Code Demodulation Timing

3.6.14 System Firmware

The operating system firmware consists of a relatively small, but sophisticated, multi-tasking operating system. The firmware is modularized, for example, PROM 0 and PROM 1 contain the firmware controlling the EVDT hardware. Other PROMs contain the terminal emulating firmware.

The most basic task (figure 3-21) is that of scanning the keyboard matrix for a pressed key, and also checking to determine if a character has been received from a communications port.

Other tasks control the display memory, tracking the cursor position, and screen refreshing.

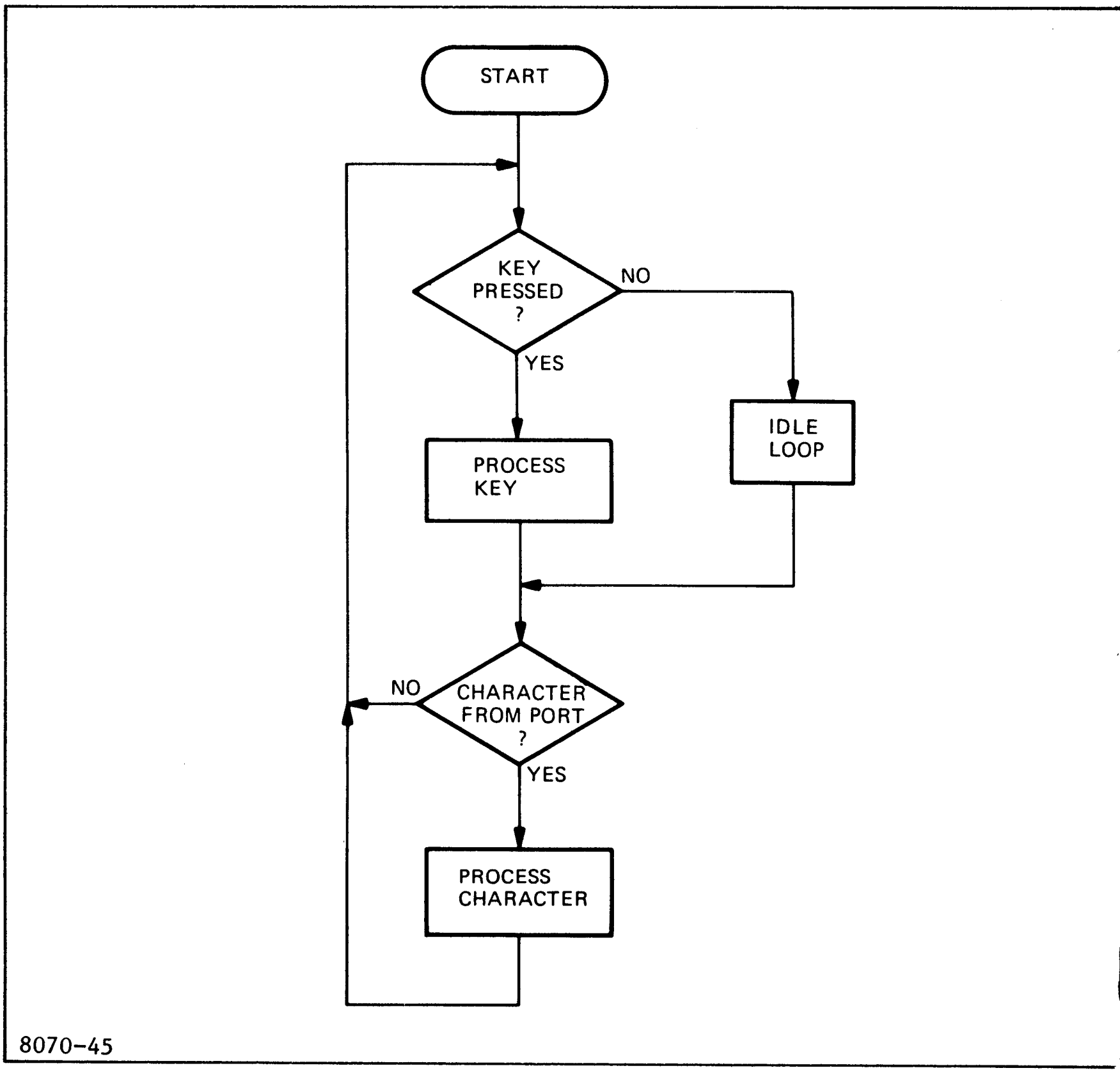


Figure 3-21. Simplified Firmware Flowchart

SECTION IV

MAINTENANCE

4.1 INTRODUCTION

This section contains informatin that will aid the service representative in maintaining and troubleshooting the Model 4309 EVDT. The information is presented in two parts, and contains general procedures for:

- Preventive Maintenance
- Trouble Analysis

4.2 PREVENTIVE MAINTENANCE

The EVDT should be cleaned each time service is performed. Clean the exterior housing and lightly dust the EVDT using a soft brush or damp lint-free cloth. Remove smudges from the exterior housing with conventional spray cleaners. Use only a lint-free cloth to clean the CRT screen, using care not to scratch it.

As part of System Preventive Maintenance, the EVDT should be opened and cleaned using a soft brush to remove dust build-up. The three DC voltages should be checked to verify proper operation of the Power Supply PCBA. The intensity and centering of the display should also be checked and the Monitor Board PCBA adjusted as required.

WARNING

Turn off the EVDT power switch and remove the power cord from the AC outlet before removing the rear housing of the video display assembly. Failure to do so may result in severe shock, which can be fatal, or may result in serious damage to the equipment. Always discharge the CRT anode to ground with a grounding strap before removing any subassemblies.

4.3 TROUBLE ANALYSIS

Trouble analysis essentially consists of two phases. In the first phase, troubleshooting procedures are applied to identify the problem. In the second phase, fault isolation procedures are applied to isolate the source of malfunction.

4.3.1 Troubleshooting Procedures

Before troubleshooting the terminal, it is essential to determine that the problem is within the terminal and that the problem is correctly identified. Troubleshooting should be approached from a logical process of elimination, as outlined in the flowchart in figure 4-1, and as described in the paragraphs that follow. (The flowchart takes into account failure at the module level, and should be used only as a guideline.)

First determine if the fault condition is due to an external power failure (no voltage at service outlet) or an internal power failure (blown fuse, bad power supply). If the fault condition is not due to a power failure, determine if the fault condition is valid (not due to operator error). As a general rule, make sure that all of the unit and module interconnect cabling is properly connected, and that there are no obvious signs of internal short circuits. Always switch off power before removing the rear housing.

Having determined that the fault condition is not due to an incorrect operating procedure, determine if the Master Reset command from the keyboard clears the problem. If it does, and the problem does not recur, the terminal can be considered operational. If the Master Reset command does not clear the problem, the next stage is to identify the problem and troubleshoot accordingly.

If there are numerous symptoms, or what appears to be a combination of problems, such as improper keyboard operation, incorrect display, communications problems, then it is likely that either the CPU or the microcode (PROM's) is bad. Replacing the main logic board or the CPU should resolve the problem. If there is a single symptom, such as incorrect display, no communications with the host or hard-copy printer, then troubleshooting should be directed to a single probable source. Adjustment of the power supply d.c. voltages may correct the condition when numerous symptoms appear.

When a communications problem is encountered, it is important to verify that the communication line is operational, including the line itself (telephone circuits) and attached modems, and that the host computer is operational. Also verify that the terminal can communicate with the hard-copy printer. If there is no communication with either the host or printer, the UART is suspect. If communication is possible with either the host or printer, the associated I/O port is suspect. If the terminal will operate in Block Mode, the CPU, video display, and host communications interface can be eliminated as the source of the problem.

If the problem is not a communications malfunction, the next determination to be made is whether or not the video display is correct, in terms of both format and character content. First, is the display the correct size (24 X 80); second, are the characters formed properly? If the display is not the correct size, the problem may be the tube itself, the CRT controller, or the Monitor board. If the characters are incorreclty formed the problem may be display memory, character generator, or composite video circuits.

If the problem appears to be in the keyboard, it may be an open or short circuit in the connector, in which case the connector should be replaced. The problem may also be in the keyboard interface logic on the main logic board; for example the parallel/serial converter may be bad. This can be verified, using an oscilloscope, by monitoring the serial line to the keyboard and seeing if the matrix code is being transmitted by the interface logic.

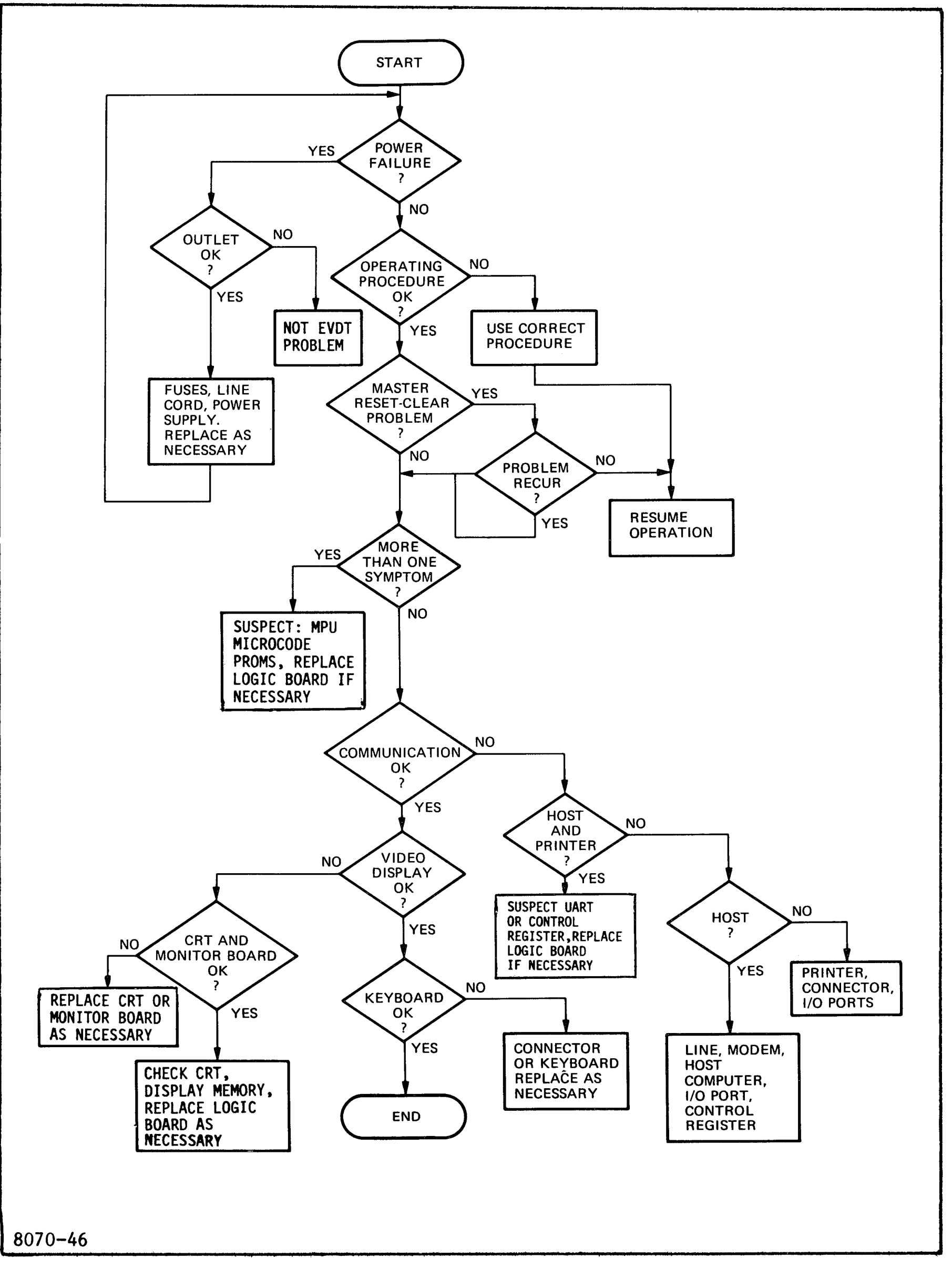


Figure 4-1. Troubleshooting Flow Chart

4.3.2 Troubleshooting Guide

Table 4-1 provides a troubleshooting guide in support of figure 4-1. The table lists fault conditions by symptom, possible cause, and corrective action. Identify the symptom, then eliminate the possible causes, one by one, in the order listed, by taking the necessary corrective action.

The troubleshooting table is not exhaustive and cannot cover all symptoms and possible causes. Its purpose is to serve as a guide, rather than a set of rules.

Table 4-1. EVDT Troubleshooting Guide

SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
A. No 'beep' upon turn on. (Beep signifies successful CPU initialization)	1. No AC power. 2. Blown fuse. 3. Defective firmware. 4. Defective logic.	1. Check for power at outlet. 2. Replace fuse(s). 3. Replace firmware EPROM's. 4. Replace Main Logic board.
B. Screen dark - no cursor or status line.	1. Brightness turned off. 2. Incorrect adjustment. 3. Defective power supply (+12V). 4. Defective monitor board. 5. Cursor is blanked. 6. Status line disabled. 7. Defective logic.	1. Adjust brightness. 2. Perform video adjustments. 3. Replace power supply. 4. Replace Monitor board. 5. Perform Master Reset. 6. Perform Master Reset. 7. Replace Main Logic board.
C. Characters entered from keyboard not displayed.	1. Keyboard connector not plugged into display unit. 2. Defective keyboard. 3. Magnet on key plunger fallen off. 4. Incorrect or defective firmware EPROM's. 5. Incorrect or defective ROM's in character generator. 6. Foreign objects under key caps. 7. Defective logic board. 8. Terminal not in Block Mode. 9. If in conversation mode - problem with host computer.	1. Connect keyboard. 2. Replace keyboard. 3. Install magnet. 4. Replace firmware EPROM's. 5. Replace character ROM's. 6. Remove objects. 7. Replace Main Logic board. 8. Put terminal in Block Mode. 9. Replace Main Logic board.

Table 4-1. EVDT Troubleshooting Guide (continued)

SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
D. Incorrect characters displayed.	1. Baud rate incorrect. 2. Defective character ROM. 3. Defective modem. 4. Defective logic board.	1. Set baud rate (Setup Menu). 2. Replace character ROM. 3. Replace modem. 4. Replace Main Logic board.
E. Keyboard character or function constantly repeats.	1. One key stuck down. 2. Magnet on one key slipped down.	1. Release key. Check for free operation. Replace if necessary. 2. Reposition magnet and glue in position as necessary.
	NOTE: As an aid to identifying the faulty key, perform either a (1) power-on reset (ESCAPE Z command) or (2) FUNCTION and CLEAR. The character then being displayed corresponds to the stuck key.	
F. CRT has incorrect vertical position and/or linearity.	1. Monitor board incorrectly adjusted.	1. Adjust as necessary.
G. CRT has incorrect horizontal position and/or linearity.	1. Monitor board incorrectly adjusted.	1. Adjust as necessary.
H. Screen brightness cannot be adjusted from keyboard or host.	1. Defective logic.	1. Replace Main Logic Board. (741 Op Amp or D/A Converter.)
I. Display wavers in Reverse video.	1. Power supply (+12Vdc) defective. 2. Monitor board. 3. Main Logic board. 4. 50Hz selected in Set Up Menu.	1. Adjust or replace power supply. 2. Adjust or replace Monitor board. 3. Replace logic board. 4. Set 50Hz software switch to 0 in SetUp Menu.
J. Printer does not receive data properly.	1. Incorrect baud rate. 2. Extension Port not on. 3. Cable not connected. 4. Pins 2 and 3 reversed in printer cable.	1. Set correct baud rate on SetUp Menu. 2. Set Extension Port to 1 on SetUp Menu. 3. Connect cable. 4. Replace with RS-232C cable.

4.3.3 Fault Isolation

Fault isolation is the follow-up process of applying the appropriate maintenance procedures to isolate the source of malfunction to the assembly or component replaceable in the field. These maintenance procedures include performing DC voltage checks, test point signal tracing, circuit adjustments, and diagnostic tests in an attempt to locate the malfunction.

4.3.3.1 DC Voltage Checks

Three non-adjustable DC voltages are provided by the Power Supply PCBA. They are + and -12 volts DC and +5 volts DC. These three voltages are measured at connector J1 on the Main Logic PCBA.

Figure 4-2 shows a top view of connector J1 and the pins at which the voltages are measured. The Power Supply PCBA should be replaced if the voltages specified in the following procedure do not fall within their respective ranges.

WARNING

Hazardous voltage is preset within the EVDT enclosure. Use caution when working with the rear housing removed.

1. Remove rear housing of video display assembly as instructed in paragraph 5.2 (Section V).
2. Locate connector J1 (figure 4-2) at the rear edge of the Main Logic PCBA.
3. Apply power to the EVDT.
4. Check for the following voltages on pins 2, 5, and 7 of connector J1:
   - Pin 2: -12VDC, ±1.55V
   - Pin 5: +5VDC, ±0.25V
   - Pin 7: +12VDC, ±1.55V

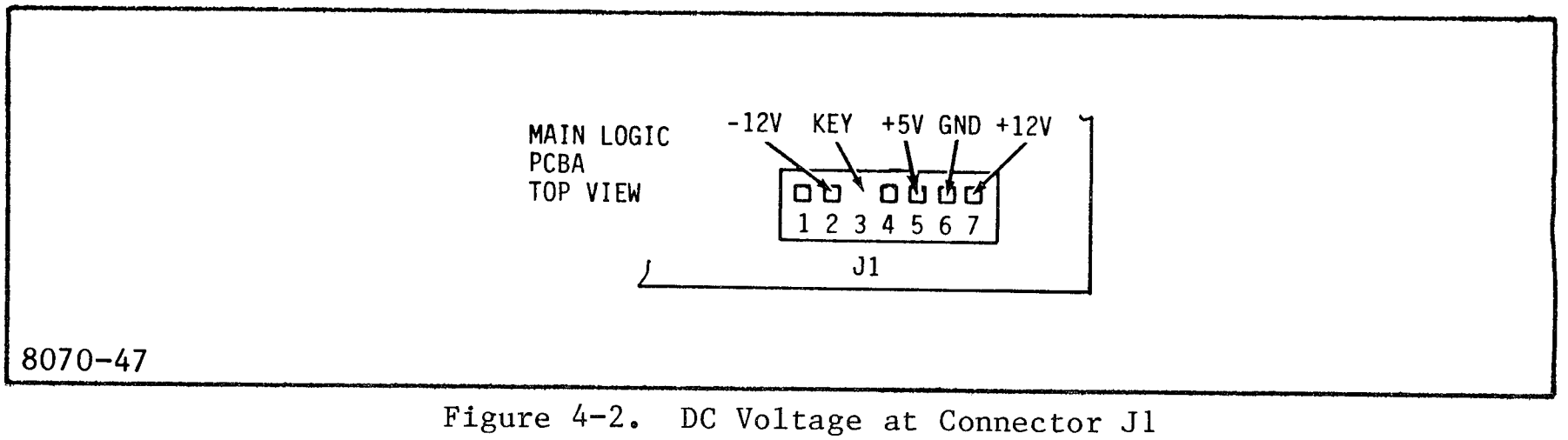


Figure 4-2. DC Voltage at Connector J1

4.3.3.2 Monitor Board (Video) Adjustment

Monitor Board adjustments include brightness, contrast, horizontal centering, vertical height, horizontal width, vertical linearity, horizontal linearity, and focus. All adjustments are made after filling the screen with uppercase Es.

1. To clear memory and reset all controls to default values, perform the Keyboard Master Reset by entering [SHIFT] [CONTROL] [FUNCTION] [ESCAPE/CLEAR] . The screen will briefly display self-test patterns. Release all four keys and wait for time-of-day clock to appear on display status line.

2. Enter [FUNC] [A] to place EVDT in Block Mode. "BK" will appear to the left of the time-of-day clock on the display status line.

3. Enter [0] [1] on numeric keypad.

4. Press and hold [SHIFT] and press [E] key numerous times to produce nearly one full line of Es on the screen.

NOTE

Do not completely fill the line with Es. The cursor must stop short of end-of-line.

5. Enter [FUNC] [^ /SET F] . This stores the line of Es into memory for function key F1.

6. Press Function key F1 enough times to completely fill screen with Es.

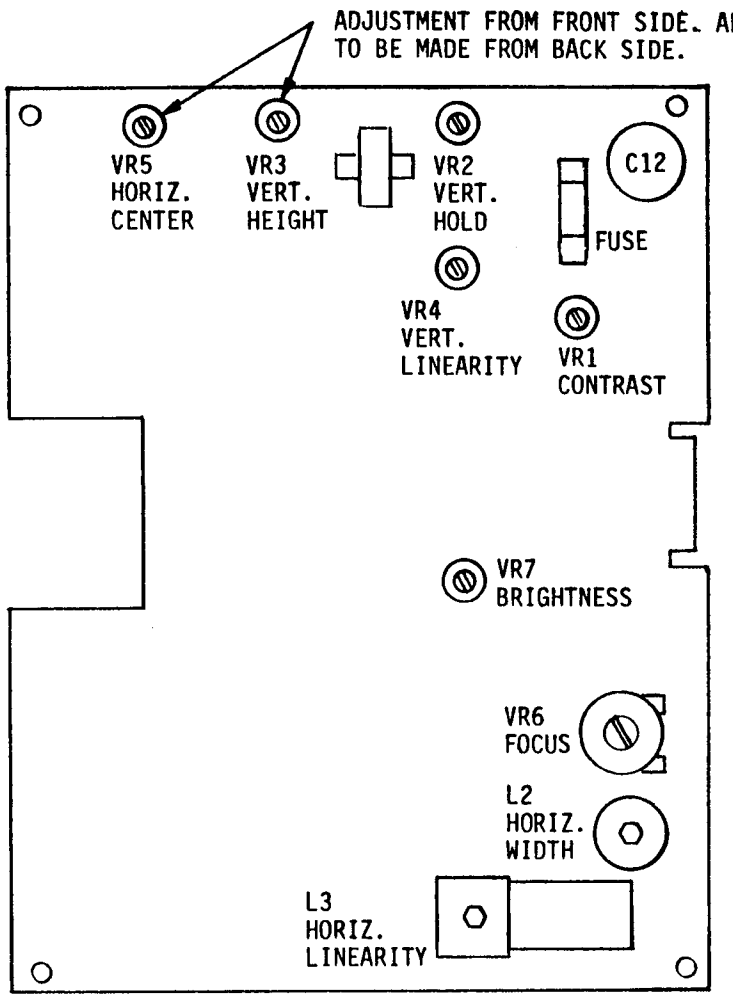
Adjustment of the Monitor Board can now begin. A non-metallic hexagonal alignment tool and a small insulated screwdriver are required to perform the following adjustments.

CAUTION

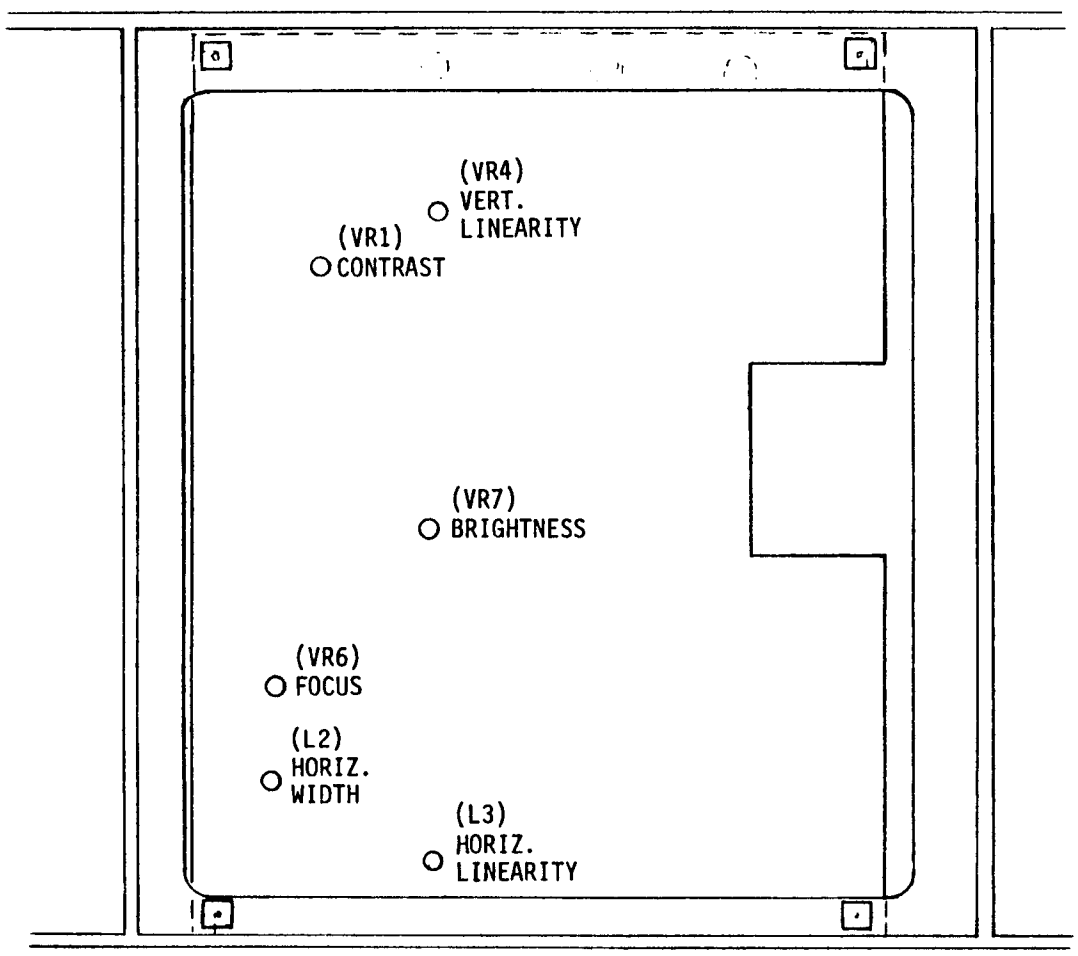
Allow terminal to warm up befor Monitor Board adjustments are performed.

7. Rotate BRIGHTness control VR7 clockwise until raster is visible on the screen (see figure 4-3). Adjust from back side of Monitor Board. Back off BRIGHTness control until raster on screen decreases to a faint image.

8. Rotate contrast (CTRS) control VR1 for desired brightness level of letters on the screen. Adjust from back side of Monitor Board.



VIDEO BOARD (FRONT SIDE)
INSIDE VIEW OF TERMINAL



VIDEO BOARD (BACK SIDE)
OUTSIDE VIEW OF TERMINAL

8070-48

Figure 4-3. Location of Monitor Board Controls

9. Rotate horizontal (H-) CENTER control VR5 to center the video horizontally in the raster. Adjust from front of Montior Board.

10. Loosen yoke locking screw (see figure 4-4). Turn the yoke for horizontal alignment of the display (no tilt). Tighten yoke locking screw.

11. Adjust the two deflection centering tabs on the back of the yoke (rotate either direction) to center the raster on the screen.

12. Decrease the BRIGHTness control (VR7) until the raster just disappears.

13. Adjust the vertical height of the screen to measure 6-1/2 inches from the top of the display status line (BFIS 4309 BK A HH:MM:SS) to the bottom of the last row of Es. Rotate vertical (V-) HEIGHT control VR3 from front side of Monitor Board.

14. Adjust the horizontal width of screen to measure 8-1/2 inches from first E to last E in a row. Using a non-metalic hexagonal alignment tool, rotate horizontal WIDTH control L2 from back side of Monitor Board.

15. Adjust vertical linearity at top and bottom of screen for equal number of rows (Es) in 1-inch vertical measure. Rotate vertical (V-) LINEarity control VR4 from back side of Monitor Board.

CAUTION

Use care in the following step to avoid dislodging the rotating magnetic core from the housing of horizontal LINEarity control L3.

16. Adjust horizontal linearity at left and right side of screen for equal number of Es in 1-inch horizontal measure. Rotate horizontal LINEarity control L3 from back side of Monitor Board.

17. Adjust video focus for sharp characters. Rotate FOCUS control VR6 from back side of Monitor Board.

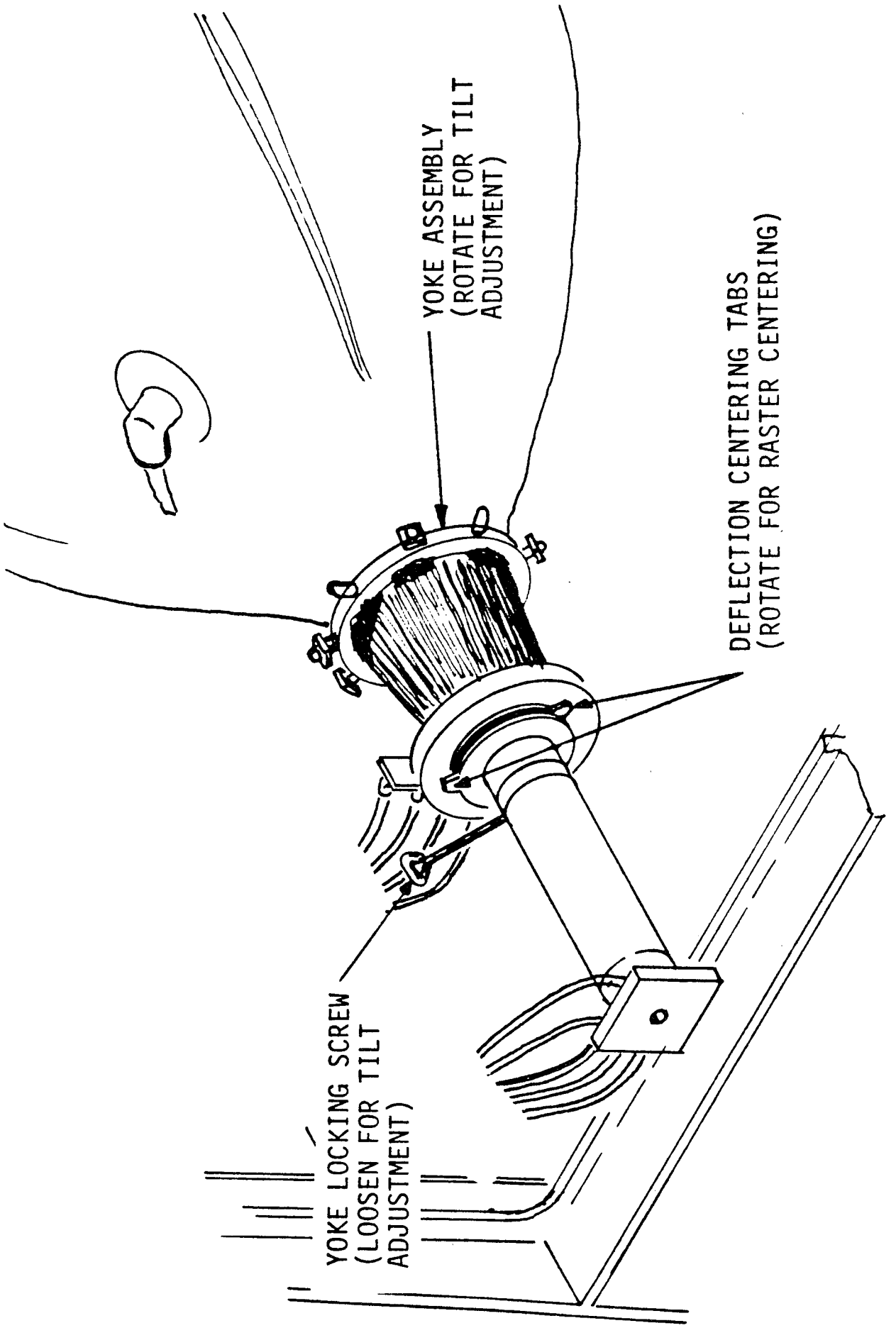


Figure 4-4. CRT Yoke Adjustments

4.3.3.3 Monitor Board Signal Tracing

Signal tracing may be used to verify the Monitor Board PCBA as being the source of display-oriented malfunctions. The standard waveforms at the various Monitor Board test points are shown in figure 4-5 (sheets 1 and 2). Note that the test points referenced in figure 4-5 are "in-circuit" test points, and are shown only on the Monitor Board schematic diagram in Section VI. (Test point pins/designations are not provided on the Monitor Board PCBA.)

4.3.3.4 EVDT Diagnostic Test

The EVDT diagnostic test is a part of the stand alone SILVER Diagnostic System. The purpose of the test is to provide the functional analysis of the EVDT and its associated Terminal Controller PCBA. The test leads to a conclusion pointing out the malfunctioning parts or confirming the operability of the unit.

The test is divided into 10 groups. The option to execute any given group is provided.

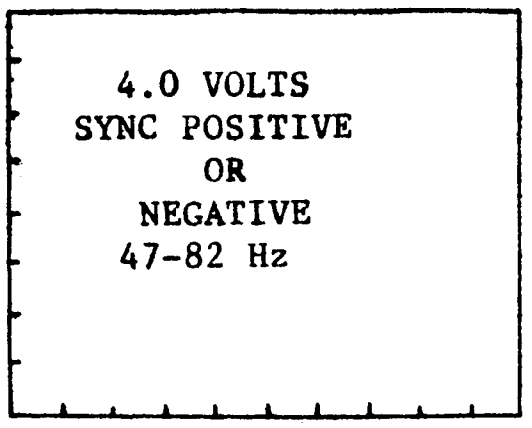
Group 1 - is designed to check extensively the Controller PCBA and EVDT display functions.

Group 2 thru 8 - test extensively the keyboard circuitry (both the Extended Run Time option and Operator Interventon option must be selected for these groups to operate). These tests will check all keyboard types supported by Basic Four except a Katakana keyboard.

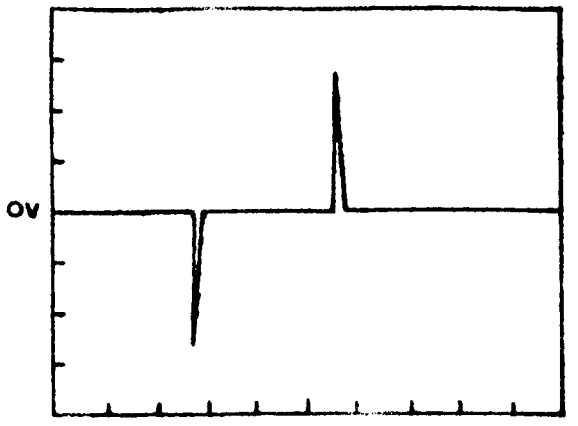
Group 9 - checks the remaining functions of the EVDT, namely the CRT display, ESCAPE/CLEAR key, the speaker assembly, and CRT intensity. It also contains the quick and simple keyboard test. The Operator Intervention option must be selected in order to execute this group.

Group 10 - checks the printer port interface of the EVDT. It is executed only on the EVDT with the serial printer actually configured as a "slave" printer. The printer status is not checked in these tests.

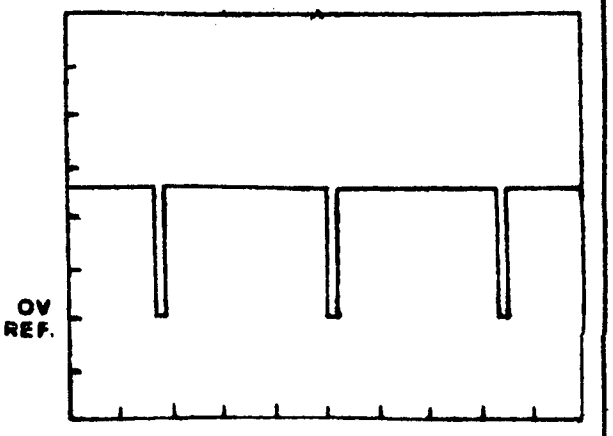
While the test is being run, errors found will be displayed on the video display screen. When the test is completed a readout will be displayed (printout if requried) stating what tests were run, errors found and possible fault locations. One pass of the EVDT Diagnostic Test takes approximately 15 minutes, if no Operator Intervention or Extended Run Time options are selected.



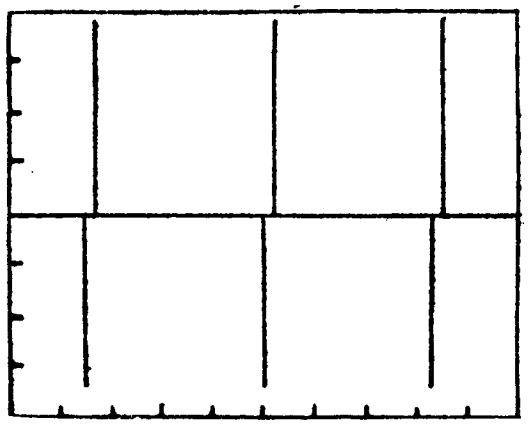
TP1



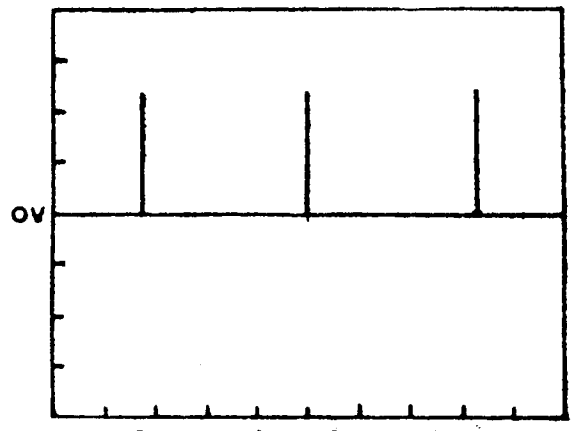
TP2-1.0V/DIV,DC,0.2ms/DIV



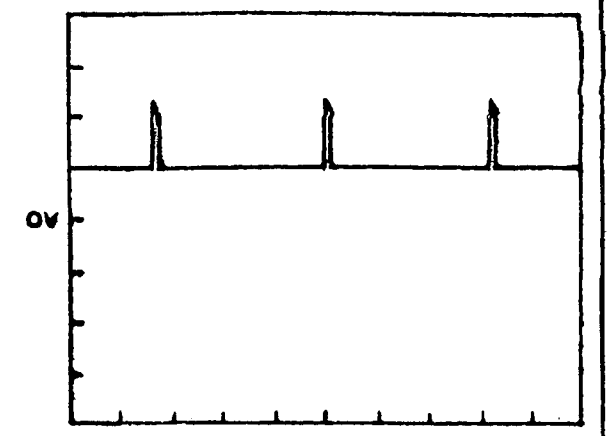
TP3-2V/DIV,DC,5ms/DIV



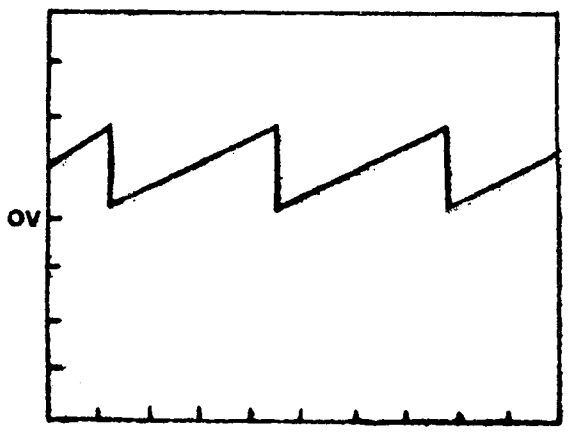
TP4-0.2V/DIV,AC,5ms/DIV



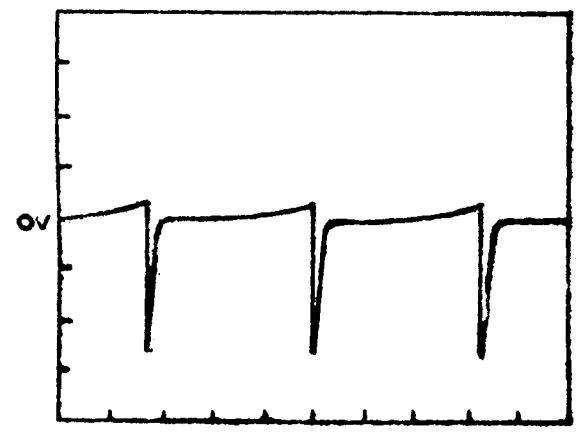
TP5-0.IV/DIV,AC,5ms/DIV



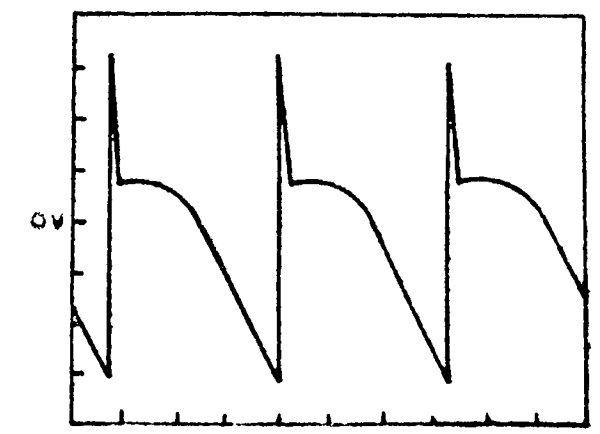
TP6-10V/DIV,DC,5ms/DIV



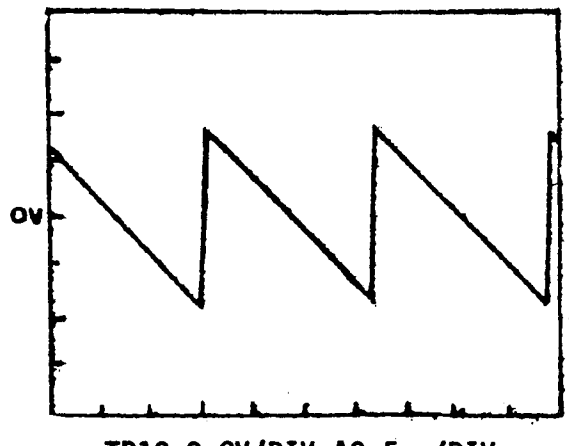
TP7-5V/DIV,DC,5ms/DIV



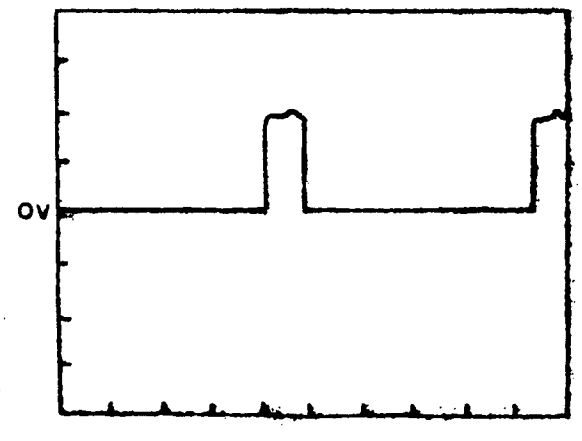
TP8-0.IV/DIV,AC,5ms/DIV



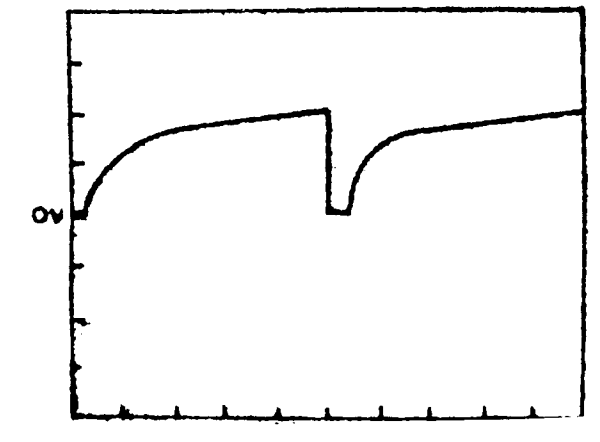
TP9-IV/DIV,AC,5ms/DIV



TP10-0.2V/DIV,AC,5ms/DIV



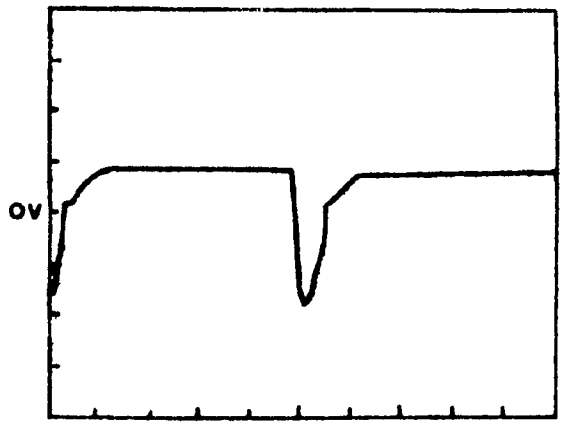
TP11-2V/DIV,DC,10uS/DIV



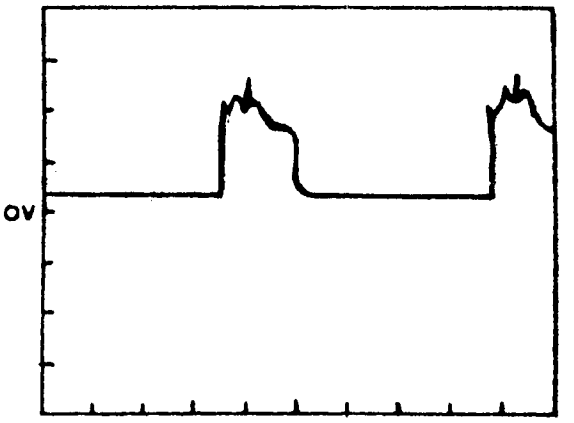
TP12-5V/DIV,DC,10uS/DIV

8070-50

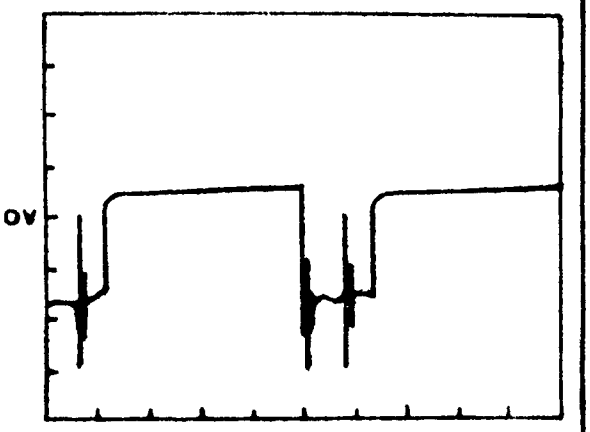
Figure 4-5. Monitor Board Waveforms (sheet 1 of 2)



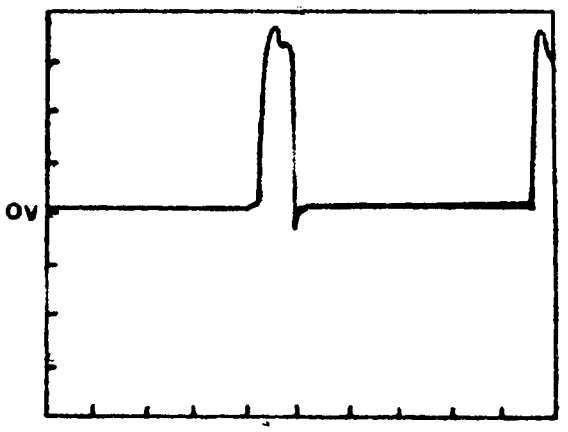
TP13-1V/DIV,DC,10uS/DIV



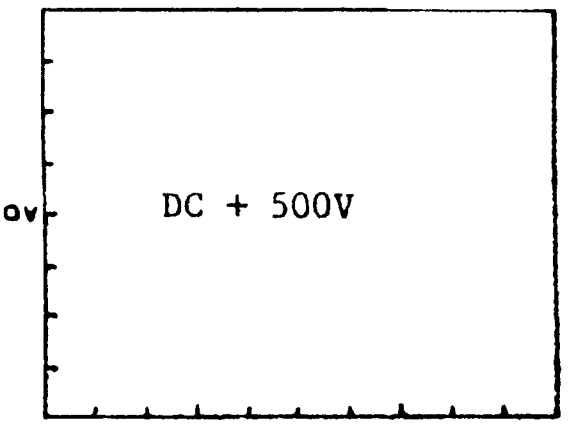
TP14-0.5/DIV,DC,10uS/DIV



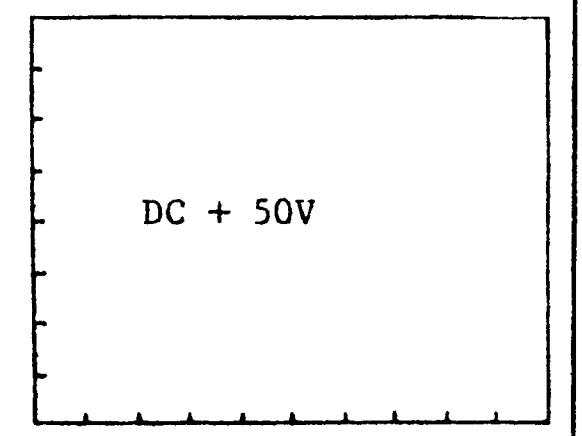
TP15-2V/DIV,DC,10uS/DIV



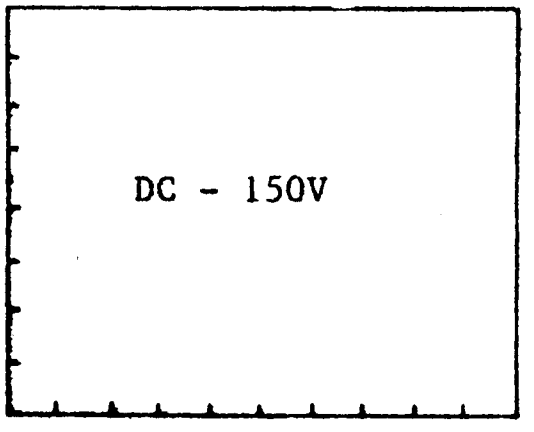
TP16-50V/DIV,DC,10uS/DIV



TP17



TP18



TP19

TP20-50V/DIV,DC,10uS/DIV

8070-51

Figure 4-5. Monitor Board Waveforms (sheet 2 of 2)

4.3.3.5 BASS System Level Diagnostic Tests

The five BASS tests which exercise the EVDT directly are %V01 thru %V05. This series of tests typically take less than 30 minutes to perform and can be invaluable in quickly locating problems in the EVDT. Tests %V04 and %V05 are especially useful in locating intermittent problems. Each of the five tests is described as follows:

1. %V01 - Keyboard Echo Test - This test should be run when it appears that the EVDT keyboard is not operating properly. The program informs the operator that it expects a certain character to be entered. The entered character is echoed if it is a printable character. Two more lines are used to show the hexadecimal equivalent of the input. To indicate a sequence break, a third line displays an asterisk (*) whenever the entry is not the expected entry.

2. %V02 - Control Interaction Test - Performs full function test for all Model 4309/7270/7280 EVDT types. The initiating display is run through the various function tests, and the user is queried as to the nature of the device's reaction to the test. If the individual test fails, the user may select a retry of the test.

3. %V03 - EVDT Exerciser - This test checks that all printable characters can be displayed. A test line consiting of all printer defined characters is displayed on every EVDT line.

4. %V04 - EVDT Scrolling Test - Checks ability of the EVDT to scroll characters without alteration. Test should be run in the event that scrolling appears to malfunction. It should be run whenever the screen appears to be dropping or inserting characters. A test line consisting of all printer defined characters is scrolled from the bottom line to the top line and then read by the EVDT under CPU control. Altered characters are logged. The test line is rotated by one character, and the test is repeated until each character of the test line has appeared in the first position.

5. %V05 - EVDT Print @ Test (Position Control) - Checks ability of the EVDT to do "@ position" control to any place on screen. A full screen image is constructed using the "@ position" control for each byte displayed. The test pattern is then read on a line by line basis and checked against the target pattern. Altered characters are jogged. Proper functioning of the scrolling operation is a prerequisite for the test. Scrolling errors will cause a failure of this test.

SECTION V

REMOVAL/REPLACEMENT/SPARE PARTS

5.1 INTRODUCTION

This section contains disassembly and parts removal/replacement procedures for the Model 4309 EVDT. This section also contains an illustrated parts list with PC board layouts and exploded views, as applicable.

5.2 GENERAL DISASSEMBLY

The following procedures provide access to the internal subassemblies of the video display assembly and the keyboard assembly.

WARNING

Turn off the EVDT power switch and remove the power cord from the ac outlet before removing the rear housing of the video display assembly. Failure to do so may result in severe shock, which can be fatal, or may result in serious damage to the equipment. Always discharge the CRT anode to ground with a grounding strap before removing any subassemblies.

5.2.1 Rear Housing Removal

1. Disconnect the keyboard connector from the front of the video display assembly. Move the keyboard out of the immediate work area. Disconnect the power-cord connector from the video display assembly.

2. Place the video display assembly face down on a clean flat surface, preferably covered by a soft cloth or clean plastic sheet.

3. Use a Phillips screwdriver and loosen, but do not remove, the four (4) screws securing the rear housing to the frame of the video display assembly. Lift the rear housing up and off the display assembly.

4. Carefully place the video display assembly in an upright position.

5. Discharge the CRT anode.

5.2.2 Keyboard Housing Removal

1. Switch off power at the video display assembly. Remove the keyboard connector from the front of the display assembly.

2. Turn the keyboard over and remove four (4) screws that secure the housing to the base.

3. Remove the housing.

NOTE

Some keyboards have the keyboard assembly mounted on the base with captive nuts protruding through the base.

5.3 REMOVAL/REPLACEMENT PROCEDURES

The following procedures provide detailed instructions for removal and replacement of the modular subassemblies, including the CRT.

5.3.1 CRT Safety Precautions

1. ALWAYS discharge the CRT anode to ground before working inside the display unit.

2. ALWAYS wear approved safety glasses.

3. NEVER handle the CRT roughly.

   a. DO NOT scratch the CRT.

   b. DO NOT strike the CRT with hard or sharp objects.

   c. DO NOT handle the CRT by the neck. Use both hands to hold the CRT across the widest dimension.

   d. DO NOT rest the CRT on the neck. Stand the CRT face down on a clean flat surface.

   e. DO NOT allow a hot soldering iron to touch the CRT.

4. Store defective CRTs in original shipping container.

5. Replacement (spare) CRTs should be kept in their shipping containers until needed.

5.3.2 Disposal of Defective CRTs

Defective CRTs, which are to be destroyed, should be tightly packed and sealed in a strong cardboard container. The CRT should be pierced, through the container, using a sharp instrument. This method of disposal prevents accidents occurring to unsuspecting disposal-collection personnel.

5.3.3 CRT Removal and Replacement

1. Turn off power and disconnect power cord from outlet and video display assembly.
2. Disconnect the keyboard.
3. Remove rear housing from the video display assembly (paragraph 5.2.1).
4. Discharge CRT anode to ground.
5. Remove front bezel.
6. Disconnect connector on rear of CRT neck.
7. Disconnect the green ground wire connecting the CRT grounding spring to the monitor board.
8. Remove the CRT anode cap.
9. Disconnect the CRT yoke assembly cable at the monitor board.
10. Remove the corner mounting hardware which secures the CRT to the plastic chassis, and carefully remove the CRT through the front of the chassis.

NOTE

Some terminals have the CRT mounted on the back side of the front corner mounts, making it necessary to remove the CRT through the rear of the chassis. In such cases it will be necessary to remove the monitor board before attempting to remove the CRT.

11. To replace the CRT, use the foregoing procedure in reverse order.
12. Refer to Section IV for CRT (video) adjustment procedures.

5.3.4 Monitor Board PCBA Removal and Replacement

1. Turn off power and disconnect power cord from outlet and video display assembly.

2. Disconnect the keyboard.

3. Remove rear housing from the video display assembly (paragraph 5.2.1).

4. Discharge CRT anode to ground.

5. Disconnect the following cables or wires:

   a. Monitor board to logic board.

   b. Monitor board to CRT socket.

   c. Monitor board to CRT yoke assembly.

   d. CRT anode cap.

   e. Green ground wire to CRT ground spring.

6. Remove the monitor board by carefully pinching the tip of each corner mounting post and pulling the post out of the mounting hole.

7. To replace a monitor board, use the foregoing procedure in reverse order.

8. Refer to Section IV for monitor board (video) adjustment procedures.

5.3.5 Power Supply PCBA Removal and Replacement

1. Turn off power and disconnect power cord from ac outlet and video display assembly.

2. Disconnect the keyboard.

3. Remove rear housing from the video display assembly (paragraph 5.2.1).

4. Discharge CRT anode to ground.

5. Disconnect power supply cable from logic board.

6. Remove screws securing power-supply bracket assembly to plastic chassis.

7. Remove the power supply PCBA up through the top of the chassis.

8. To replace a power supply PCBA, use the foregoing procedure in reverse order.

9. Refer to Section IV for Power Supply DC voltage checks.

5.3.6 Logic Board Removal and Replacement

CAUTION

The logic board contains ICs that are extremely sensitive to static discharge. Always discharge the body to ground by hand contact, before removing, handling, or replacing a logic board. Do not allow the logic board to contact any of the CRT deflection circuits, the yoke, or CRT anode, even if the anode is grounded.

1. Turn off power and disconnect power cord from outlet and video display assembly.
2. Disconnect the keyboard.
3. Remove rear housing from the video display assembly (paragraph 5.2.1).
4. Discharge CRT anode to ground.
5. Disconnect power supply connector (J1) from logic board.
6. Disconnect monitor board connector (J3) from logic board.
7. Carefully slide logic board out of chassis.
8. To replace a logic board, use the foregoing procedure in reverse order.

5.4 ILLUSTRATED PARTS LIST

This portion of Section V provides information on the assemblies and component parts of the Model 4309 EVDT. Each parts list is supported by an illustration (figure) that locates the respective assemblies and/or parts. The illustrations may be used as an aid in parts removal and replacement procedures. The parts lists and their associated illustrations are listed in the Illustrated Parts List Index, which includes the figure and table number, title, and page number for each assembly whose parts are listed.

Assemblies and parts which are recommended for stocking in the Field, so as to minimize equipment down time in the event of failure, are designated by a Sorbus Inventory Control Number (ICN).

ILLUSTRATED PARTS LIST INDEX

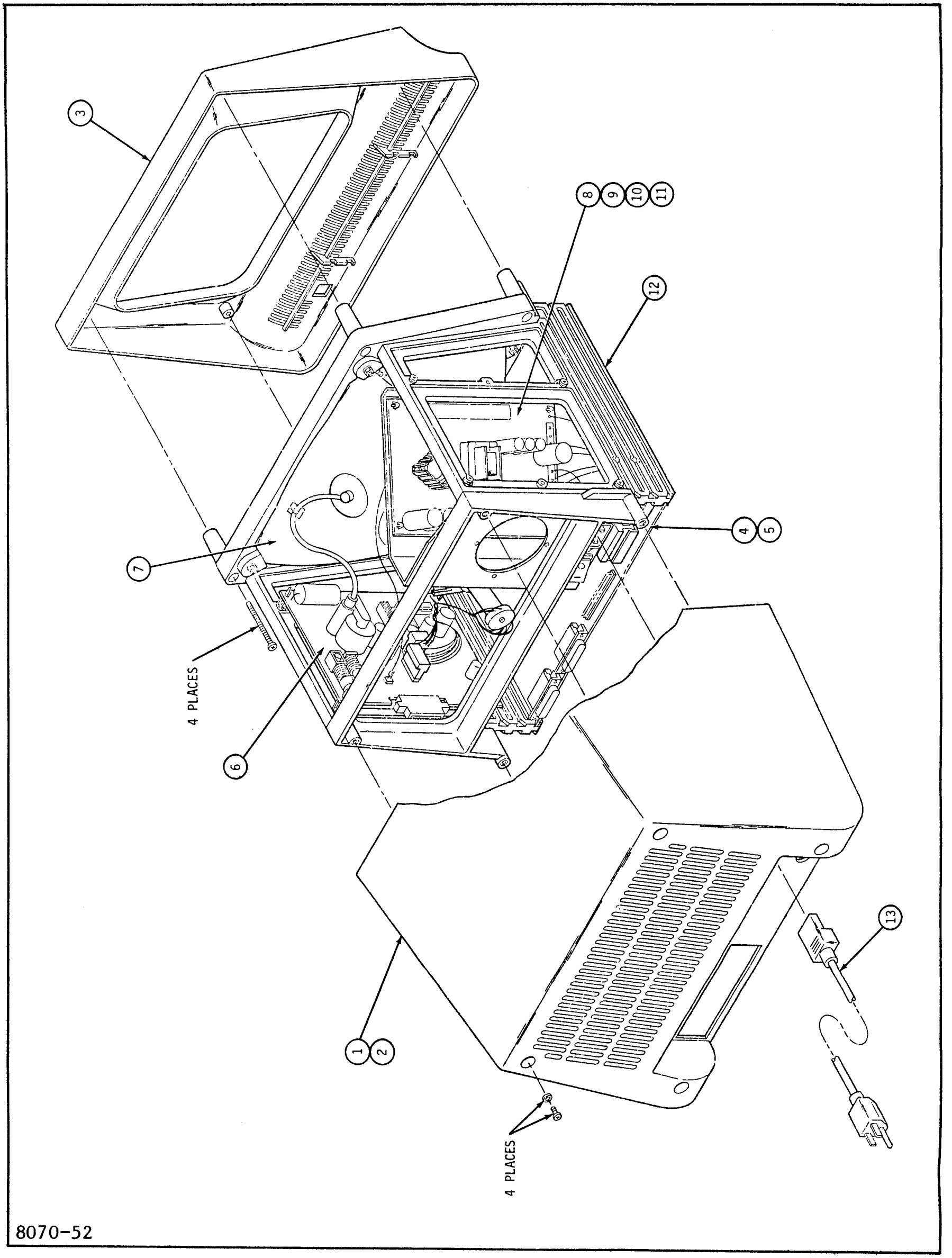


Figure 5-1. EVDT Video Display Assembly

Table 5-1. Parts List, EVDT Video Display Assembly

FIG. 5-1 INDEX NO.	DESCRIPTION	ICN DESIGNATION	PART NO.	QTY.
1	Housing, Rear		05-5006-12	
2	Shield, EMI (not shown)		907369	1
3	Bezel		05-5005-01	1
4	PCBA, Main Logic Board (Refer to table/figure 5-3)	MM780010	903373-001	1
5	Cable Assembly, Logic Board to Monitor Board		907365	1
6	PCBA, Monitor Board (Refer to table/figure 5-4)	MM780020	03-1831-00	1
7	CRT, Green (P31), 12-inch	MM783030	02-1832-00	1
8	PCBA, Power Supply (Refer to table/figure 5-5)	MM783010	02-1302-00	1
9	Bracket, Power Supply		907354	1
10	Switch, Power On-Off		04-6501-00	1
11	Receptacle, Power Cord		04-7600-00	1
12	Chassis Subassembly		907352	1
13	Power Cord, 110 VAC, 3-wire		03-7000-00	1
14	Plate, RS-232 Ports (not shown)		907349	1

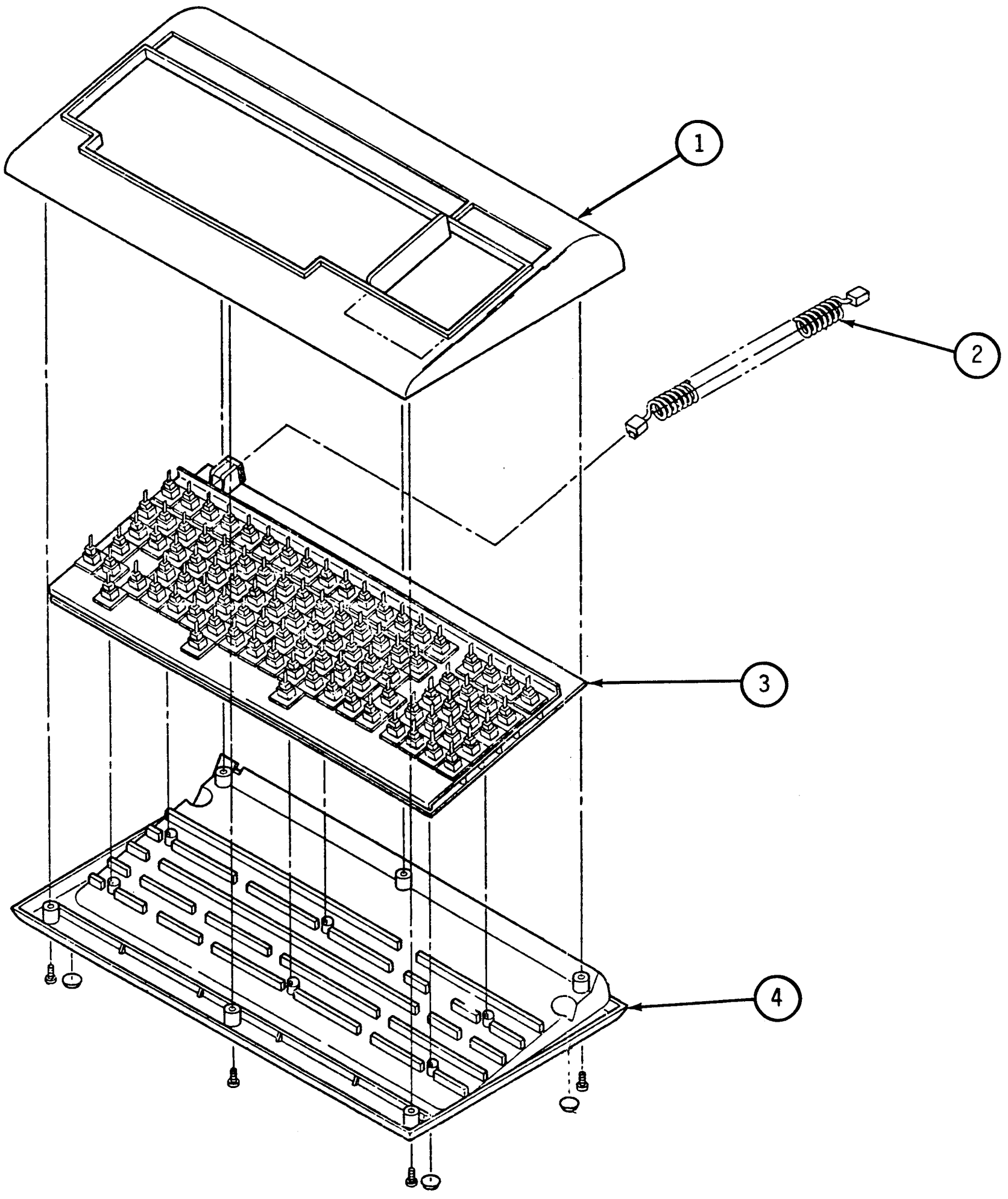
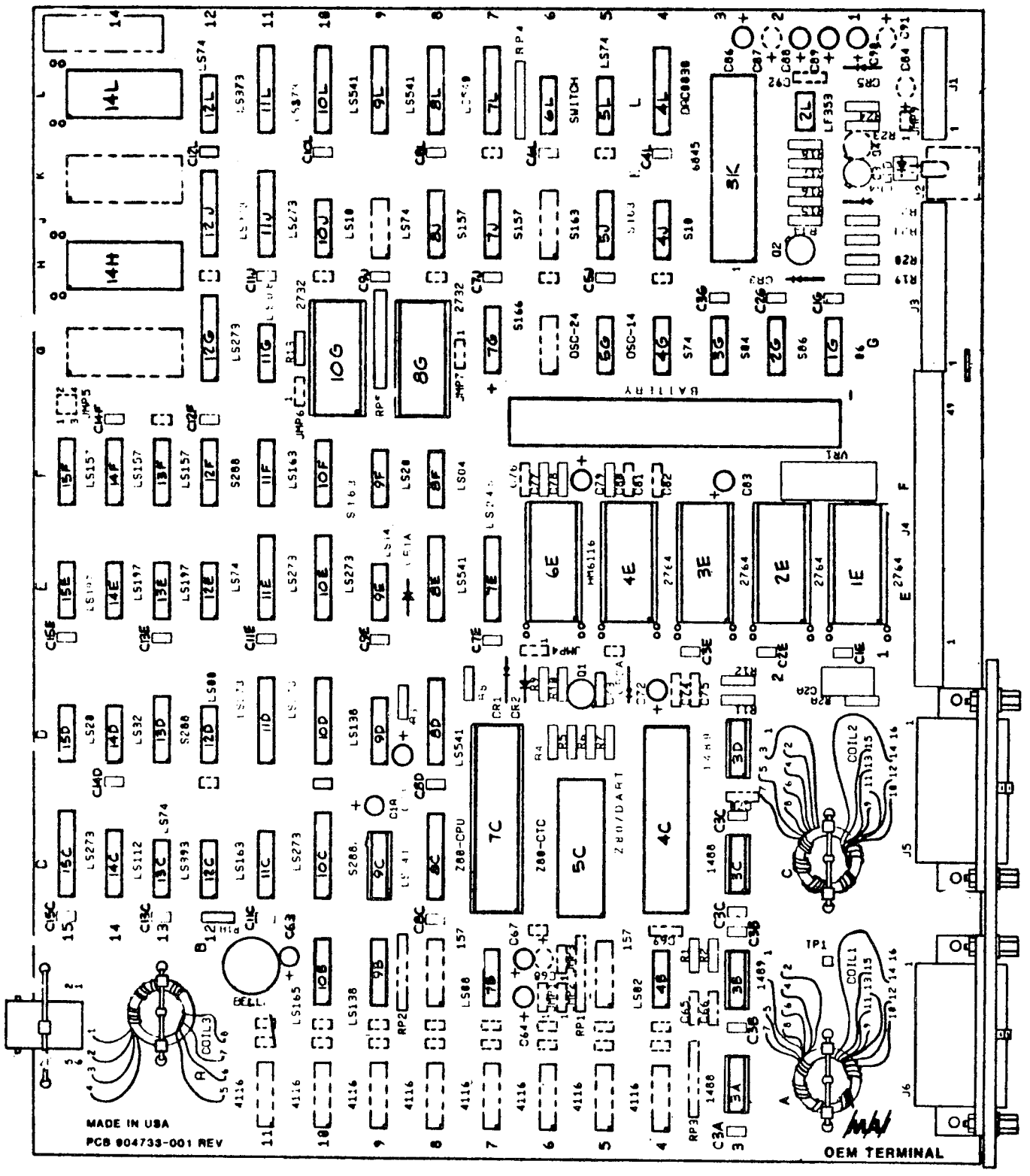


Figure 5-2. EVDT Keyboard Assembly

Table 5-2. Parts List, EVDT Keyboard Assembly

FIG. 5-2 INDEX NO.	DESCRIPTION	ICN DESIGNATION	PART NO.	QTY.
	Keyboard Assembly, Domestic	MM783020	400433-001	
	Keyboard Assembly, German	TBD	400432-001	
	Keyboard Assembly, Spanish	TBD	400435-001	
1	Housing, Keyboard	-	-	1
2	Cable, Keyboard	TBD	03-7001-00	1
3	PCBA, Keyboard (Refer to table/figure 5-6)	TBD	65-02574-XXX	1
4	Base, Keyboard	-	-	1



8070-54

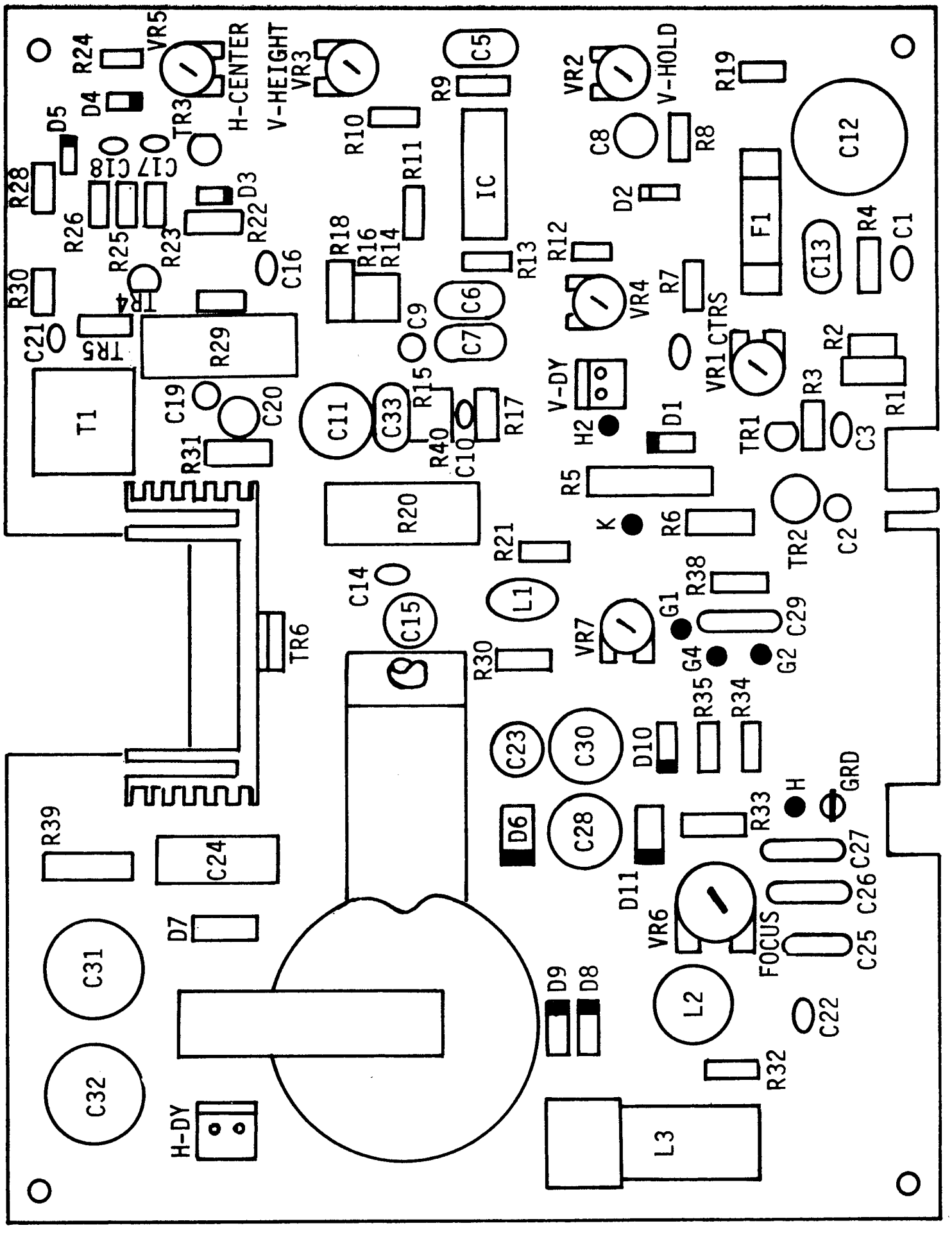
Figure 5-3. Main Logic Board PCBA

Table 5-3. Parts List, Main Logic Board PCBA, MM780010

PART NUM	QTY	PART DESCRIPTION	REMARKS
903373-001	1	PCB LCGIC	REV A
101709	1	IC 74LS00 QUAD 2-IN NAND	12D
101710	1	IC 74LS02 QUAD 2 IN NOR	4B
101541	1	IC 74S04 INVERTER HEX	3G
101316	1	IC 7406 QUAD BUFFER/DRIVER	1G
101711	2	IC 74LS08 QUAD 2INP AND	11G,7B
101712	1	IC 74LS10 TRIPLE INPUT NAND GATE	10J
101672	2	IC 74LS20 POS NAND GATE	15D,9F
101714	1	IC 74LS32 QUAD 2-IN OR	14D
101741	5	IC 74LS74 DUAL D-TYPE POS EDG-TRIG F/F	12L,5L,13C,12E,9J
101657	3	IC 74LS157 QUAD 2-1 LINE DATA SELEC/MUX	14F,15F,13F
101719	2	IC 74LS138 3-8 LINE DECODER/DEMULTIPLEX	9D,9B
161114-001	1	IC SHIFT REGISTER 8 BIT PARALL TO SERIAL	10B
161112-001	3	BINARY COUNTER 4 STAGE PRESETTABLE	14E,15E,13E
161023	9	IC 74LS273 OCTAL D-TYPE FLIP-FLOP	10D,12G,12J,10C,11D, 10E,15C,11E,11J
161013	2	IC 74LS373 OCTAL D-TYPE LATCH 3-STATE	10L,11L
161028	1	IC 74LS393 DUAL 4 BIT BINARY COUNTER	12C
101613	2	IC MC1488L QUAD LINE DRIVER	3A,3C
101612	2	IC MC1489L QUAD LINE RECEIVER	3B,3D
162002-002	1	IC Z80A 8 BIT MICRO-P	7C
162001-001	1	IC Z80A-CTC COUNTER/TIMER CRCT	5C
161105-001	1	Z-80 DUAL ASYNC RECEIVER/TRANSMITTER	4C
162035-001	1	IC, CRT CONTROLLER	3K
101537	1	IC 74166 8 BIT SHIFT REGISTER	7G
165016-001	4	IC 2732 4KX8 EPROM 450 NS	2E,3E,4E,1E
161107-001	2	IC RAM STATIC 2KX8 150NS	14L,14H
101656	1	IC 74LS04 HEX INVERTER	8F
101543	1	IC 74S10 GATE TRIPLE 3-INPUT NAND	4J
101629	1	IC SN74S74 DUAL D-TYPE FLIP/FLOP	4G
101673	1	IC 74S86 QUAD 2-INPUT EXCLUSIVE OR GATE	2G
101783	1	IC 74LS112 DUAL J-K EDG-TRIG FLIP/FLOP	14C
101633	2	IC SN74S157 QUAD 2-1 LINEDATA SELECT/MUX	7J,8J
101642	3	IC 74LS163 BINARY COUNTER SYNC	10F,11F,11C
101721	1	IC 74S163 SYSCHRONOUS 4 BIT COUNTER	5J
161066-001	1	IC 74LS245 OCTAL BUS XCVR	7E
165017-001	3	IC 74S288, PROM, 32 X 8	9C,12F,13D
161113-001	1	IC, OCTAL BUS DRIVER, INVERTING,3-STATE	7L
161110-001	1	8-BIT DOUBLE BUFFERED D-TO-A CONVERTER	4L
161109-001	1	OP AMP DUAL JFET WIDE BAND	2L
132014-001	1	IC REGULATOR -5.0V 0.5A TO220 PCK.G	VR1
111000-107	1	RES CARBON FILM .25W 5% 75 OHM	R17
111000-048	6	RES CARBON FILM .25W 5% 220 OHM	R9,10,18,23,7,14
111000-008	1	RES CARBON FILM .25W 5% 820 OHM	R22
111000-052	1	RES CARBON FILM .25W 5% 470 OHM	R15
111000-011	10	RES CARBON FILM .25W 5% 1.2K OHM	R13,8,24,19,16,20,21
111000-060	4	RES CARBON FILM .25W 5% 4.7K OHM	R1,2,11,12
111000-030	1	RES CARBON FILM .25W 5% 560 OHM	R3
119001-003	1	RES NTWK SIP 8 PIN 7 RES 4.7K OHM	RP4
103000-004	1	CAP MICA DIPPED 33PF 5% 300V	C73
104007-001	34	CAP CERAMIC Z5U DIP .1UF 20% 50V	C3A,3B(2 REQ'D),3C(2 REQ'D),8C,11C,13C, 15C,8D,14D,1E,2E,3E, 7E,9E,11E,13E,15E, 12F,14F,1G,2G,3G,5J, 7J,9J,11J,4L,6L,8L, 10L,12L,10D

Table 5-3. Parts List, Main Logic Board PCBA, MM780010 (continued)

ITEM	PART NUM	CTY	PART DESCRIPTION	REMARKS
	102004-004	8	CAP TANT 4.7UF 10% 50V	C64,67,71,72,83,79, 88,90
	180051-001	1	TRANSFORMER,BALUN	COIL 3
	108022-001	2	CAP ALUM ELECT MINI 47UF +50 -10% 10V	C63,89
	153002-001	1	TRANSDUCER,AUDIO 98DB	BELL
	161104-001	5	IC OCTAL BUFFER/LINE DRIVER	8C,8D,8E,8L,9L
	111000-039	1	RES CARBON FILM .25W 5% 22 OHM	R5
	141007-002	1	TRANS PNP SWITCHING/AMPLIFIER 2N3906	Q1
	101220	4	DIODE IN4148 SILICON SWITCHING	CR1,2,3,1A
	325005-003	4	SOCKET IC DIP FOUR-LEAF CONT GOLD 14 POS	3A,3B,3C,3D
	325005-010	1	SOCKET IC DIP FOUR-LEAF CONT GOLD 40 POS	7C
	325005-004	1	SOCKET IC DIP FOUR-LEAF CONT GOLD 16 POS	9C
	325005-001	7	SOCKET IC DIP FOUR-LEAF CONT GOLD 24 POS	1E,2E,3E,4E,6E,8G, 10G
	161108-001	1	IC RAM STATIC 2KX8 CMOS 200NS	6E
	315052-001	1	CONTACT PCB SOLDER MOUNT MALE .250X.032	1G
	104003-002	3	CAP CERAMIC X7R .1UF 10% 50V	C80,77,78
	150001-020	1	OSCILLATOR CRYSTAL CLOCK - 14.7456 MHZ	OSC 14
	161117-001	1	DIODE ZENER 8.7V 250MW LOW NOISE	CR4
	161118-001	1	LED RED DIFFUSED T1L220	LED
	101306	2	TRANS NPN SILICON 2N2222A	Q2,3
	108022-002	1	CAP ALUM ELECT MINI 220UF +50 -10% 10V	C86
	331005-001	1	SWITCH SPST DIP 7 POS	6L
	180052-001	2	TRANSFORMER,BLAUN	COIL 1,COIL 2
	165016-004	1	IC 2732 2KX8 EPROM 250 NS	10G
	300005-005	1	CONN HDR .045 W/LOCK .156 CTS 7 POS	J1
	300089-001	1.	CONN MODULAR JACK PC BRD MOUNT 6 POS	J7
	300005-013	1.	CONN HDR .045 W/LOCK .156 CTS 11 POS	J3
	300032-015	1.	CONN HDR .025SQ DBL ROW .100 CTS 50 POS	J4
	313222-003	2.	CONN RT ANG PCB 25 SOCKET	J5,6
	161015	1.	IC 74LS14 HEX SCHMITT TRIGGER INVERTER	9E
	111000-063	1.	RES CARBON FILM .25W 5% 10K OHM	R2A
	104003-012	1.	CAP CERAMIC X7R .047UF 20% 200V	C2A
	183005-001	1.	BATTERY,NICAD,2.4 VOLT	4F
	208000-001	4.	RIVET BLIND .116DX.188L ALUM	J5,6
	907349-001	1.	PLATE CONNECTOR PCBA-2 CUTOUTS	J5,6
	100114	4.	SCREWLOCK FEMALE 4-40 THD D TYPE	J5,6
	221019-001	7.	CABLE TIE 0.62 DIA BUNDLE	*
	119004-002	1.	RES NTWK SIP LP 10 PIN 9 RES 4.7 OHM	RP5



8070-55

Figure 5-4. Monitor Board PCBA

Table 5-4. Parts List, Monitor Board PCBA, MM780020

PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION
38195-3913	Capacitor, 390 pF, 5%, 50V	C1
28149-4791	Capacitor, 4.7 uF, +75, -10%, 25V	C2, C9
31115-1031	Capacitor, 0.01 uF, 5%, 50V	C3, C14, C21
31115-1021	Capacitor, 0.001 uF, 5%, 50V	C4, C16
31115-1541	Capacitor, 0.15 uF, 5%, 50V	C5
31115-1041	Capacitor, 0.1 uF, 5%, 50V	C6, C7, C13, C33
28148-1011	Capacitor, 100 uF, +50, -10%, 25V	C8
38115-3303	Capacitor, 33 pF, 5%, 50V	C10
28128-1021	Capacitor, 1000 uF, +50, -10%, 10V	C11
28148-1021	Capacitor, 1000 uF, +50, -10%, 25V	C12
28148-2211	Capacitor, 220 uF, +50, -10%, 25V	C15
31115-2221	Capacitor, 0.0022 uF, 5%, 50V	C17, C18, C22
28169-1091	Capacitor, 1 uF, +75, -10%, 50V	C19
28118-2211	Capacitor, 220 uF, +50, -10%, 6.3V	C20
28128-4711	Capacitor, 470 uF, +50, -10%, 10V	C23
33166-2731	Capacitor, 0.027 uF, 10%, 630V	C24
39587-1038	Capacitor, 0.01 uF, 20%, 1KV	C25, C26, C27, C29
28198-4701	Capacitor, 47 uF, +50, -10%, 100V	C28
28000-0001	Capacitor, 3.3 uF, +75, -10%, 250V	C30
28449-6891	Capacitor, 6.8 uF, 20%, 25V	C31
28449-1001	Capacitor, 10 uF, 20%, 25V	C32
150019-001	Diode, 1N4002	D1, D2
150020-001	Diode, 1S2473	D3, D4, D5
150029-001	Diode, RGP20B	D6
150022-001	Diode, RGP20J	D7

Table 5-4. Parts List, Monitor Board PCBA, MM780020 (continued)

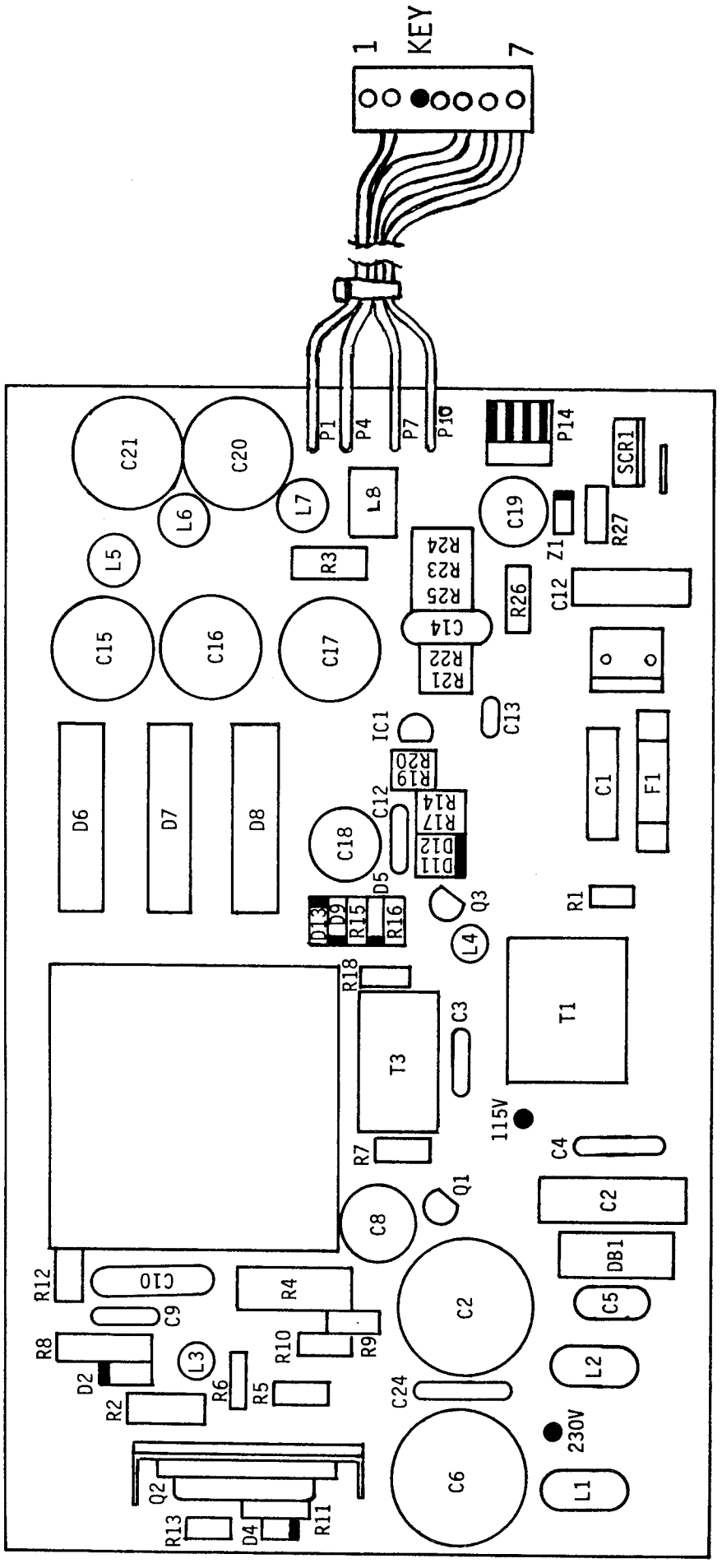
PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION
150021-001	Diode, RGP10J	D8, D11
150023-001	Diode, RGP10G	D9
150024-001	Diode, Zener, 1N4752A, 33V	D10
490002-001	Fuse, 2A, 250V, Fast-Blow	F1
452003-001	Inductor, 4.7 uH, 5%	L1
463001-001	Inductor, Variable (WIDTH)	L2
463002-001	Inductor, Variable (HORIZONTAL LINEARITY)	L3
170014-001	IC, TDA1170N	IC1
22245-3304	Resistor, 33 ohms, 5%, 1/2W	R1
22225-1003	Resistor, 10 ohms, 5%, 1/4W	R2, R19
22225-1023	Resistor, 1K, 5%, 1/4W	R3, R4
23265-8216	Resistor, 820 ohms, 5%, 2W	R5
22245-2214	Resistor, 220 ohms, 5%, 1/2W	R6
22225-3323	Resistor, 3.3K, 5%, 1/4W	R7, R22
22225-4723	Resistor, 4.7K, 5%, 1/4W	R8
22225-1043	Resistor, 100K, 5%, 1/4W	R9
22225-1843	Resistor, 180K, 5%, 1/4W	R10
22225-7543	Resistor, 750K, 5%, 1/4W	R11
22225-6233	Resistor, 62K, 5%, 1/4W	R12
22225-6243	Resistor, 620K, 5%, 1/4W	R13
22225-5633	Resistor, 56K, 5%, 1/4W	R14, R15
22225-6833	Resistor, 68K, 5%, 1/4W	R16
22225-8233	Resistor, 82K, 5%, 1/4W	R17

Table 5-4. Parts List, Monitor Board PCBA, MM780020 (continued)

PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION
22245-1094	Resistor, 1 ohm, 5%, 1/2W	R18
24146-5083	Resistor, 0.5 ohm, 10%, 3W	R20
22225-1523	Resistor, 1.5K, 5%, 1/4W	R21, R27
22225-4323	Resistor, 4.3K, 5%, 1/4W	R23
22225-1033	Resistor, 10K, 5%, 1/4W	R24
22225-8223	Resistor, 8.2K, 5%, 1/4W	R25
22225-2223	Resistor, 2.2K, 5%, 1/4W	R26
22225-3333	Resistor, 33K, 5%, 1/4W	R28
24146-8203	Resistor, 82 ohms, 10%, 3W	R29
22245-1014	Resistor, 100 ohms, 5%, 1/2W	R30
22245-1594	Resistor, 1.5 ohms, 5%, 1/2W	R31
22225-2023	Resistor, 2K, 5%, 1/4W	R32
22225-1853	Resistor, 1.8M, 5%, 1/4W	R33
22225-1033	Resistor, 10K, 5%, 1/4W	R34, R35, R38
22225-7533	Resistor, 75K, 5%, 1/4W	R36
22225-2243	Resistor, 220K, 5%, 1/4W	R37
22225-1595	Resistor, 1.5 ohms, 5%, 1W	R39
22225-3394	Resistor, 3.3 ohms, 5%, 1/4W	R40
470001-001	Transformer, Horizontal Drive	T1
470002-001	Transformer, Flyback	T2
140017-001	Transistor, NPN, 2N3904	TR1
140018-001	Transistor, NPN, 2N3053	TR2
140019-001	Transistor, NPN, 2SC536	TR3, TR4
1400020-001	Transistor, NPN, 2SC2314	TR5
1400038-001	Transistor, NPN, 2SD823	TR6

Table 5-4. Parts List, Monitor Board PCBA, MM780020 (continued)

PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION
251012-001	Potentiometer, 500 ohms, 20%, 0.1V (CONTRAST)	VR1
251011-001	Potentiometer, 250K, 20%, 0.1V (V-HEIGHT, HOLD)	VR2, VR3
251009-001	Potentiometer, 100K, 20%, 0.1V (V-LINEARITY)	VR4
251013-001	Potentiometer, 2.2K, 20%, 0.1V (H-CENTER)	VR5
251010-001	Potentiometer, 5M, 20%, 0.25V (FOCUS)	VR6
251009-001	Potentiometer, 100K, 20%, 0.1V (BRIGHTNESS)	VR7



8070-56

Figure 5-5. Power Supply PCBA

Table 5-5. Parts List, Power Supply PCBA, MM783010

PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION
NOTE All Part No's are TBD	Capacitor, 0.01 uF, 20%, 250V	C1, C2
	Capacitor, 4700 pF, 20%, 400V	C3, C4
	Capacitor, 0.22 uF, 20%, 250V	C5
	Capacitor, Electrolytic, 100 uF, 20%, 250V	C6, C7
	Capacitor, Electrolytic, 200 uF, +50, -10%, 10V	C8
	Capacitor, 470 pF, 20%, 3KV	C9
	Capacitor, 0.10 uF, 20%, 1KV	C10, C11
	Capacitor, 0.22 uF, 20%, 100V	C12, C14
	Capacitor, 0.022 uF, 20%, 50V	C13
	Capacitor, Electrolytic, 1000 uF, +50, -10%, 25V	C15, C16, C17
	Capacitor, Electrolytic, 330 uF, +100, -20%, 16V	C18, C19
	Capacitor, Electrolytic, 470 uF, +50, -10%, 25V	C20
	Capacitor, 2200 uF, +50, -10%, 16V	C21
	Capacitor, 0.22 uF, 20%, 250V	C24
	Diode, Rectifier, RGP10A	D1
	Diode, Rectifier, RGP10J	D2
	Diode, Rectifier, RGP10M	D3
	Diode, Rectifier, 1N4001GP	D4
	Diode, 1N4606	D5
	Rectifier Assembly	D6
	Rectifier Assembly	D7
	Rectifier Assembly	D8
	Diode, Rectifier, RGP10B	D9

Table 5-5. Parts List, Power Supply PCBA, MM783010 (continued)

PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION
	Diode, 1N4606	D11
	Diode, 1N4606	D12
	Diode, Rectifier	D13
	Bridge Rectifier, KBP10	DB1
	Fuse, 2A, 250V	F1
	IC, Regulator	IC1
	Filter Choke Coil Assembly	L1
	Filter Choke Coil Assembly	L2
	Base Choke, 2.2 uH	L3
NOTE	Choke, 1.5 mH	L4
All Part No's are TBD	Filter Choke Coil Assembly	L5
	Filter Choke Coil Assembly	L6
	Choke Coil Electrolytic, 470 uF,	L7
	Transistor, NPN, SD467	Q1
	Transistor, Power	Q2
	Transistor, PNP	Q3
	Thermistor, 4 ohms, 10%	R1
	Resistor, Carbon Film, 330K, 5%, 1/2W	R2
	Resistor, Metal Oxide Film, 220 ohms, 5%, 1W	R3
	Resistor, Metal Oxide Film, 33 ohms, 5%, 1/2W	R4
	Resistor, Carbon Film, 1K, 5%, 1/4W	R5
	Resistor, Carbon Film, 27 ohms, 5%, 1/4W	R6
	Resistor, Carbon Film, 68 ohms, 5%, 1/4W	R7

Table 5-5. Parts List, Power Supply PCBA, MM783010 (continued)

PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION
	Resistor, Carbon Film, 10 ohms, 5%, 1/4W	R9, R10
	Resistor, Metal Film, 0.75 ohms, %5, 1W	R11
	Resistor, Metal Film, 1 ohm, 5%, 1W	R12
	Resistor, Carbon Film, 5.6 ohms, 5%, 1/4W	R13
	Resistor, Carbon Film, 68 ohms, 5%, 1/4W	R14
	Resistor, Carbon Film, 270 ohms, 5%, 1/2W	R15, R16
NOTE	Resistor, Carbon Film, 8.2 ohms, 5% 1/4W	R17
All Part No's are TBD	Resistor, Carbon Film, 560 ohms, 5%, 1/4W	R18
	Resistor, Carbon Film, 56 ohms, 5%, 1/4W	R19, R20
	Resistor, Carbon Film, 12K, 5%, 1/4W	R21
	Resistor, Carbon Film, 470 ohms, 5%, 1/4W	R22
	Resistor, Metal Film, 4.7K, 2%, 1/4W	R23
	Resistor, Carbon Film, 68K, 5%, 1/4W	R24
	Resistor, Metal Film, 22K, 2%, 1/4W	R25
	Resistor, Metal Film, 2.7K, 2%, 1/4W	R26
	Resistor, Carbon Film, 12 ohms, 5%, 1/4W	R27
	SCR C122U	SCR1
	Common Mode Transformer Assembly	T1
	Power Transformer Assembly	T2
	Control Transformer Assembly	T3
	Diode, Zener, 5.6V, 5%, 1W	Z1

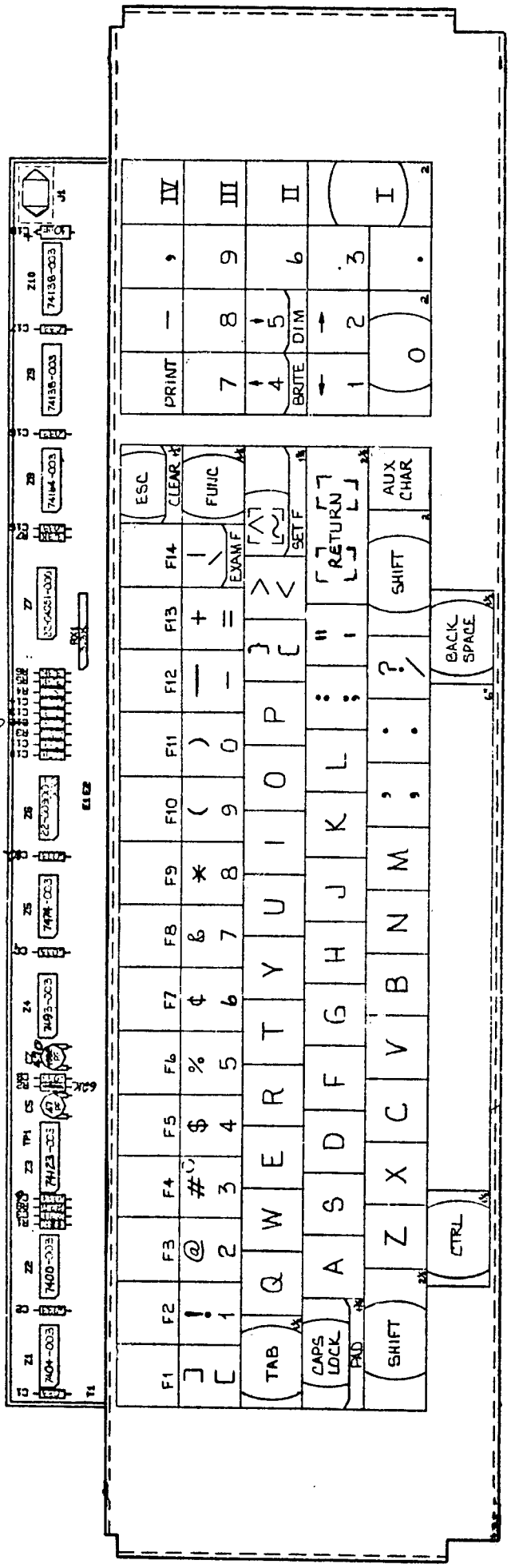


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Figure 5-6. Keyboard PCBA

Table 5-6. Keyboard PCBA

PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION
65-02547-001	Keyboard PCBA, International	
65-02547-002	Keyboard PCBA, Domestic	
32-00333-004	Capacitor, 0.03 uF	C1, C2, C4, C6, C8, C9, C11-C17
27-00220-006	Capacitor, 22 pF	C3
28-00470-004	Capacitor, 47 pF	C5
28-00102-004	Capacitor, 470 pF	C7
28-00221-004	Capacitor, 220 pF	C10
32-00106-010	Capacitor, Electrolytic, 10 uF	C18
39-00585-000	Connector, Keyboard Cable	J1
-	Resistor Pack, 33K (8 places)	RX1
-	Resistor, 11K	R1
-	Resistor, 62K	R2
-	Resistor, 680 ohms	R3
-	Resistor, 3.3K	R4, R5, R6, R7
-	Resistor, 82 ohms	R8
-	Resistor, 1K	R9
7404-003	IC, Hex Inverter, 74LS04	Z1
7400-003	IC, Quad Nand Gates, 74LS00	Z2
74123-003	IC, Dual Monostable Multivibrator, 74LS123	Z3
7493-003	IC, 4-Bit Binary Counter, 74LS93	Z4
7474-003	IC, Dual D-Type Flip-Flop, 74LS74	Z5
22-00900-000	IC, Proprietary	Z6
22-04051-000	IC, Proprietary	Z7
74164-003	IC, 8-Bit Serial-to-Parallel Shift Register, 74LS164	Z8

Table 5-6. Keyboard PCBA (continued)

PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION
74138-003	IC, 3-to-8 Line Decoder, 74LS138	Z9, Z10
400436-001	Keycap Kit, Italian	
400437-001	Keycap Kit, French	
400438-001	Keycap Kit, Swedish	
400439-001	Keycap Kit, German	
400440-001	Keycap Kit, Norwegian	
400441-001	Keycap Kit, Danish	
400447-001	Keycap Kit, Domestic	
400448-001	Keycap Kit, Spanish	
61-04031-001	Keyswitch, Domestic RETURN Key, Right Side (with pad - no spring)	
61-04031-002	Keyswitch, Domestic RETURN Key, Left Side (with standard spring - no pad)	
61-04024-001	Keyswitch, Standard 92 Places	
45-00053-030	Spring, Keyswitch, SPACE Bar	
45-00053-070	Spring, Keyswitch, ESCAPE/CLEAR and PRINT Keys	
45-00053-015	Spring, Standard; 88 Places Domestic, 89 Places International	

SECTION VI

REFERENCE DATA

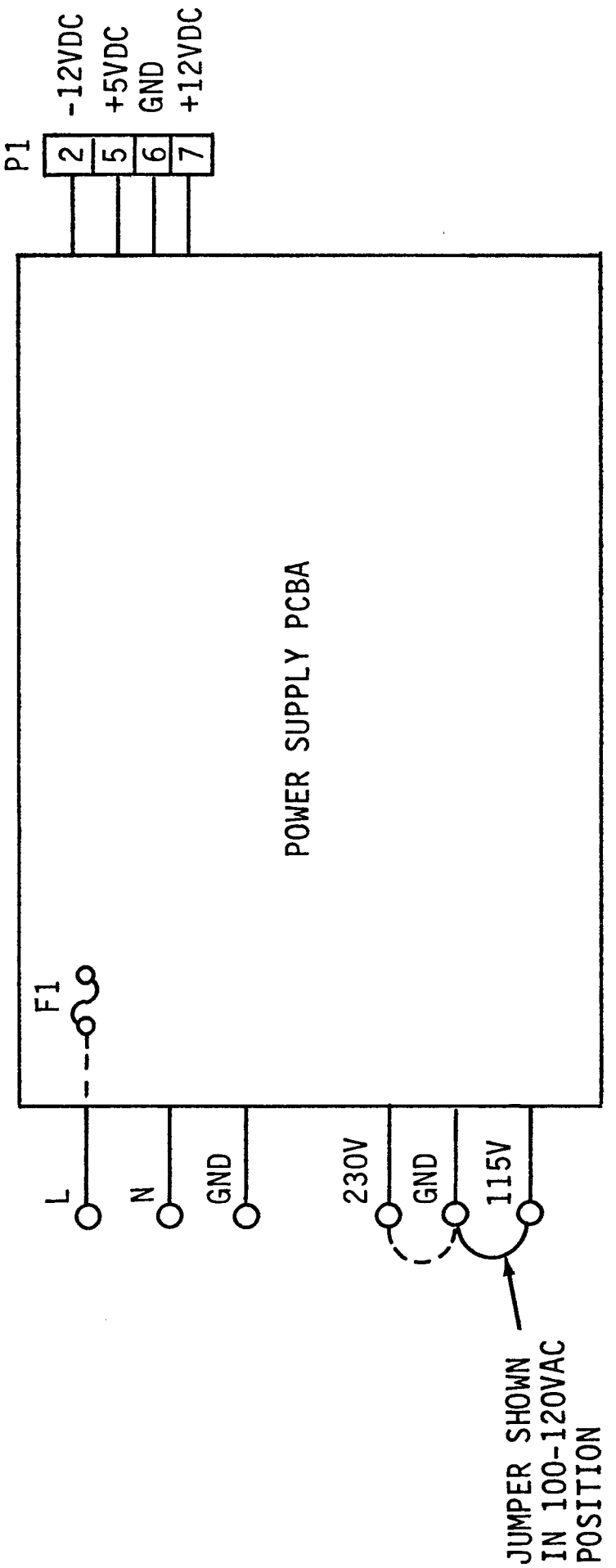

Figure 6-4. Input/Output Diagram, Power Supply PCBA

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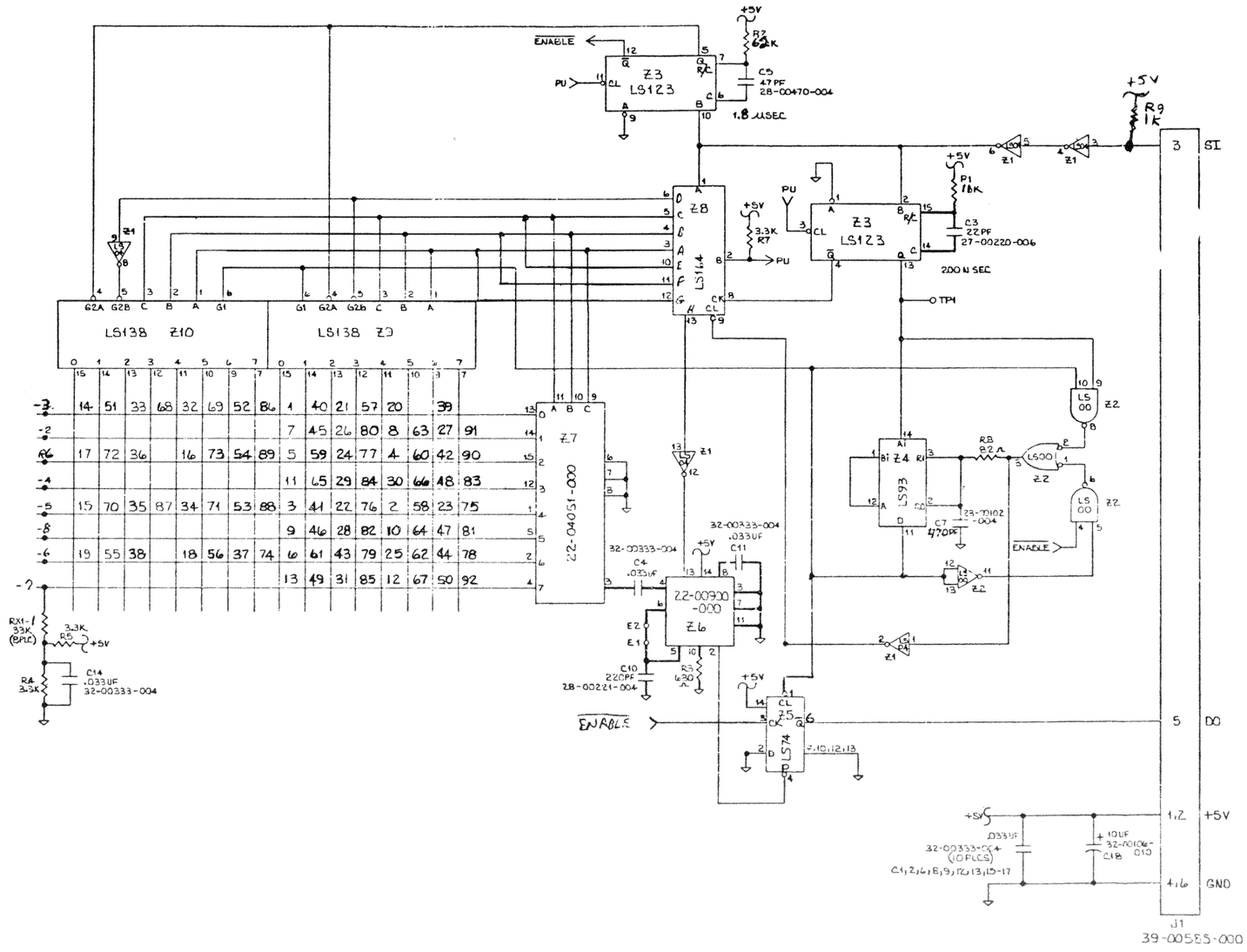

-3	14	51	33	68	32	69	52	86	1	40	21	57	20		39
-2									7	45	26	80	8	63	27	91
-4	17	72	36		16	73	54	89	5	59	24	77	4	60	42	90
-4									11	65	29	84	30	66	48	83
-5	15	70	35	87	34	71	53	88	3	41	22	76	2	58	23	75
-8									9	46	28	82	10	64	47	81
-6	19	55	38		18	56	37	74	6	61	43	79	25	62	44	78
-7									13	49	31	85	12	67	50	92

NOTE: THIS DIAGRAM IS FOR REFERENCE ONLY - REVISION LEVEL WILL NOT BE MAINTAINED

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Figure 6-1. Logic Diagram, Keyboard PCBA

Table 6-1. EVDT to DCE/Host CPU Interface Signals (I/O Port A)

CONN/PIN	SIGNAL	SOURCE	DESCRIPTION
J5-1	None (PROT GND)	EVDT/DCE/Host	Protective (chassis) ground.
J5-2	TXD	EVDT	Transmitted Data - Serial data transmitted to DCE/Host.
J5-3	RXD	DCE/Host	Received Data - Serial data received by EVDT.
J5-4	RTS	EVDT	Request to Send (always true) - Indicates to DCE/Host that data is ready to be transmitted.
J5-5	CTS	DCE/Host	Clear to Send - Indicates that DCE/Host is ready to accept data from EVDT.
J5-6	DSR	DCE/Host	Data Set Ready - Not used by EVDT.
J5-7	GND	EVDT/DCE/Host	Signal Ground (common return).
J5-8	DCD	DCE/Host	Data Carrier Detect - Indicates that DCE/Host is receiving data transmitted by EVDT.
J5-20	DTR	EVDT	Data Terminal Ready (always true) - Indicates that EVDT is ready to transmit or receive data.

Table 6-2. EVDT to Serial Printer Interface Signals (I/O Port B)

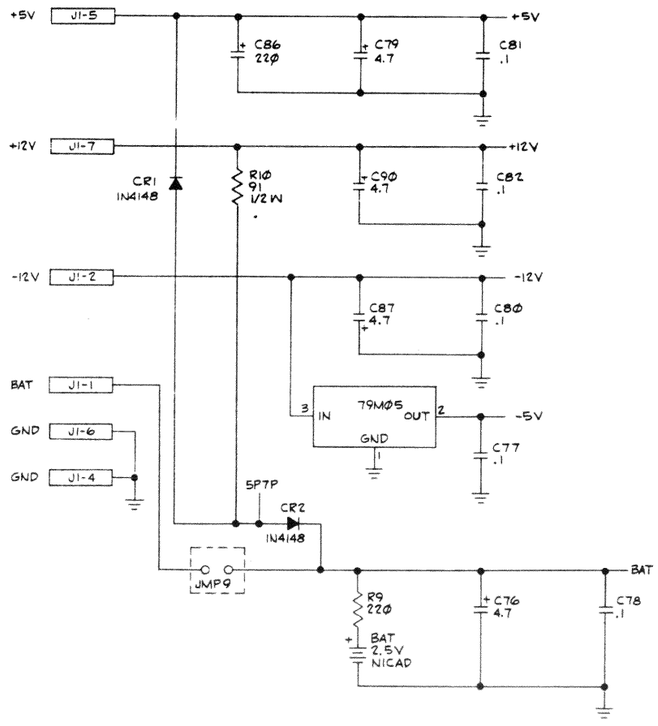
CONN/PIN	SIGNAL	SOURCE	DESCRIPTION
J6-1	None (PROT GND)	EVDT/Printer	Protective (chassis) ground.
J6-2	RXD	Printer	Received Data - Serial data received by EVDT.
J6-3	TXD	EVDT	Transmitted Data - Serial data transmitted to printer.
J6-4	DCD	Printer	Data Carrier Detect - Indicates that printer is receiving data transmitted by EVDT.
J6-5	DTR	EVDT	Data Terminal Ready - Indicates that EVDT is ready to transmit or receive data.

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
RP5	
R24	
C93	
CR6	
Q4	
COIL 3	
LED	
BELL	
J8	
JMP9	

SPARES			
LOCATION	IC TYPE	NO. OF SPARES	PIN NO. OF SPARES
3B	1489	1	(6,4)
7B	74LSØ6	3	(1,2,3)(4,5,6)(11,12,13)
9E	74LS14	2	(1Ø,11)(12,13)
12E	74LS74	1	(8,9,1Ø,11,12,13)
8F	74LSØ4	1	(1,2)

IC POWER DISTRIBUTION CHART			
LOCATION	TYPE	GND	+5V
3A	1488	7	
3B	1489	7	14
4B	74LSØ2	7	14
5B	74157	8	16
7B	74LSØ8	7	14
8B	74157	8	16
9B	74LS138	8	16
1ØB	74LS165	8	16
3C	1488	7	
4C	Z8ØA-DART	31	9
5C	Z8ØA-CTC	5	24
7C	Z8ØA-CPU	29	11
8C	74LS541	1Ø	2Ø
9C	745288	8	16
1ØC	74LS273	1Ø	2Ø
11C	74LS163	8	16
12C	74LS393	7	14
13C	74LS74	7	14
14C	74LS112	8	16
15C	74LS273	1Ø	2Ø
3D	1489	7	14
8D	74LS541	1Ø	2Ø
9D	74LS138	8	16
1ØD	74LS273	1Ø	2Ø
11D	74LS273	1Ø	2Ø
12D	74LSØØ	7	14
13D	745288	8	16
14D	74LS32	7	14
15D	74LS2Ø	7	14
1E	2732/2764	12/14	24/28
2E	2732/2764	12/14	24/28
3E	2732/2764	12/14	24/28
4E	2732/2764	12/14	24/28
6E	HM6116	12	24
7E	74LS245	1Ø	2Ø
8E	74LS541	1Ø	2Ø
9E	74LS14	7	14
1ØE	74LS273	1Ø	2Ø
11E	74LS273	1Ø	2Ø

IC POWER DISTRIBUTION CHART			
LOCATION	TYPE	GND	+5V
12E	74LS74	7	14
13E	74LS197	7	14
14E	74LS197	7	14
15E	74LS197	7	14
8F	74LS04	7	14
9F	74LS2Ø	7	14
1ØF	74LS163	8	16
11F	74LS163	8	16
12F	745288	8	16
13F	74LS157	8	16
14F	74LS157	8	16
15F	74LS157	8	16
1G	74Ø6	7	14
2G	74S86	7	14
3G	74SØ4	7	14
4G	74S74	7	14
7G	74166	8	16
8G	2732	12	24
1ØG	2732	12	24
11G	74LSØ8	7	14
12G	74LS273	1Ø	2Ø
14G	4Ø16	12	24
14H	4Ø16	12	24
4J	745174	7	14
5J	745163	8	16
6J	745163	8	16
7J	745157	8	16
8J	745157	8	16
9J	74LS74	7	14
1ØJ	74LS174	7	14
11J	74LS273	1Ø	2Ø
12J	74LS273	1Ø	2Ø
3K	MC6845	1	2Ø
14K	4Ø16	12	24
4L	DAC0830	1Ø	
5L	74LS74	7	14
7L	74LS54Ø	1Ø	2Ø
8L	74LS541	1Ø	2Ø
9L	74LS541	1Ø	2Ø
1ØL	74LS373	1Ø	2Ø
11L	74LS373	1Ø	2Ø
12L	74LS74	7	14
14L	4Ø16	12	24



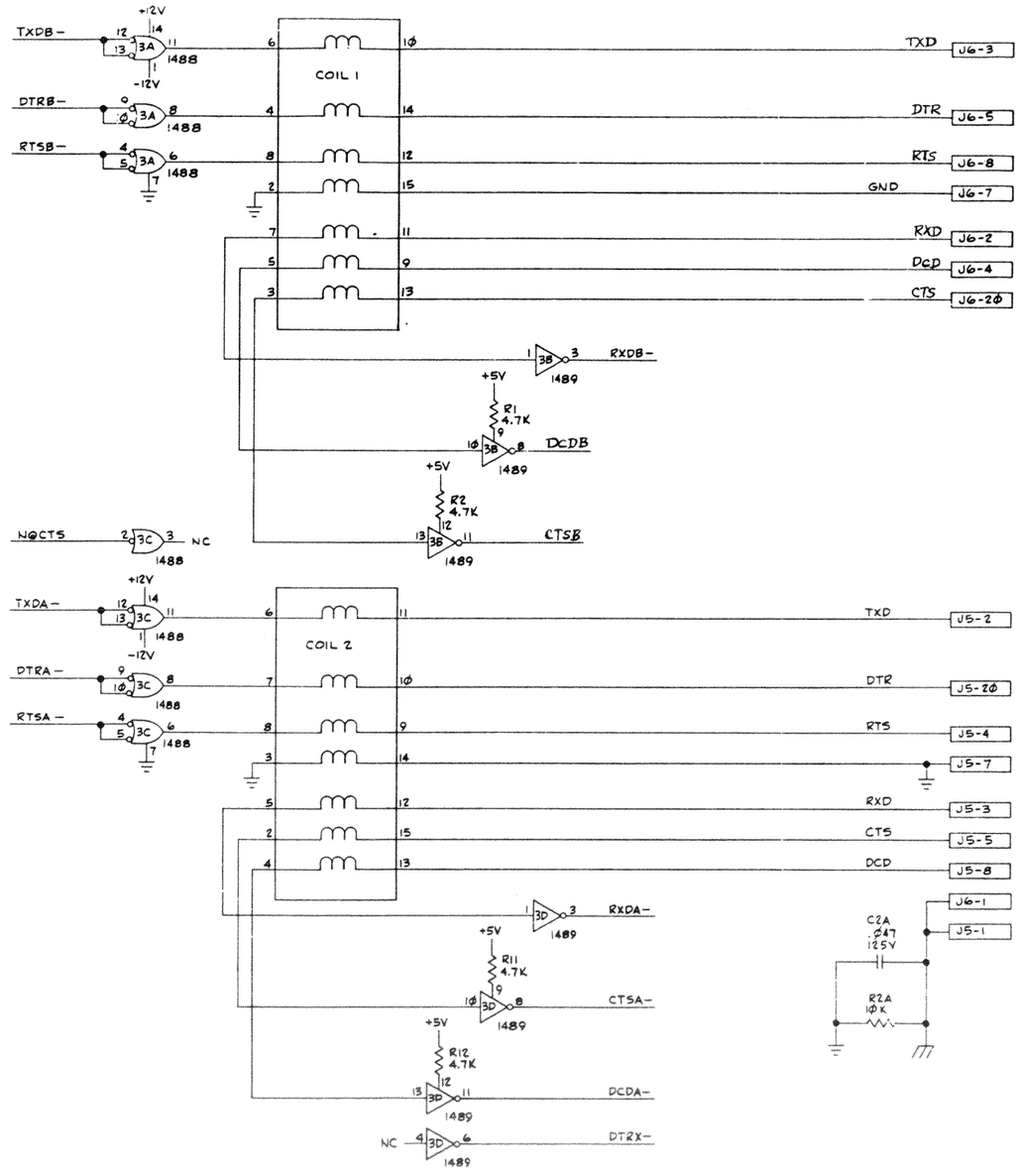
JUMPER TABLE			
LOCATION		STD	FUNCTION
JMP1	1-2		64K OPTIONAL PAGING RAM-VCC (4A-11A)
JMP1	2-3		16K OPTIONAL PAGING RAM-VCC (4A-11A)
JMP2	1-2		64K OPTIONAL PAGING RAM-VDD (4A-11A)
JMP2	2-3		16K OPTIONAL PAGING RAM-VDD(4A-11A)
JMP3	1-2		64K OPTIONAL PAGING RAM-VBB (4A-11A)
JMP3	2-3		16K OPTIONAL PAGING RAM-VBB (4A-11A)
JMP4	1-2		SELECT 4K CMOS NON-VOLATILE RAM (6E)
JMP4	2-3	✓	SELECT 2K CMOS NON-VOLATILE RAM (6E)
JMP5	1-3, 2-4	✓	SELECT 2K HMOS SCREEN RAM (14G-14L)
JMP5	1-3, 3-4		SELECT 4K HMOS SCREEN RAM (14G-14L)
JMP6	1-2	✓	SELECT 4K (2732) CHARACTER GENERATOR EPROM (1ØG)
JMP6	2-3		SELECT 2K (2716) CHARACTER GENERATOR EPROM (1ØG)
JMP7	1-2	✓	SELECT UNDERLINE ATTRIBUTE POSITION-LINE 1Ø
JMP7	2-3		SELECT UNDERLINE ATTRIBUTE POSITION-LINE 9
JMP8			
JMP8			
JMP9	OPEN	✓	SELECT ON BOARD BATTERY
JMP9	1-2		SELECT EXTERNAL BATTERY

8070-59

Figure 6-2. Logic Diagram, Main Logic Board PCBA (Sht. 1 of 12) 903385 Rev. A

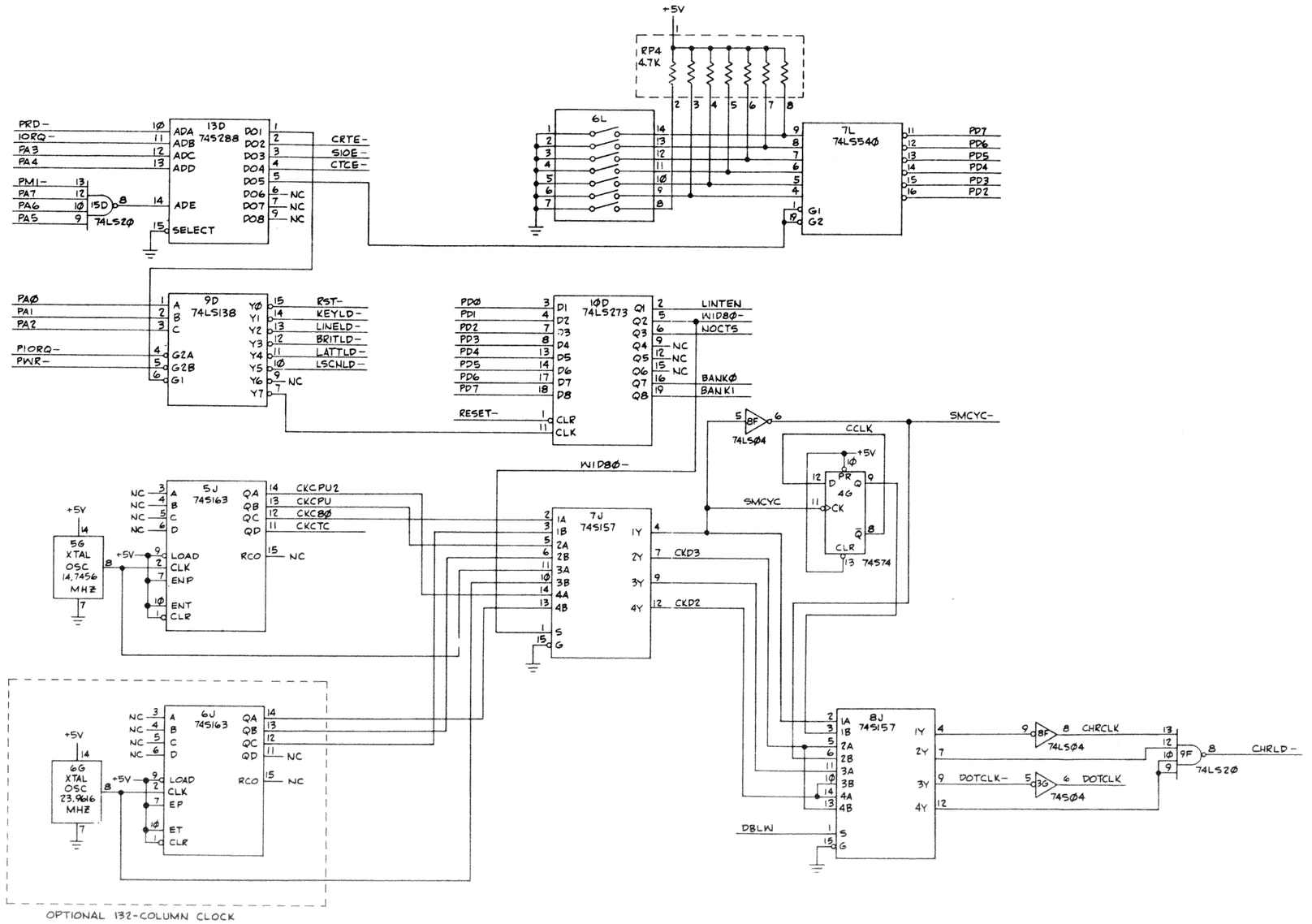
Table 6-2. EVDT to Serial Printer Interface Signals (I/O Port B) (continued)

CONN/PIN	SIGNAL	SOURCE	DESCRIPTION
J6-7	GND	EVDT/Printer	Signal Ground (common return).
J6-8	RTS	EVDT	Request to Send - Indicates to printer that data is ready to be transmitted.
J6-20	CTS	Printer	Clear to Send - Indicates that printer is ready to accept data from EVDT.



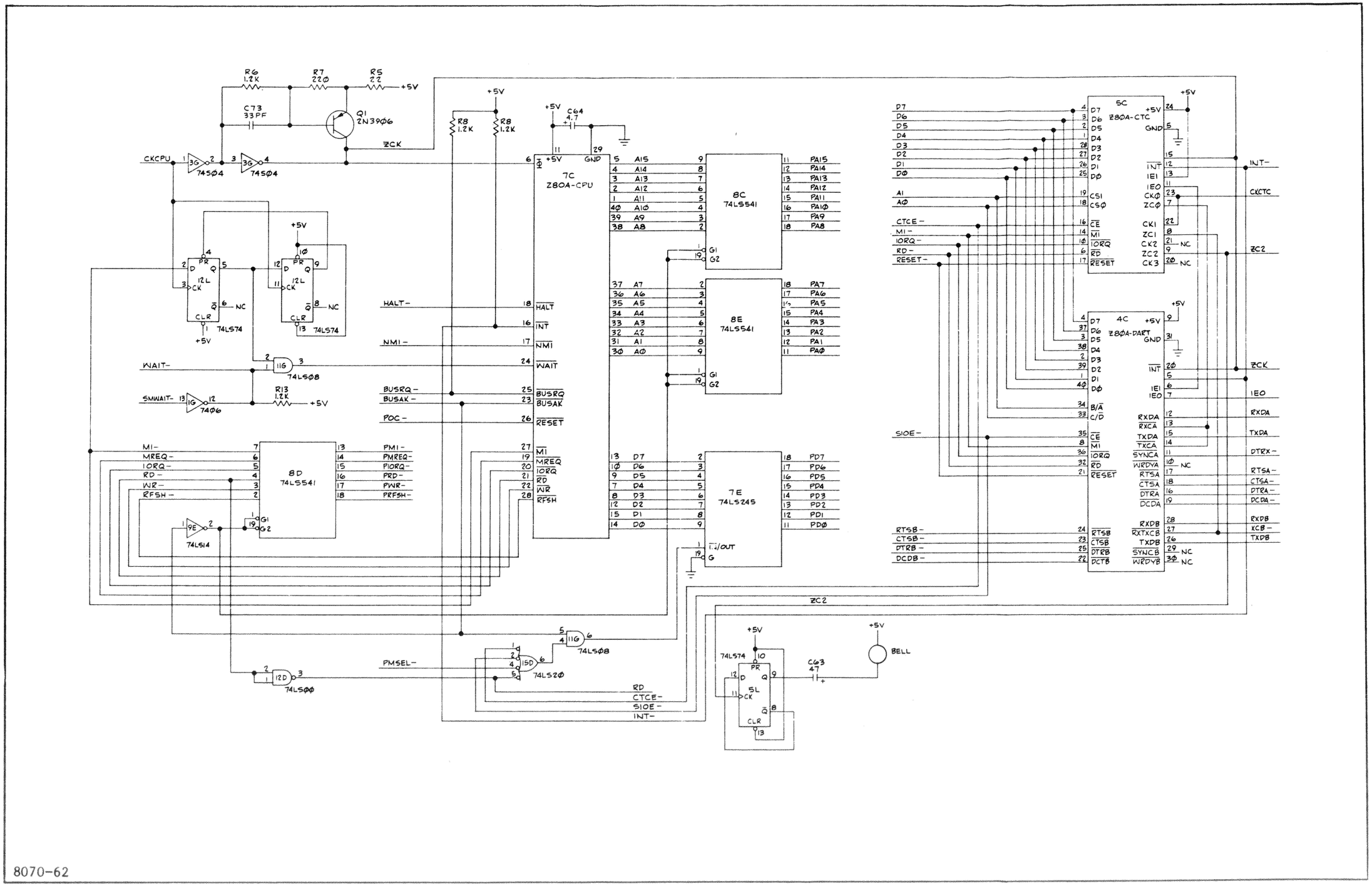
8070-60

Figure 6-2. Logic Diagram, Main Logic Board PCBA (Sht. 2 of 12) 903385 Rev. A



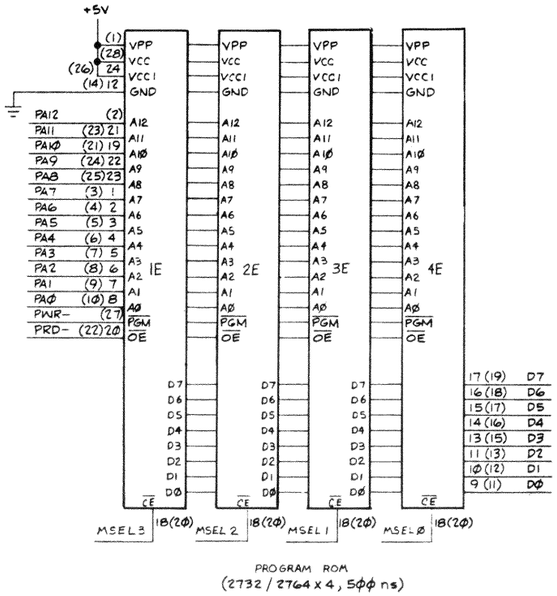
8070-61

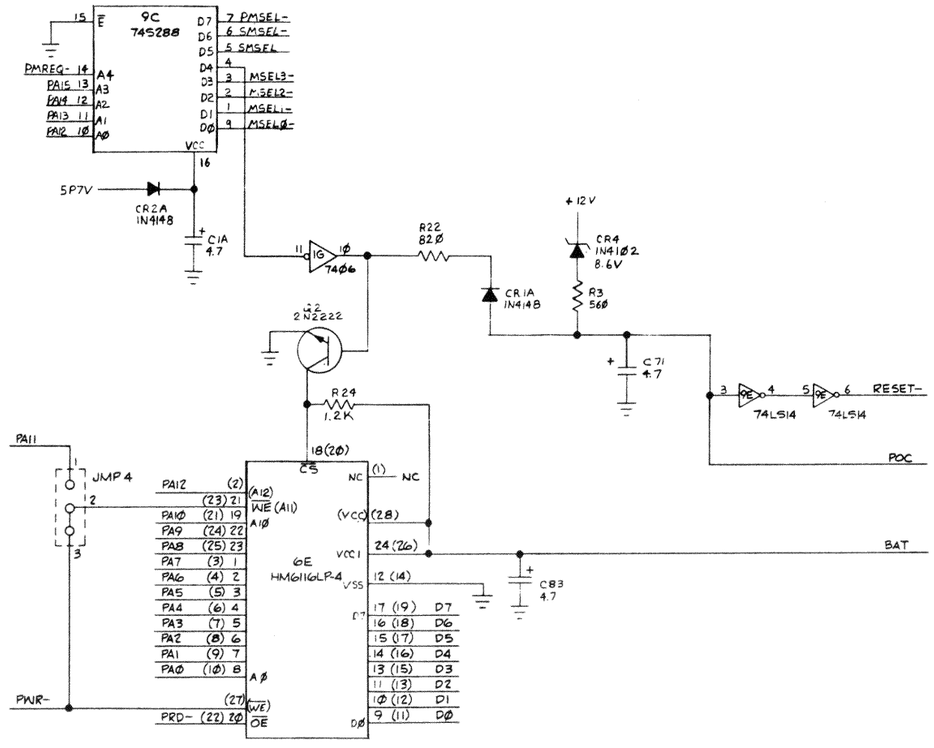
Figure 6-2. Logic Diagram, Main Logic Board PCBA (Sht. 3 of 12) 903385 Rev. A



8070-62

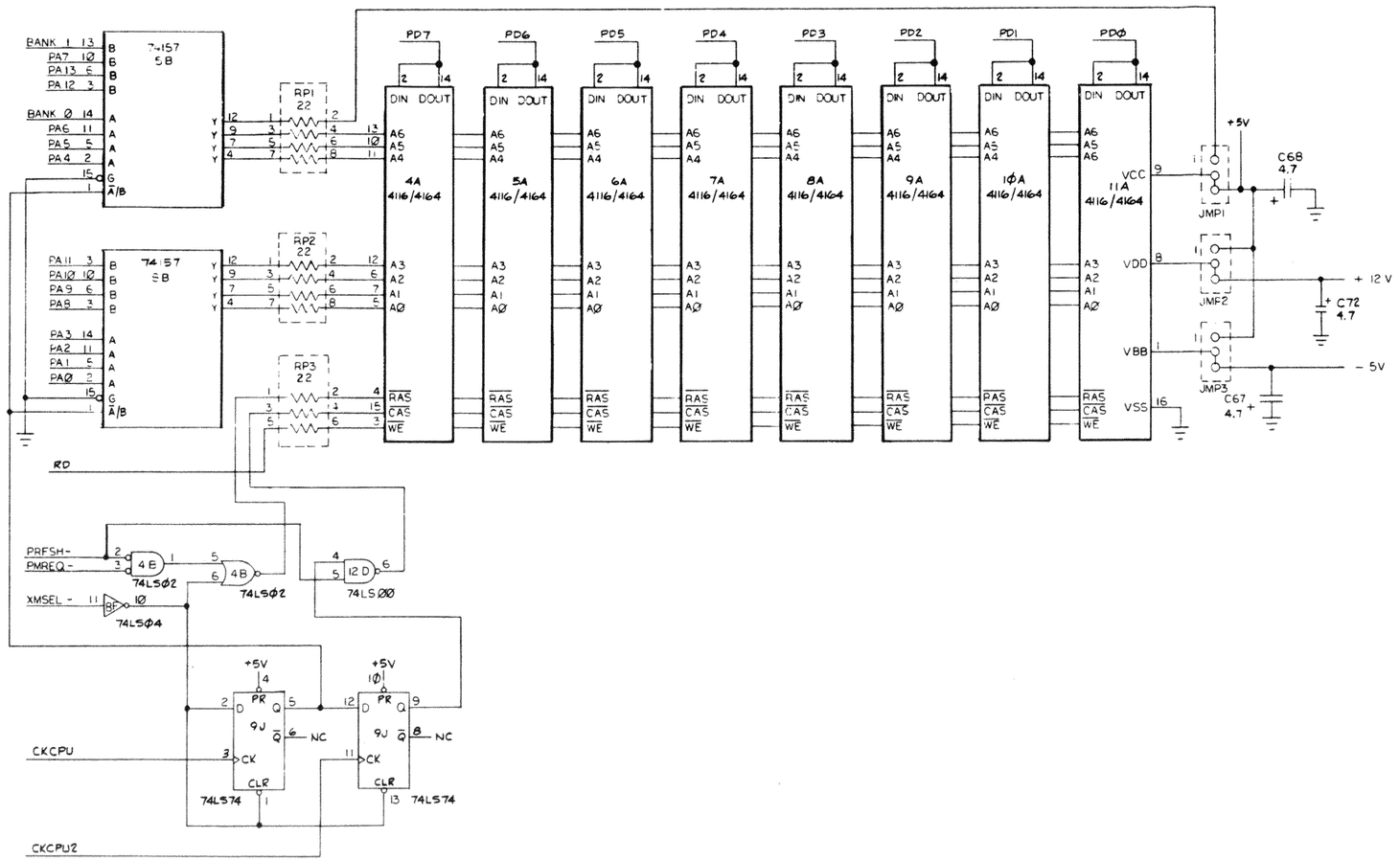
Figure 6-2. Logic Diagram, Main Logic Board PCBA (Sht. 4 of 12) 903385 Rev. A





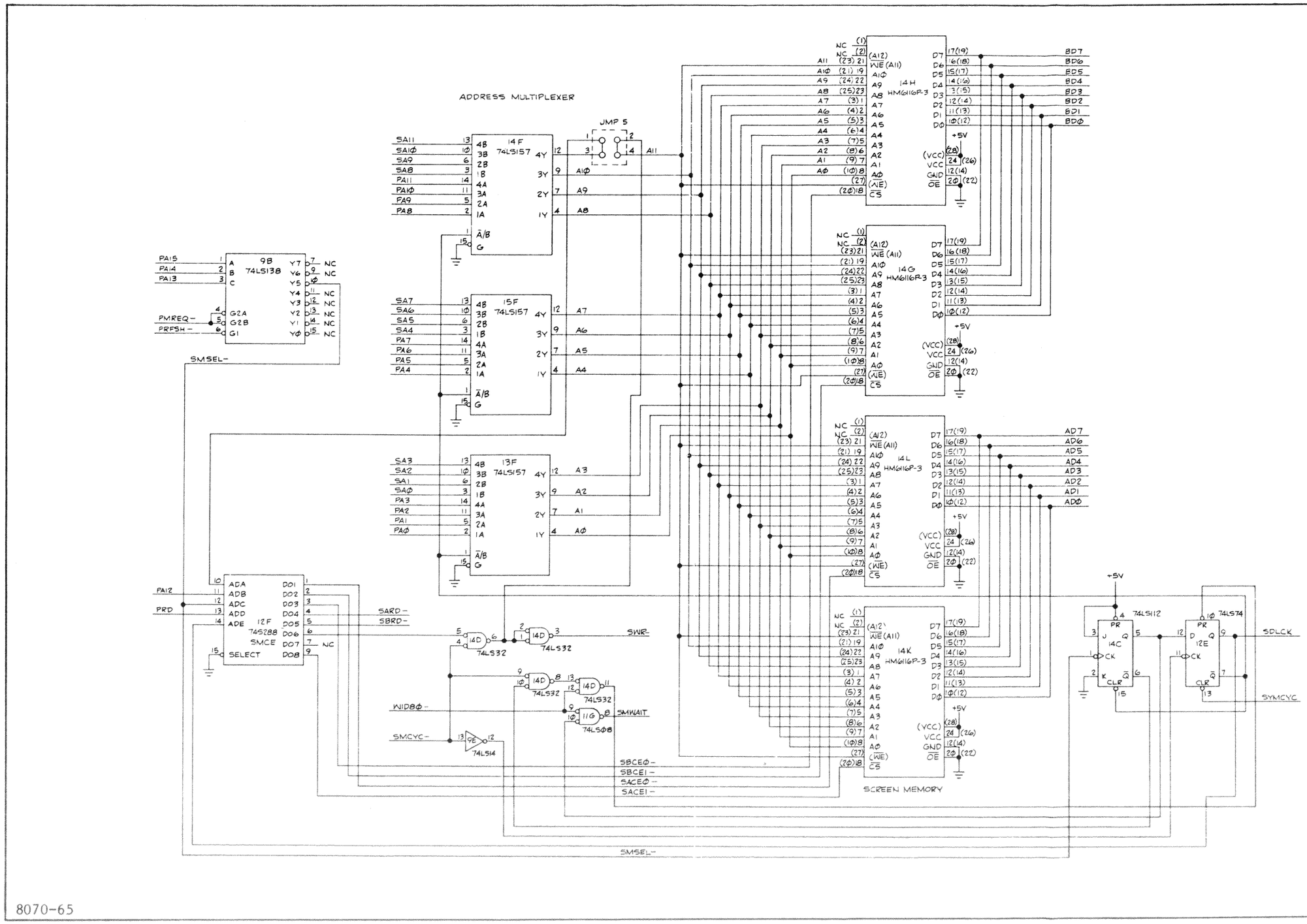
8070-63

Figure 6-2. Logic Diagram, Main Logic Board PCBA (Sht. 5 of 12) 903385 Rev. A



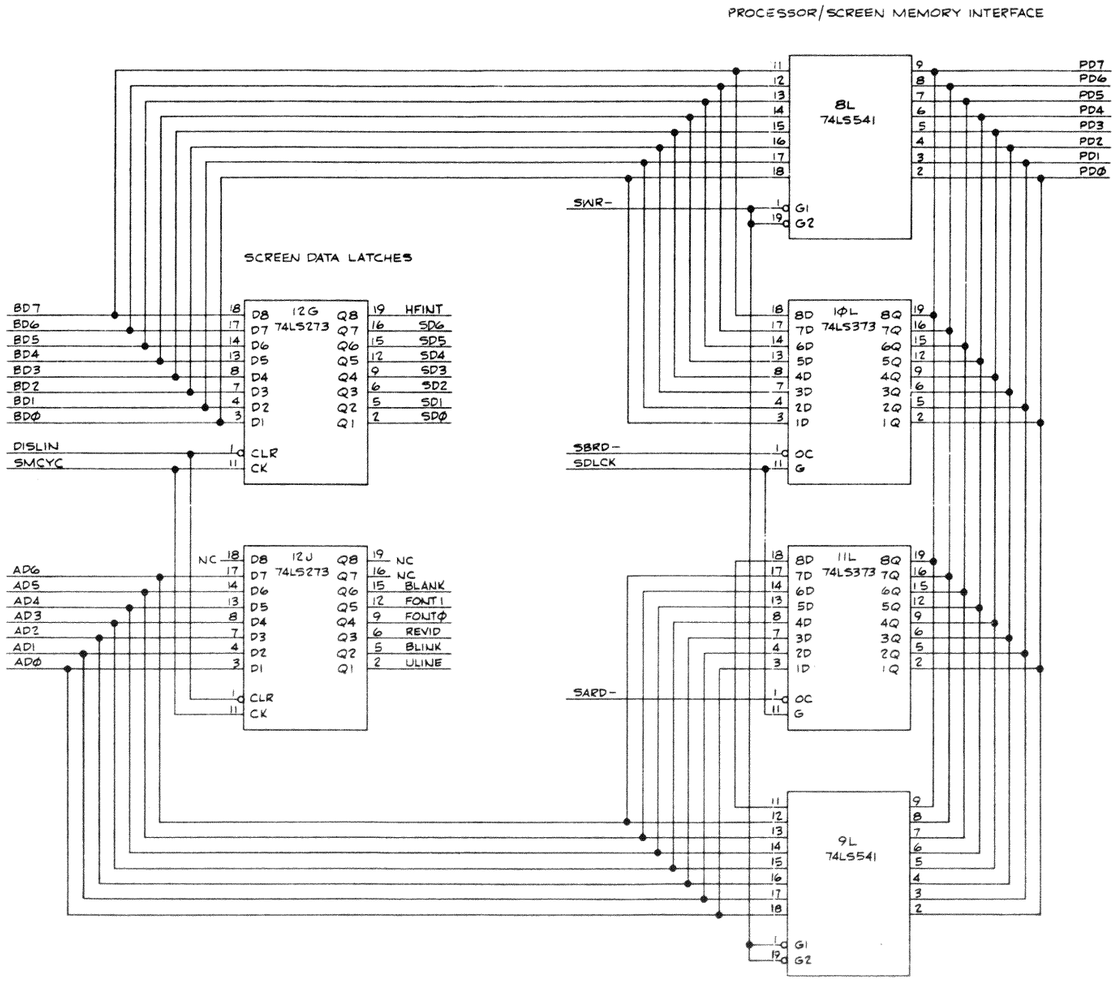
8070-64

Figure 6-2. Logic Diagram, Main Logic Board PCBA (Sht. 6 of 12) 903385 Rev. A



8070-65

Figure 6-2. Logic Diagram, Main Logic Board PCBA (Sht. 7 of 12) 903385 Rev. A



8070-66

Figure 6-2. Logic Diagram, Main Logic Board PCBA (Sht. 8 of 12) 903385 Rev. A

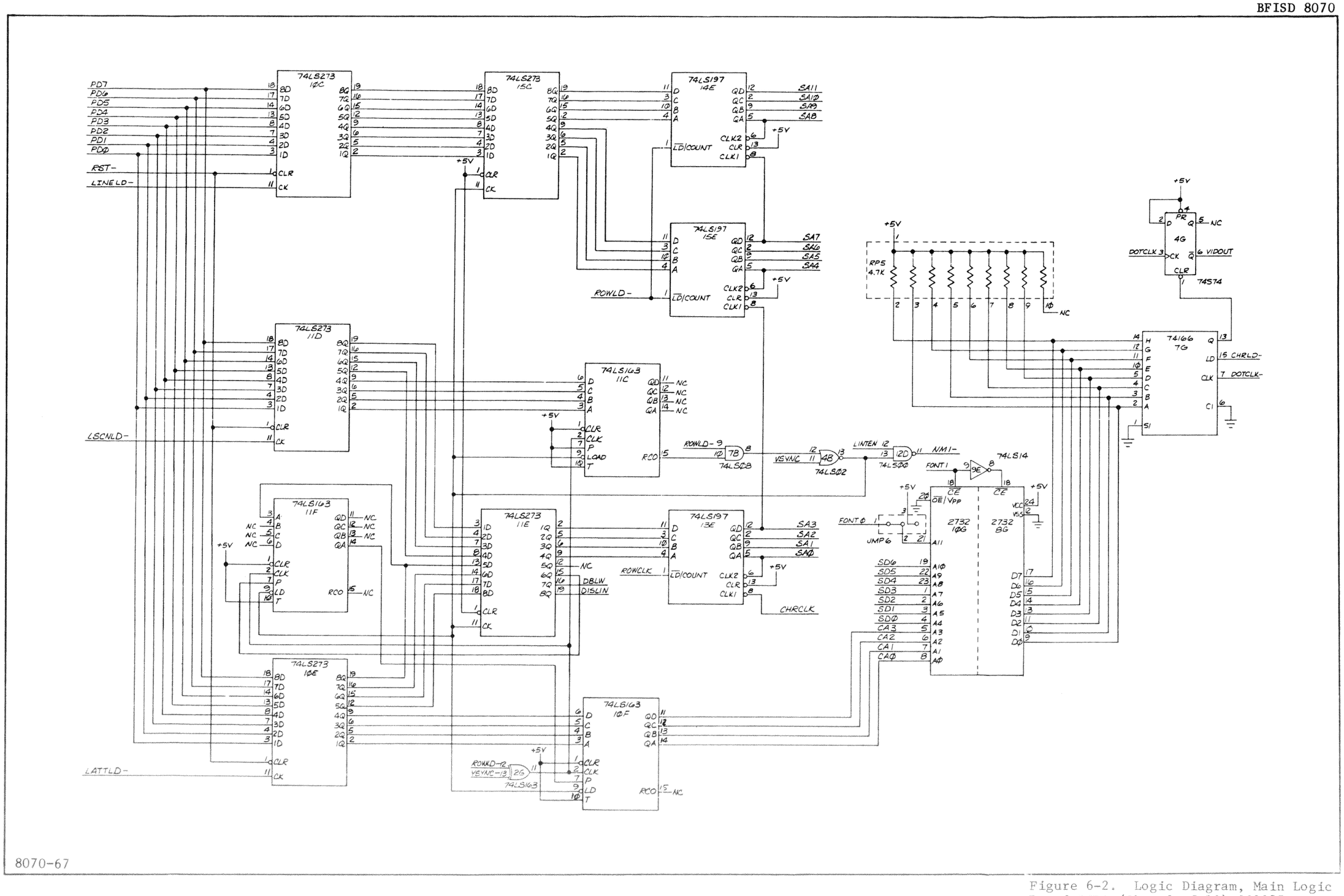
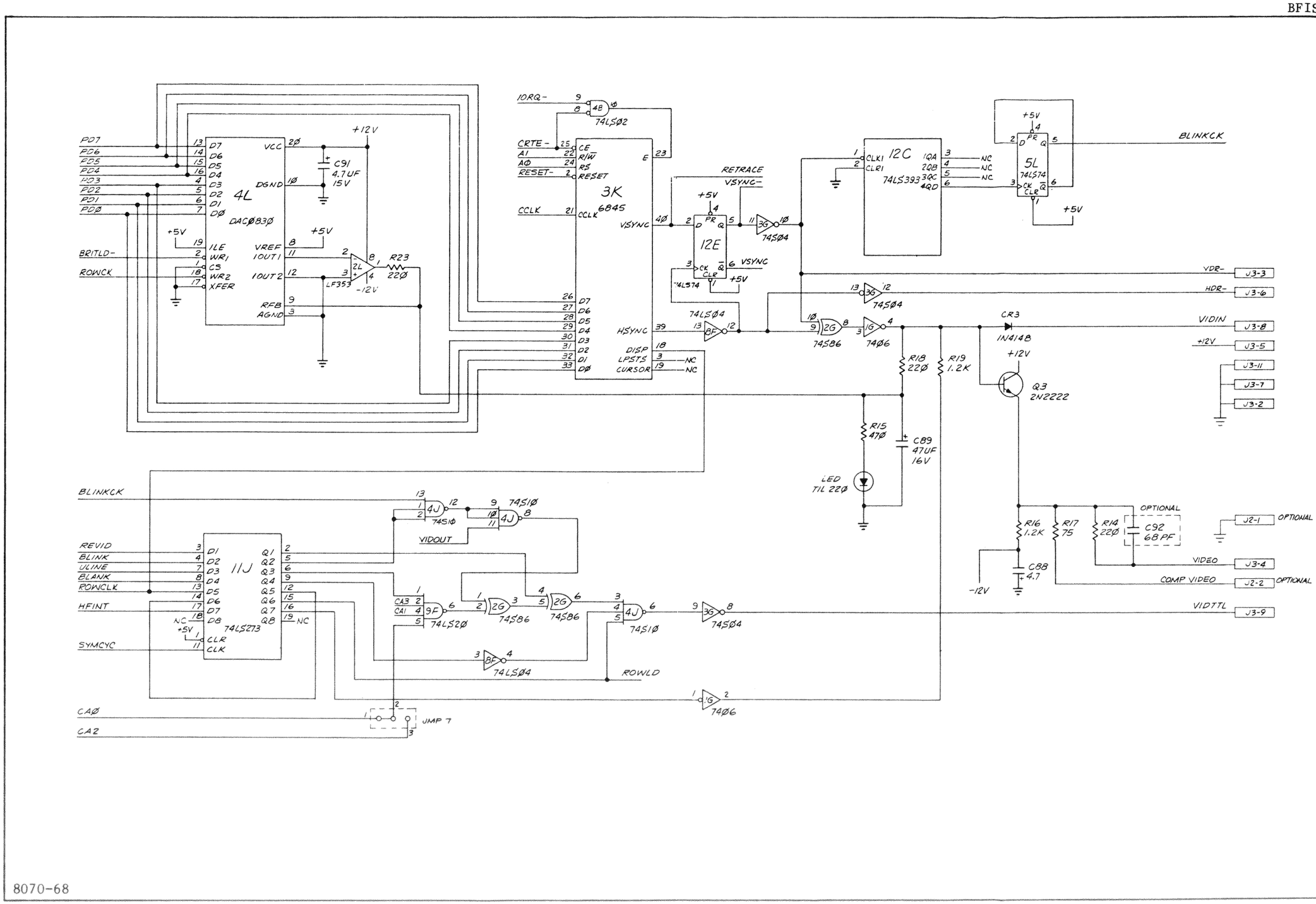
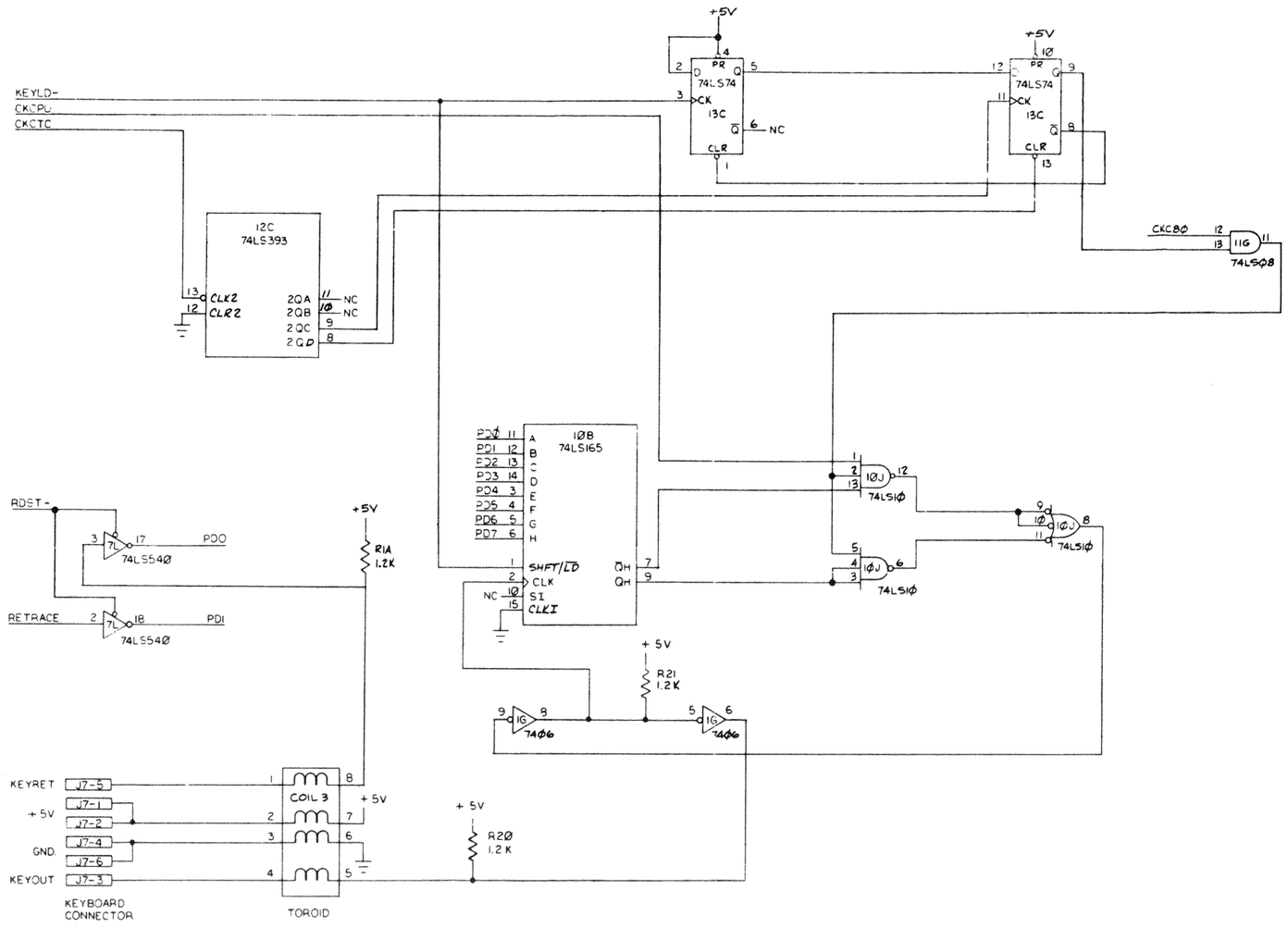


Figure 6-2. Logic Diagram, Main Logic Board PCBA (Sht. 9 of 12) 903385 Rev. A



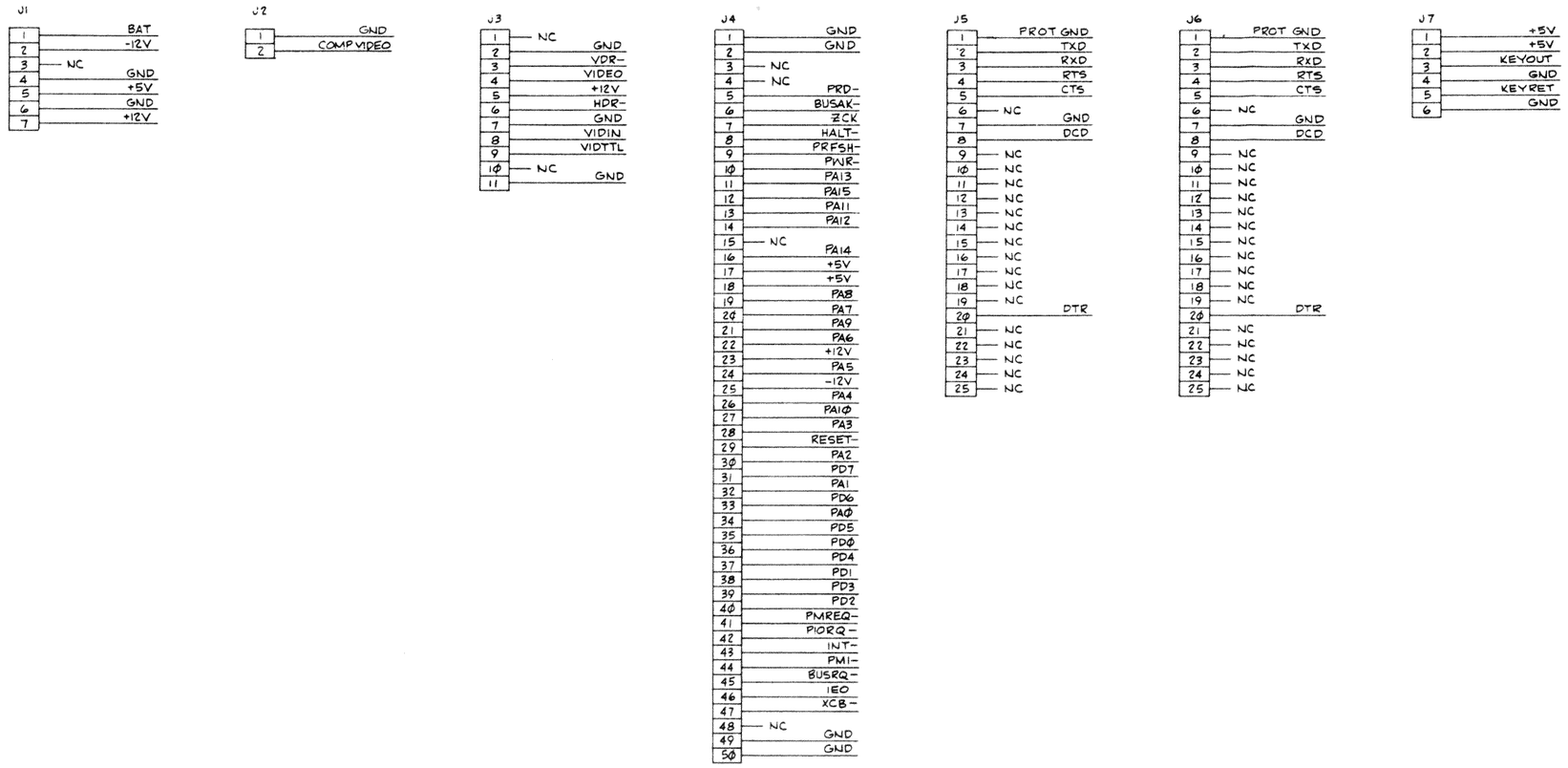
8070-68

Figure 6-2. Logic Diagram, Main Logic Board PCBA (Sht. 10 of 12) 903385 Rev. A



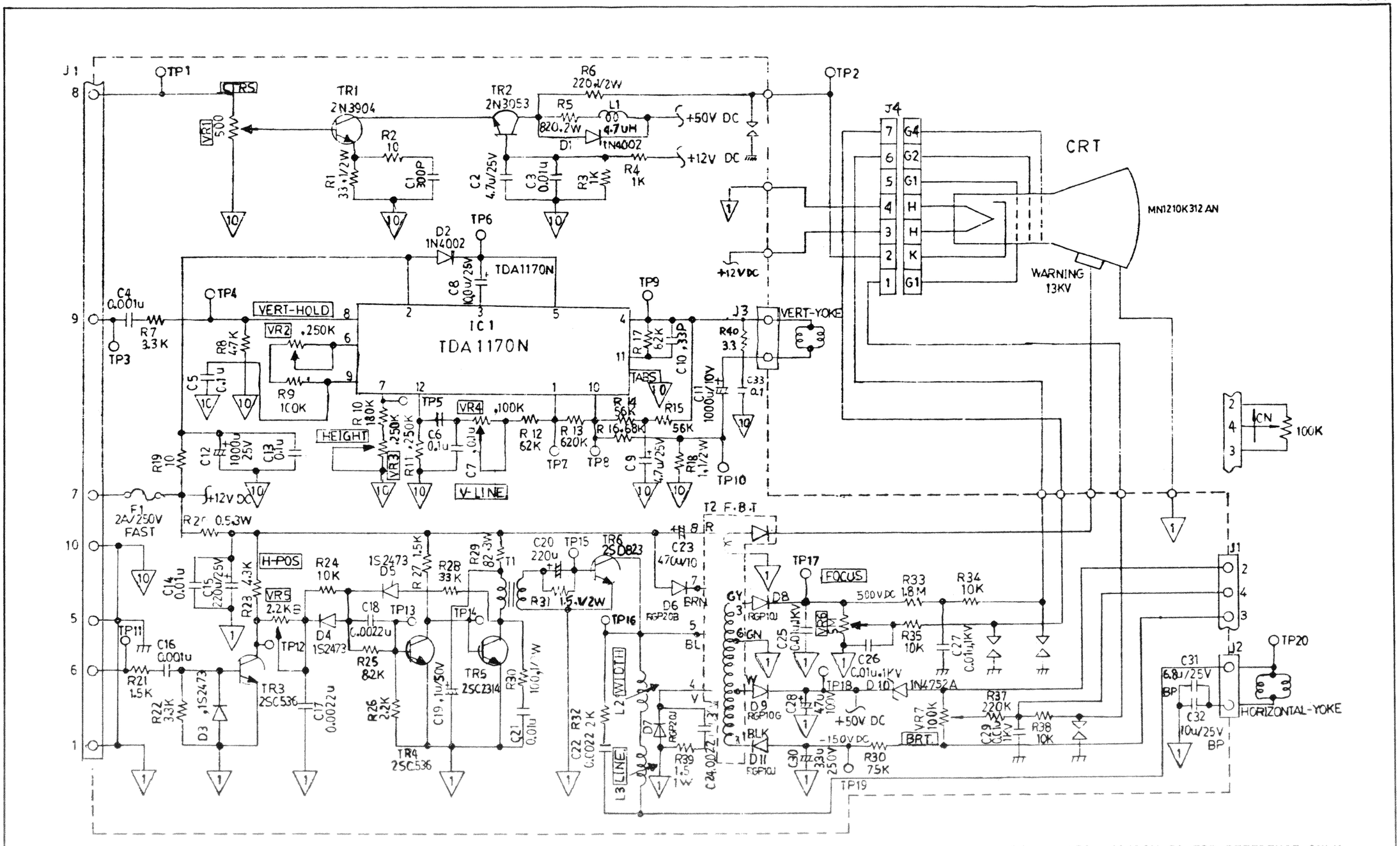
8070-69

Figure 6-2. Logic Diagram, Main Logic Board PCBA (Sht. 11 of 12) 903385 Rev. A



8070-70

Figure 6-2. Logic Diagram, Main Logic Board PCBA (Sht. 12 of 12) 903385 Rev A



NOTE: THIS DIAGRAM IS FOR REFERENCE ONLY - REVISION LEVEL WILL NOT BE MAINTAINED

8070-71

Figure 6-3. Schematic Diagram Monitor Board PCBA