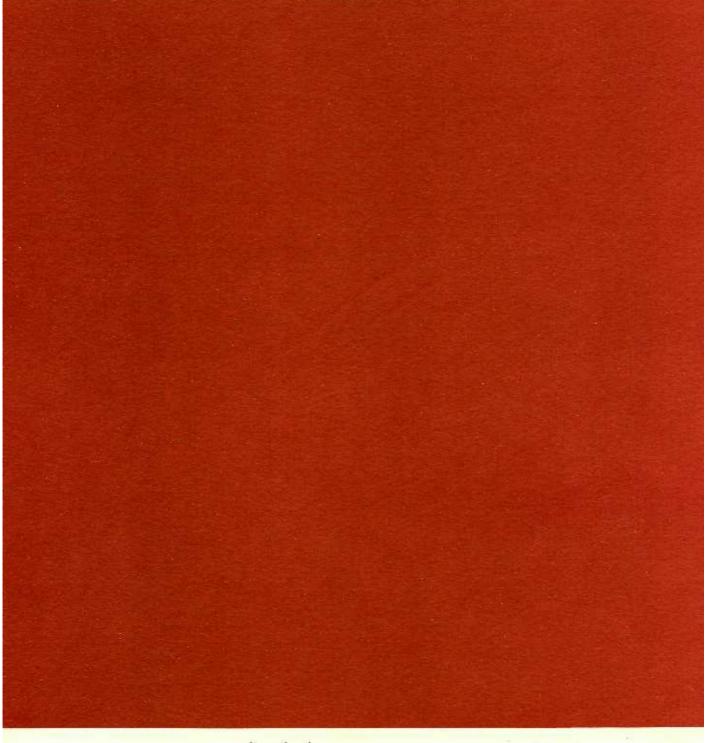
Basic Four Series 2000Desktop Computer SystemBFISD 8079AService Manual





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PREFACE

This manual provides service information for the Model 4108 Base Unit, used in the MAI® 2000 Series Desktop Computer System. The information is presented as an aid for field service personnel and supports the installation, operation and maintenance of each device contained in the Base Unit.

The major topics covered in this manual are:

- Section I Introduction
- Section II Installation and Operation
- Section III Functional Description
- Section IV Maintenance
- Section V Removal/Replacement
- Section VI Illustrated Parts List
- Section VII Floppy Disk Drive
- Section VIII 20 Megabyte Winchester Drive System
- Section IX 50 Megabyte Winchester Drive System
- Section X Schematics

NOTICE

MAI/Basic Four equipment is designed to meet the safety requirements of Underwriters Laboratories (UL) and the emission requirements of the Federal Communications Commission (FCC) and Verbandes Deutscher Elektrotechniker (VDE) as well as certain other applicable safety or regulatory agencies.

Compliance requires the use of specific interconnecting cables that have been determined to meet the applicable criteria. Use of cables not meeting these requirements could result in violations of local building codes and regulations, with resulting damages.

MAI/Basic Four shall have no responsibility for any results whatsoever that flow from any use of any cables other than those supplied or installed by MAI/Basic Four Information Systems or our authorized representatives.

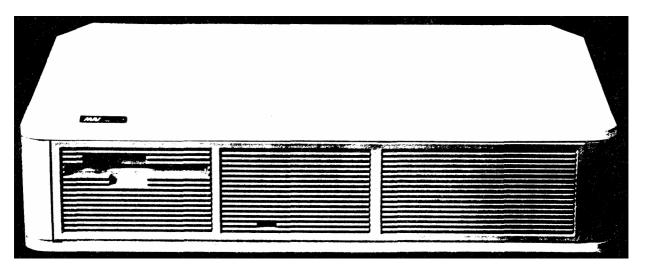


Figure 1-1. Model 4108 Base Unit

SECTION I

INTRODUCTION

1.1 GENERAL

The MAI® 2000 Series Desktop Computer System is a general purpose, multi-user, multitasking, 16-bit microcomputer system. The minimal system comprises a Base Unit (figure 1-1) and a video display terminal (VDT).

Device controller boards are available that plug into a Central Microprocessor Board, inside the Base Unit. A full complement of these boards (4) can support a magnetic cartridge streamer and 12 additional VDTs or serial printers. Also available is the Local Area Network Controller board, giving the system a LAN capability, based on CORVUS-licensed OMNINET. A maximum of six plug-in memory array boards provides 1.5 megabytes of system (main) memory.

1.2 SYSTEM DESCRIPTION

The configuration of the MAI 2000 Series Desktop Computer System is defined by the architecture of the Model 4108 Base Unit. Hence the following discussion focuses on Base Unit components and on the optional plug-in printed circuit boards. The Base Unit contains a central processing unit (CPU) that embraces the integrated bus, single board concept (the Central Microprocessor Board). Residing on the Central Microprocessor Board are two serial ports, a parallel port and a floppy disk controller. All subunits either are located on or plug into the Central Microprocessor Board. Figure 1-2 is a block diagram of the Base Unit hardware system. The minimal, or "entry level," Base Unit consists of no less than the following components:

- A Base Unit power supply module
- A Central Microprocessor Board (CMB)
- Three (plug-in) main Memory Array boards
- One 20 MB hard disk (Winchester) drive, with a controller board
- One floppy diskette drive or one tape streamer controller board

The Base Unit provides an inherent capability of supporting a second hard disk drive (unless a floppy diskette drive is present); another VDT (or a serial printer); and one parallel printer. Additional I/O (input/output) options are printed circuit boards that plug into the Central Microprocessor Board (or plug into a previously-installed I/O printed circuit board). These include 4-Way Controller boards (paragraph 1.2.4), a Magnetic (tape) Cartridge Streamer (MCS) Controller board (paragraph 1.2.5), and a Local Area Network Controller (LANC) board (paragraph 1.2.6). Three additional memory array boards may be plugged into the existing memory stack (Paragraph 1.2.2).

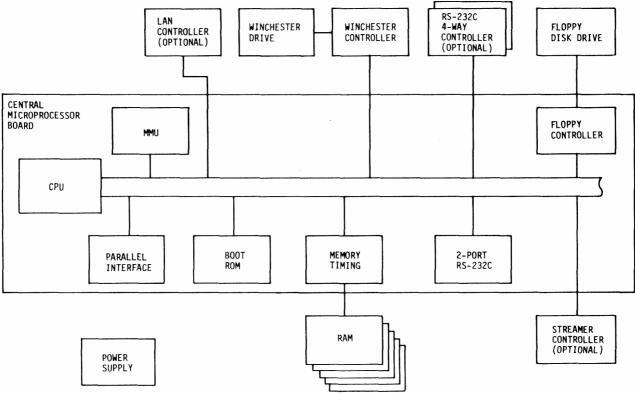


Figure 1-2. Block Diagram of the Base Unit Hardware System.

1.2.1 Central Microprocessor Board (CMB)

The CMB logic comprises three major functional areas: (1) the central processor section, (2) the memory control section and (3) the I/O section. The sections are linked primarily by the system bus structure. Figure 1-3 shows the layout of the Central Microprocessor Board, with additional subareas indicated. The central processor section is designed about the high-performance Motorola 68010 microprocessor chip, running at a clock rate of 8 MHz. The 68010 chip has a 32-bit internal architecture and a large, uniform memory address space. Other features include three major data sizes (byte, word, long word), supervisor and user states, and many flexible addressing options. The central processor section also includes the local I/O bus and the boot/diagnostic PROMs (programmable read-only memory).

A memory management unit (MMU) partitions the user portion of main memory into eight variable-length segments (per user). The MMU also controls the swapping of these segments to and from main memory and provides address translation, protection, sharing and memory allocation. Memory timing, address buffers and parity generation/checking logic also is part of the memory control section.

Onboard logic and controller can support two floppy diskette drives. Both drives are mounted inside the Base Unit. The driven diskette is 5.25 inches, soft-sectored, double-sided and double-density.

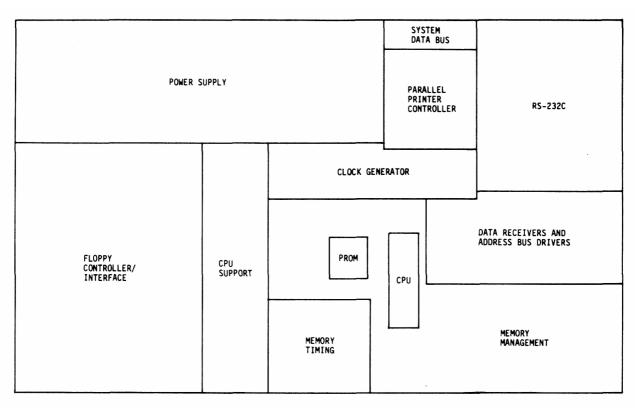


Figure 1-3. The Layout of the Central Microprocessor Board.

For an entry-level system, external peripherals are provided for by two serial (RS-232) connectors and one parallel connector. Logic and controllers for these are located on the GMB. The parallel connector allows attachment of the MAI/Basic Four® Model 4201 150/300 lines-per-minute parallel printer, or any similar plug-compatible printer with the Centronics interface. The two EIA RS-232C (25-pin) serial ports will accommodate two industry-standard terminals or one terminal and one serial printer.

1.2.2 Memory Array Boards

The Memory Array boards contain the active elements (i.e., RAM chips and signal buffers) that make up the main (system) memory. The array itself consists of industry standard 64K X 1 dynamic RAM chips. Each board provides 256K bytes arranged as 128K words, plus byte parity. Hence, the array contains 36 RAM chips. These boards are physically stacked on the CMB, and a maximum of six boards may be installed. Each array is plugged into the board below it. A full stack of six 256K Memory Array boards provides 1.5M bytes of main memory. Address space assignment of each Memory Array board is made by DIP switch selection. The Memory Array board responds to any contiguous set of addresses starting on a 256K byte boundary. At least three 256K byte Memory Array boards are required per Base Unit.

1.2.3 Winchester Disk Controller Board

The Winchester Disk Controller (WDC) board supports one or two Winchester (hard disk) drives, both residing in the Base Unit. (Two drives are possible only in the absence of floppy disk drives.) The WDC board, via its bus adapter, provides high performance DMA (direct memory access) to the system memory. The board is compatible with the many Winchester drives that conform to the Seagate Technology ST506 interface. No more than two Winchester drives may be used with a single Base Unit; therefore, no more than one WDC board is ever needed. The WDC board is piggy-backed to a WDC Bus Adapter board, and the combination plugs into either the Central Microprocessor Board or any previously-installed device controller board (stacked), so long as the WDC board is at the top.

1.2.4 4-Way Controller Board

The 4-Way Controller board provides four additional serial ports for each 4-Way Controller board installed in the Base Unit. This allows the user to add more display terminals and serial printers to the system. In special circumstances up to 14 terminals/printers may be attached to one system. However, system performance is specified for no more than eight terminals active simultaneously (two 4-Way Controller boards installed).

The 4-Way Controller ports conform to the primary subset of the EIA standard full duplex RS-232C interface via 9-pin D connectors, located on the 4-Way Controller board. Modem capabilities are provided for remote terminal support. The 4-Way Controller also supports eight-bit character transmission.

The 4-Way Controller board is intelligent (Z-80 based). Transmission of data from the Central Microprocessor Board to the 4-Way Controller board is by direct memory access (DMA) of 16-bit (word-wide) memory locations. Transmission is through data packets and command blocks. Reception of data by the Central Microprocessor Board from the 4-Way Controller board is buffered, program controlled and interrupt driven. Such parameters as stop bits, baud rate and parity are software programmable. Baud rates of up to 19.2K bits/second are allowable.

A partial set of the 4-Way Controller ports may be used to allow incremental growth of the system; remaining ports may go unused and will not affect the operation of the system. The 4-Way Controller board plugs into either the Central Microprocessor Board or any previously-installed 4-Way Controller board (stacked).

1.2.5 Magnetic Cartridge Streamer Controller Board

The Magnetic Cartridge Streamer Controller (MCS) board will support a single, high speed, 1/4-inch magnetic cartridge streamer drive. The drive itself is located external to the Base Unit. A single cable connects the drive to the MCS board at the outside rear of the Base Unit. The MCS board is intelligent (Z80 based) and uses high performance direct memory access (DMA) to the system memory, on the Central Microprocessor Board, in the Base Unit. Only one drive per Base Unit is ever required; therefore, no more than one MCS board is ever necessary. The MCS board plugs into either the Central Microprocessor Board or any device controller board that may be present (stacked), but above the 4-Way Controller boards. (Note: information on the 1/4-inch MCS drive is contained in a separate service manual.)

1.2.6 Local Area Network Controller Board

The Local Area Network Controller (LANC) board allows the creation of a local area network (LAN) or, where possible, allows connection of the MAI 2000 Series Computer System to an existing network. The LANC board is a single-channel communications controller, providing an interface to CORVUS-licensed OMNINET. The LANC provides bit-serial data communication to other local subsystems as well (such as a file server, disk server, printer and workstations). Up to 63 subsystems (nodes) can be connected via the LAN. Each subsystem follows the Carrier Sense Multiple Access/Collision Avoidance(CSMA/CA) protocol when it is accessing the network.

The bit transfer rate on the network cable is 1M bits/sec when the cable is properly terminated. No more than one LANC board per system may be installed. The LANC board is plugged into either the Central Microprocessor Board or any previously-installed device controller board (stacked), but always immediately below the WDC Bus Adapter board.

1.3 SPECIFICATIONS

Specifications for the MAI 2000 Series Computer System are listed in table 1-1.

Table 1-1. Specifications, MAI 2000 Series Desktop Computer System

PARAMETERS	CHARACTERISTICS

PHYSICAL

Base Unit

Height	6.1 inches (15.5 cm)		
Width	23.65 inches (60.1 cm)		
Depth	14.5 inches (36.8 cm)		
Weight	35 pounds (15.87 kg)		
POWER SOURCE REQUIREMENTS			
Line Voltage	100-120 VAC range (108.5 VAC nominal) or 220-240 VAC range (225.5 VAC nominal)		
Steady State Input Power	Less than 390 watts, maximum		

Table 1-1. Specifications, MAI 2000	Series Desktop Computer System (continued)
PARAMETERS	CHARACTERISTICS
Input Surge Current	Less than 35 amperes , maximum peak
Frequency	50 or 60 hertz
LINE FUSE	
100-120 VAC	6A, "Normal-Bio"
220-240 VAC	3A, "Normal-Bio"
POWER SUPPLY OUTPUTS	
Voltage	+5.000 and +12.000 VDC (nominal)
Current	20A @ +5 VDC (nominal); 0.3A @ -5VDC (nominal); 2.9A @ +12 VDC (nominal); 0.4A @ -12 VDC (nominal)
ENVIRONMENTAL	
Operating:	
Temperature	50°F to 98.4°F (10°C to 38°C)
Relative Humidity	20% to 80%, non-condensing
Altitude	Sea level to 10,000 feet
Storage:	
Temperature	-50°F to 122°F (-10°C to 50°C)
Relative Humidity	10% to 90%, non-condensing
Altitude	Sea level to 10,000 feet
OPERATIONAL	
Microprocessor Unit	Motorola 68010 (16/32-bit @ 8 MHz)
Floppy Disk Drives	One or two 5 1/4-inch, double-sided , double-density diskette drives (two drives may be installed only in the absence of a second hard disk drive). Storage capacity: 640K bytes

Table 1-1. Specifications, MAI 2000 Series Desktop Computer System (continued) PARAMETERS CHARACTERISTICS Winchester Disk Drives One or two 5 1/4-inch, non-removable hard disks (two drives may be installed only in the absence of floppy drives) Serial I/O Channels Two to sixteen asynchronous, bidirectional EIA RS-232C ports and one 2-wire local area network (LAN) port Parallel I/O Channels One 8-bit output channel for connection to any plug-compatible printer with the Centronics interface I/O Device Controller Boards 1 to 4 with LAN controller; 1 to 5 without LAN controller Main Memory 768K bytes (minimum) to 1.5M bytes (maximum); 64K X 1 dynamic RAM chips. Word length: 16 bits

SECTION II

INSTALLATION AND OPERATION

2.1 GENERAL

The Base Unit of the MAI® 2000 Series Computer System is designed to work in a normal office environment, free from dust and dirt. Hence, there are few restrictions on the suitability of location. Extremely nigh temperatures and humidity levels should be avoided.

The Model 4108 Base Unit has been fully tested at the factory and was in full working order when shipped.

2.2 UNPACKING AND INSPECTING THE BASE UNIT

The Base Unit is shipped in one carton, which also includes a power cable. Examine the carton upon arrival for signs of damage and mishandling. (Any damage sustained during shipment is the responsibility of the shipper.) Place the carton in an upright position, and open it.

CAUTION

Do not lift the Base Unit by the cover. The cover may release from the main chassis, causing the chassis to fall.

Lift the Base Unit from the carton as follows: grasp the Base Unit at opposite ends by wrapping your fingers around the bottom corners. Make sure your fingers are supporting the Base Unit by the bottom surface of the main chassis. Now lift. Place the Base Unit on a flat surface. (Save the packing and the carton, in case you have to move the Unit at a later time.) Check the Base Unit and any other contents of the carton for signs of damage.

2.3 INSTALLING THE 2000 SERIES COMPUTER SYSTEM

This procedure assumes that all the desired peripherals that will be part of the 2000 Series Computer System have been set up (according to applicable service/installation manuals) and are waiting to be connected to the Base Unit. (Required cables and their part numbers are shown in Section V, figure 5-2.) The Base Unit as shipped should match the utility power available to the user. The ac power outlets should be near the Base Unit so that extension cables are not necessary.

CAUTION

Only three-wire connectors and three-pronged plugs with the third wire connected to earth ground are acceptable electrical connectors. No two-wire connectors or plugs, with or without connection to a conduit ground, are to be used. Unstable equipment operation may result.

The Base Unit is easy to install. To prepare it for use, follow these steps.

- Remove the Base Unit cover by inserting a screwdriver, or a similar device, in the slot at the bottom right-hand side of the Base Unit cover. Push in to disengage the latch. Repeat with the left-hand side, remove the cover, and place the cover top-down on a flat surface. Remove all packing material from the disk drive(s) area. Remove the cardboard device supporting the Memory Array and I/O device controller boards.
- Install all device controller board options, following the procedures in "REMOVAL/REPLACEMENT," Section V, in this manual. For convenience, PCBA switch settings, jumper placements and cable connections are also included in this section, in paragraph 2.4.
- 3. Place the Base Unit on any convenient surface, such as a desk, table or stand. The Base Unit also may be positioned vertically, on end (this requires a special stand). In any case, be careful not to restrict the airflow through any of the Base Unit vents. Allow approximately four inches on all sides of the Base Unit for air ventilation.
- 4. Verify that the Base Unit power switch, at the rear of the Base Unit, is OFF (the "0" side of the switch is depressed).

CAUTION

Avoid plugging the Base Unit into a wall receptacle with the Base Unit power switch ON (with the "1" side depressed). This will corrupt the file system.

- 5. If the Base Unit includes a floppy diskette drive, push the drive button and remove the protective shipping cardboard from the drive.
- 6. Temporarily reposition the Base Unit so that you can easily reach the back panel to make the proper cable connections.

- 7. Connect a video display terminal to serial port 3 (the leftmost port of the four serial ports on the bottom 4-Way Controller board, as seen from the rear of the Base Unit. (Note: If you are connecting a Model 4310 EOT, the cable part number is 907753-001, and the PA end connects to the Base Unit.) Secure all connector screws.
- 8. Refer to the appropriate terminal manual for the setup procedure. The proper initial default parameters are the following:

9600 bits/second

7-bit character

1 stop bit

odd parity

- 9. Refer to the appropriate manual for electrical current specifications for each device that will be plugged into the wall outlet. To make sure the system will not trip a circuit breaker, the breaker rating must be greater than the combined current ratings of all the devices in the system. The Base Unit requires a 6A rating for 100-120 VAC and a 3A rating for 220-240 VAC.
- 10. Plug in the power cables for both the Base Unit and the terminal, and turn on the terminal.
- 11. Turn on the Base Unit (depress the "1" side of the Base Unit power switch), and press CTRL C during memory self test (to interrupt normal OS loading for system self-test verification).
- 12. Compare the information on the screen with the actual hardware in the Base Unit. They should match. (Note: the minimal system must contain at least three Memory Array boards; these provide 786,432 bytes of system memory. There also must be one Winchester Drive Controller board in the Base Unit [it always is the topmost board in the I/O device controller stack].) The following is an <u>example</u> of what you will see on the screen at this point:

Basic Four Information Systems MAI 2000

System S	Self Test Bl.1.7: SSN 2	000-90013	
cmb		pass	
memory	[size=1024 kbytes]	pass	c <alt load=""></alt>
fd		pass	
fw	[modules= 0]	pass	
wd		pass	
CS		pass	
ln	[modules= 0,nodes= 01] pass	

Boot device:

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13. Proceed with normal system load by pressing CR for Boot Device and then pressing CR again for SYSTEM FILE. Press CR again when the date prompt comes on the screen. (Note: If the operating system does not load, refer to the User's Guide, BFISD 6203A.) The following is an example of what you will see on the screen at this point (last few lines only):

Basic Four Information Systems M A I 2 0 0 0 System name: MAI 2000 System serial number: Operating System version: EOS7121C, BOSS/IX release 7.1A*20 (Sep 21

12:57:43 PM, 10/03/84. Update clock: hhmmssxx mtnddyy Wed Oct 3 1984 12:57:45 <single user mode>

ADMIN>

- 14. Shut down the system as follows:
 - a. Press CTRL D.
 - b. Type 'shutdown' (CR).
 - c. Wait for the prompt, and then turn OFF the Base Unit power (by depressing the "0" side of the power switch, at the rear of the Base Unit). The following is what you will see on the screen prior to shutdown (last four lines only; the last line is the prompt for power down):

ADMIN> <EOF> single, multi, or shutdown? shutdown

Press 'RETURN' key to reboot ('C'=alt-load, 'S'=self-test):

CAUTION

An incorrect shutdown procedure will corrupt the file system. If this has occurred, refer to Section IV, "MAINTENANCE," in this manual, to recover.

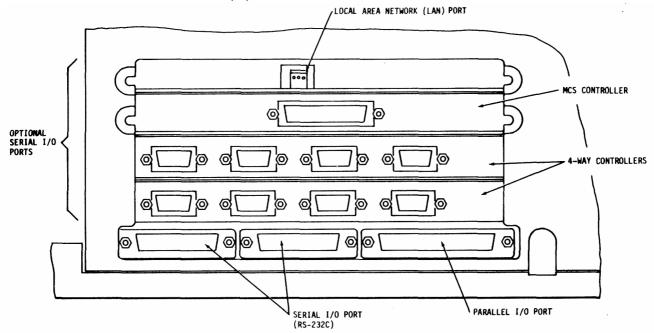
15. Turn OFF the Base Unit power.

16. Connect the rest of the peripherals to the Base Unit. Refer to the appropriate installation/maintenance manuals for setup procedures.

A parallel printer may be connected to the Base Unit parallel I/O port (port 2, 37-pin connector). A serial printer or another terminal may be connected to Base Unit serial I/O port 1 (25-pin RS-232 connector). Additional serial printers and terminals may be connected to the remaining Base Unit serial I/O ports.

- 17. If the system is equipped with the Magnetic Cartridge Streamer (MCS) unit, plug the PB end of the MCS cable into the back of the MCS unit. Plug the PA end into the connector on the MCS Controller board, at the rear of the Base Unit (see figure 2-1).
- 18. If the system is to be part of a local area network (LAN), refer to paragraph 2.4 in this section before proceeding.
- 19. Turn ON the Base Unit power.
- 20. When the operating system has booted, type in the time/date, and press CR; or just press CR. (Note: remain in the single-user mode.)
- 21. Type 'menu' and press CR.
- 22. Configure a port for each peripheral in the system as follows:

a. Select the UTILITY programs (1).



b. Select SYSTEM (8).

Figure 2-1. Rear View of Base Unit, Showing Location of All Connectors

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- c. Select PORT CONFIGURATION (2). (Refer to the User's Guide, BFISD 6203A, "Utilities" section, for details.)
- d. Press CR and select ADD DEVICE.
- e. Type in the port number.
- f. Type in the number corresponding to the device type.
- g. Type in the number corresponding to the device model.
- h. Select a device name.
- i. Select the appropriate parameters.
- j. Repeat this procedure from Step e for each periheral device in the system.

(Note: Configuration changes will not occur until the operating system is re-booted.

- 23. Shut down the system and re-boot.
- 24. Press CTRL D.
- 25. Type in 'multi' and press CR.
- 26. Type in 'admin' and press CR.
- 27. Check all terminals by logging on and observing the login message.
- 28. Check all printers as follows:
 - a. Type in "menul and press CR.
 - b. Select UTILITY programs.
 - c. Select DIRECTORIES.
 - d. Select DISPLAY.
 - e. Select REPORT DEVICES.
 - f. Select PRINTER NAME.
 - g. Repeat this procedure from Step c for each printer in the system.
 - h. To exit, press Motor Bar IV (MBIV).

- 29. Verify operation of the Magnetic Cartridge Tape Streamer (MCS) unit (if present) as follows:
 - a. Log on by typing in 'admin' to get to the command interpreter.
 - b. Turn on the MCS unit, and insert a scratch tape.
 - c. Label the tape by typing in

MCSLABEL SET=TEST ID=TEST SER=1 (CR)

(The utility will rewind the tape; replace an existing label, or format the tape and write a new label; and again rewind the tape. Upon completion of the process, the new tape label is displayed on the screen.)

- d. As a final read verification, type in 'MCSLABEL1 to redisplay the label.
- 30. Shut down the system as follows:
 - a. Type in 'shutdown 0.'
 - b. Press CTRL D.
 - c. Type in 'shutdown.'
 - d. Wait for the prompt, and then turn OFF the Base Unit power (by depressing the "0" side of the power switch, at the rear of the Base Unit).
 - 31. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to "snap" into place.
- 2.4 SWITCH SETTINGS, JUMPER PLACEMENTS, CABLE CONNECTIONS

The following paragraphs contain switch settings, jumper placements and cable connection for the following:

- o Central Microprocessor Board (paragraph 2.4.1)
- o Memory Array PCBA (paragraph 2.4.2)
- o Winchester Controller PCBA (paragraph 2.4.3)
- o 4-Way Controller PCBA (paragraph 2.4.4)
- o Magnetic Cartridge Streamer Controller PCBA (paragraph 2.4.5)

2.4.1 Central Microprocessor Board

See figure 2-2 for jumper locations and figure 2-3 for cable part numbers.

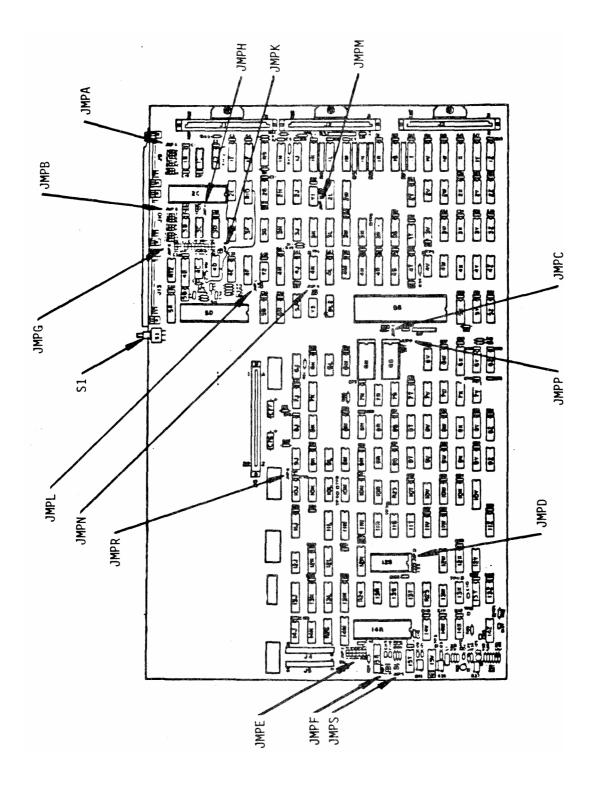
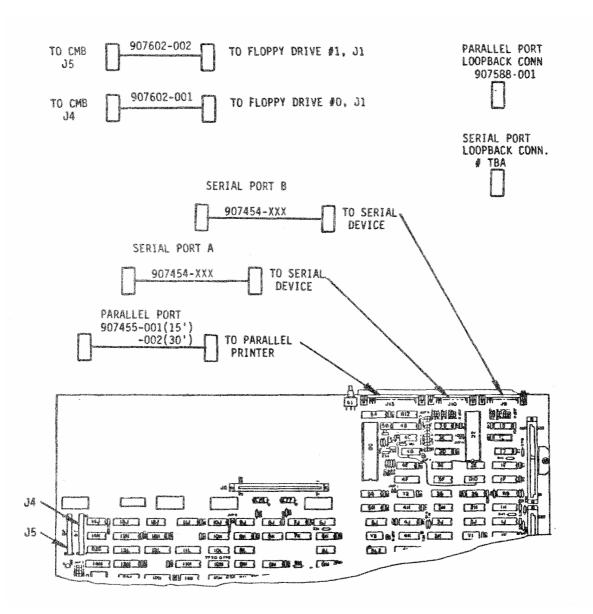


Figure 2-2. Location of Jumpers on Central Microprocessor Board



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Connect jumper N between points 1 and 2. (This jumper allows the master oscillator to be disconnected from the dividers and buffers. An external oscillator can be injected at this point. Normal operation is with jumper N installed.)

Connect jumpers C and P. These jumpers configure the board to accept four different size EPROMs, used for system diagnostics and the debugger. The Central Microprocessor Board can handle 2732, 2764, 27128 and 27256 EPROMs. As received, the CMB has jumpers in etch to handle either 2732s or 2764s; no modification is necessary. To use the other size EPROMs, or to switch back to the 2732 or the 2764, after using a larger EPROM, follow the chart below.

EPROM	JUMPER C	JUMPER P
2732 (4K x 8)	1 and 2	1 and 2
2764 (8K x 8)	1 and 2	1 and 2
27128 (16K x 8)	2 and 3	1 and 2
27256 (32K x 8)	2 and 3	2 and 3

NOTE: An earlier version of the CMB (Rev. 1) could only handle 2716s and 2732s. On this CMB, jumper C must be connected as follows:

EPROM	JUMPER C
2716 (2K x 2732 (4K x	2 and 3 1 and 2

Connect jumper R. (This jumper, when disconnected, disables the memory refresh circuitry, thereby allowing easier debugging of memory and bus arbitration circuits. Normal operation is with jumper R connected between points 1 and 2.)

Connect jumpers A, B, G, H and K according to the following tables. (The serial port has two programmable ports. Each can be configured as RS-232 and support a modem, a printer or a terminal. Additionally, port B supports X-21. Note that only one cable is needed to support printers, terminals or modems. All signal switching is done on the Central Microprocessor Board via the jumpers. The RS-232 cable is a pin-for-pin connection. No signals or pins are cross-connected.)

PORT A: MODEM		TERMINAL		NAL	PRINTER		
	Name	Jumper A	Cable	Jumper A	Cable	Jumper A Cable	
	CTS	7 and 8	pin 5	7 and 9	pin 4	7 and 9 pin 4	
	DSRA	3 and 4	pin 6	*1 and 3	pin 20	1 and 3 pin 20	
	DTR	1 and 2	pin 20	*2 and 4	pin 6	2 and 4 pin 6	
	RTSA	9 and 10	pin 4	8 and 10	pin 5	8 and 10 pin 5	
	RXDA	11 and 12	pin 3	11 and 13	pin 2	11 and 13 pin 2	
	TXDA	13 and 14	pin 2	12 and 14	pin 3	12 and 14 pin 3	
	RNGA	In Place	pin 22				
	TRXCA	In Place	pin 15				
	DCDA	In Place	pin 8				

PORT	B: MODEM		TERMINA	L	PRINTER	<u>.</u>
Name	Jumper B	Cable	Jumper B	Cable	Jumper B	Cable
CTSB DSRB DTRB RTSB RXDB TXDB	7 and 8 3 and 4 1 and 2 9 and 10 13 and 14 15 and 16	pin 6 pin 20 pin 4	7 and 9 3 and 1 2 and 4 8 and 10 13 and 15 14 and 16	pin 20 pin 6 pin 5 pin 2		pin 20 pin 6 pin 5
	Jumper G		Jumper G		Jumper G	
RXDB DCDB TRXCB		pin 8	15 and 16 17 and 18 19 and 20 23 and 24	pin 8	15 and 16	pin 2
	Jumper H		Jumper H			
DCDB	1 and 2		1 and 2			
	Jumper K		Jumper K		Jumper K	
D422	*1 and 2		*1 and 2		*1 and 2	

NOTE: Be sure to disconnect all unused jumper positions on port B.

PORT B - RS-422:

Jumper	Connect	AND	Jumper	Connect
G	1 and 2		В	11 and 12
G	3 and 4		В	15 and 16
G	5 and 6		Н	2 and 3
G	7 and 8			
G	9 and 10			
G	11 and 12			
G	13 and 14			
G	21 and 22			

NOTE: When RS-422 is used in port B, be sure that jumpers

G:15 and 16, G:19 and 20, and K: 1 and 2

are disconnected.

*This jumper disables the RS-422 drivers.

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Connect jumpers L and M. (The serial ports are capable of communicating at a number of different speeds and can communicate both synchronously and asynchronously. Jumper L connects the master clock to the Baud rate generator, used for asynchronous input/output. Jumper M connects the synchronous clock to the port. These clocks are disconnectable for service purposes. Normal operation is with both jumpers [L and M] inserted, connecting pins 1 and 2 on each jumper block.)

Connect jumper D according to the following table. (The floppy disk drive support logic, on the Central Microprocessor Board, can support both 2K x 8 and 8K x 8 static buffers. This RAM is used as a sector buffer to speed up overall system performance when using the floppy drive. In addition, an optional 8K x 8 buffer may be used so that an entire track of information may be input/output to the 68010 microprocessor at one time without the processor having to read from the disk sector by sector.)

RAM SIZE	JUMPER D
2K x 8	2 and 3
8K x 8	1 and 2

Connect Jumper E. (The floppy disk controller, located on the Central Microprocessor Board, has three different data separators available: the Analog, the Standard Microsystems Corp. [SMC], and the Western Digital [WD]. The installation of the jumper depends on which data separator is used.)

SEPARATOR:

Analog			SMC	WD	
Data	1 and 2	Data	3 and 4	Data 5 and 6	
Clock	7 and 8	Clock	9 and 10	Clock 11 and 12	

Connect jumper F according to the following table. (This jumper selects between Standard Density and High Density decoding on the Western Digital data separator. The system described in this manual uses Standard Density disk drives.)

MEDIA	JUMPER F
Standard Density	1 and 2
High Density	3 and 4

Verify that jumper S is not connected. (This jumper is only to be used when calibrating the Western Digital data separator. The jumper grounds the VFOE input to the WD1691, simulating a read condition. Normal operation is the jumper disconnected.)

For a standard Central Microprocessor Board configuration, recheck the jumper nstallation by referring to the jumper configuration table (2-1). The following assumptions are made:

2732 or 2764 EPROMs 2K x 8 sector buffer Standard RS-232 DCE on serial ports A and B Analog Data Separator Standard density disk drives

Table 2-1. CMB Jumper Configuration

JUMPER	CONNECT	FUNCTION
А	7 and 9	Serial Port A - CTS
A	8 and 10	Serial Port A - RTS
A	11 and 13	Serial Port A - RXDA
A	12 and 14	Serial Port A - TXDA
В	1 and 3	Serial Port B - DSRB
В	2 and 4	Serial Port B - DTRB
В	7 and 9	Serial Port B - CTS
В	8 and 10	Serial Port B - RTSB
В	13 and 15	Serial Port B - RXDB
В	14 and 16	Serial Port B - TXDB
С	None	EPROM Size Select - 2732, 2764
D	2 and 3	Floppy Sector Buffer Size Select - 2K x 8
Е	1 and 2	Floppy Data Separator Select - Data
Е	7 and 8	Floppy Data Separator Select - Clock
F	1 and 2	Floppy Density Select
G	15 and 16	Serial Port B - RXDB
G	17 and 18	Serial Port B - DCDB
G	19 and 20	Serial Port B - TRXCB
G	23 and 24	Serial Port B - TRXCB
Н	1 and 2	Serial Port B - DCDB
K	1 and 2	Serial Port B - RS-422 Disconnect
L	1 and 2	Baud Rate Generator Connect
М	1 and 2	Serial Communications Synchronous Clock Connect
N	1 and 2	Master Oscillator Connect
P	None	EPROM Size Select - 2732, 2764
R	None	Refresh Enable
S	None	WD Data Separator Enable (Floppy Calibrate)

2.4.2 Memory Array PCBA

Set the appropriate switches for the desired physical address of the Memory Array PCBA. Refer to table 2-2 for a listing of switch settings, and see figure 2-4 for switch locations. Be careful not to duplicate addresses of existing Memory Array PCBAs; compare the switch settings of all the PCBAs.

		Table	2-2.	Memory Arra	y Module Addres	s Switch	Settings	
ADDR			01	G 2	G 2	G 4		96
(K By	(les)		S1	S2	S3	S4	S5	S6
0 t	256		ON	ON	DON'T CARE	ON	ON	ON
256 t	o 512		ON	ON	DON'T CARE	ON	ON	OFF
512 t	o 768		ON	ON	DON'T CARE	ON	OFF	ON
768 t	o 102	4	ON	ON	DON'T CARE	ON	OFF	OFF
1024 t	o 128	0	ON	ON	DON'T CARE	OFF	ON	ON
1280 t	o 153	6	ON	ON	DON'T CARE	OFF	ON	OFF

Note: OFF = OPEN and ON = CLOSED

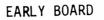
2.4.3 Winchester Disk (Single-Board) Controller Connect the appropriate jumpers for the desired board address and drive type as listed in table 2-3. See figure 2-5 for jumper locations and cable connections.

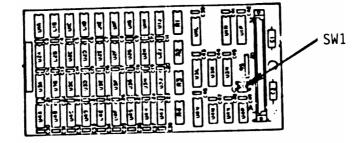
	Table 2-3. Winchester	Disk Controller Jump	per Connections
JUMPER A	BOARD ADDRESS (HEX)	JUMPERS B and C	DRIVE TYPE
1 and 2	CCXXXX	1A and 2A	143 MB (Note 2)
2 and 3	CDXXXX	1B and 2B	10/20 MB (Note 3)
		1C and 2C	50 MB (Note 4)

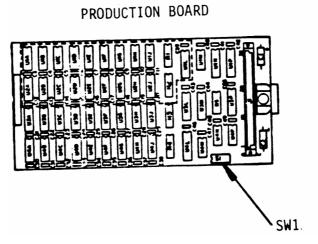
Notes: 1. Jumper B controls drive 0; jumper C controls drive 1. 2. Write precompensation always off.

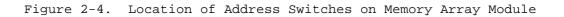
- 3. Write precompensation always on.

4. Write precompensation on at and above the reduced write current cylinder.









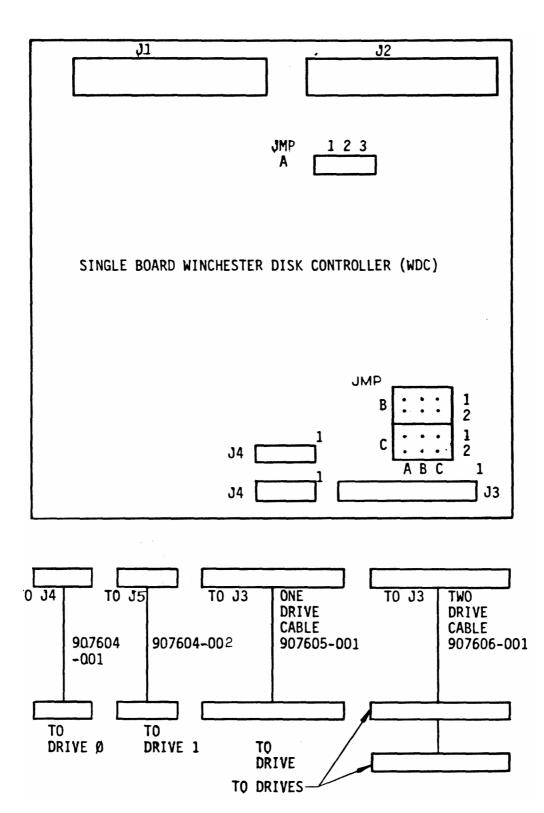


Figure 2-5. Location of Jumpers on (Single-Board) Winchester Disk Controller

2.4.4 4-Way Controller PCBA

Set the appropriate switches on the 4-Way Controller PCBA for the controller board address/DMA arbitration number and for the kind of peripheral(s) served by the Base Unit according to the listings shown in table 2-4. See figure 2-6 for the location of the switches.

```
Table 2-4. 4-Way Controller PCBA Switch Settings
```

SWITCH S1

		DMA Arbitration					PCBA	Address		
	S1	S2	S3	S4	S5	S6	 S7	 S8	 S9	 S10
Board 1 Board 2 Board 3 Board 4	ON ON ON ON	OFF OFF OFF OFF	OFF OFF OFF OFF	OFF ON ON ON	OFF OFF ON ON	OFF OFF OFF ON	OFF OFF OFF OFF	ON ON OFF OFF	OFF OFF ON ON	ON OFF ON OFF

SWITCHES PGM1-4*

For PGM1 through PGM4, connect the pins according to the PCB detail used:

PCB detail 904741-001 (current production)

PCB detail 904943-001 (future production)

TERMINAL/PRINTER	MODEM	TERMINAL/PRINTER	MODEM
1 to 7	1 to 2	1 to 3	1 to 2
2 to 8	3 to 4	2 to 4	3 to 4
3 to 4	7 to 8	9 to 11	9 to 10
9 to 10	9 to 10	10 to 12	11 to 12
13 to 15	13 to 14	13 to 15	13 to 14
14 to 16	15 to 16	14 to 16	15 to 16

*PGM1 through 4 are actually jumpers (as opposed to switches) enclosed in plastic rectangular "boxes." Each box may be pulled from its position and then reinstalled to connect any two adjacent pins. There is one PGM "group" per controller port, six boxes per PGM group, and 16 pins per PGM group.

2.4.5 Magnetic Cartridge Streamer Controller PCBA

Set the appropriate switches on the MCSC PCBA for the correct bus arbitration number and mode according to the listing shown below. See figure 2-7 for the location of the switches.

SWITCH SW1

_	В	us Arbitr	ation		_		
S1	S2	S3	S4	S5	S6	S7	S8
ON	ON	ON	ON	OFF	OFF	ON	ON

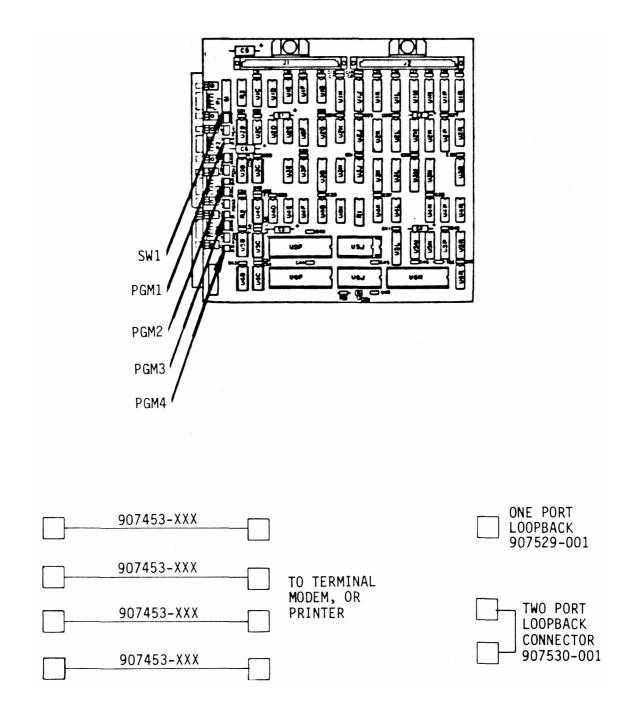
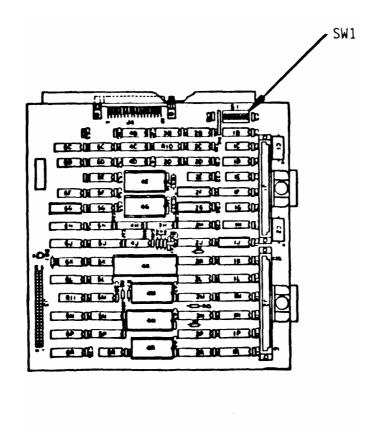
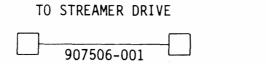
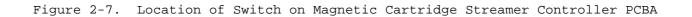


Figure 2-6. Location of Switches on 4-Way Controller PCBA







2-19

2.5 INSTALLING THE LOCAL AREA NETWORK (LAN)

When the user purchases the local area networking option for his 2000 Series system, he must obtain the following hardware and software components.

- a. The Local Area Network Controller (LANC) board
- b. A floppy diskette or cassette containing the LAN software
- c. One 15-foot tap cable
- d. One Tap Box™
- e. A user's manual

If this is the first 2000 Series system being installed, and a local area network does not yet exist, the following hardware also may be required.

- a. Network cables in 1,000-foot lengths, or shorter (total length not to exceed 4,000 feet)
- b. Two Tap Boxes
- c. A repeater for every 1,000 feet of cable after the first 1,000 feet, and an additional repeater when there are more than 32 systems on the network (63 systems, maximum)

The network cable is twin-lead, shielded or unshielded. Local electrical and fire regulations determine which type may be used and also determine where the cable may and may not be placed.

The cable also must meet certain LAN transmission specifications.

The following cables are recommended for use.

Manufacturer Part No. (22 AWG, shielded) Part No. (20 AWG, unshielded)

Alpha	9823	1895
Belden	9182	8205

2.5.1 Installing the LANC Board

Before installing the LANC board, you must set the station address (the user may have a number for you). The address uniquely identifies this station to all other stations on the network. To set it, first locate and identify the address switch on the LANC board. It will be found next to the cable connector (J3), as shown in figure 2-8.

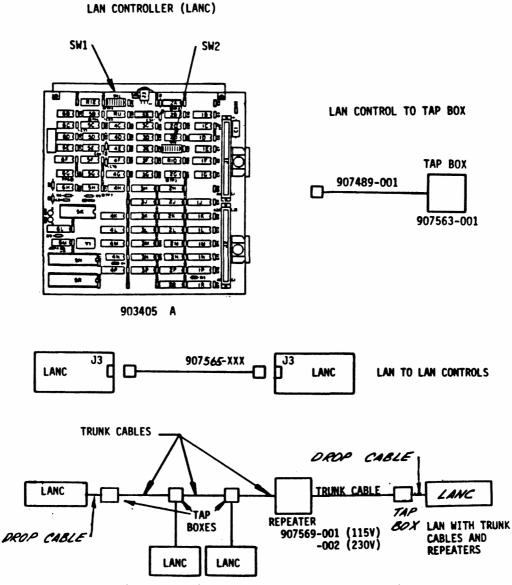


Figure 2-8. Location of Switches and Cable Information for LANC PCBA

The address switch comprises eight smaller switches, each set individually. The "off" position of each switch represents binary 1.

SWITCH SW1

Bias	Terminator			Station A	ddress		_
S1	S2	S3	S4	S5	S6	S7	S8
*	* *	Ť	Ť	Ť	ſ	Ť	Ť

- * represents the "bias." Switch 1 is set to 1 (off) on only one LAN controller board in a network; all other LAN controllers must have this switch set to 0 (on). A maximum of two LAN controller boards per Base Unit is allowable, but one per Base Unit is the normal configuration.
- ** represents the terminator setting. Only two controllers, one at each end of the network, may have this switch on; all other controllers must have the switch off.
- T represents the binary coded station address bit positions. Switch S8 is the least significant bit, and switch S3 is the most significant bit. Each LAN controller board has one unique address: the first address is 000001, and the 63rd address is 111111 (all switches off). (Note: 000000 is illegal.)

Switch S1 is the Bias switch and normally is set to the on position; however, one station must have this switch turned off to bias the line. Switch S2 is on only at the ends of a network; all other controllers must have this switch off. Switches S3 through S8 are set for the desired address; these may be treated as a 6-bit binary word, with switch no. 8 as the least significant bit.

There are 64 possible combinations of settings. With on = 0 and off = 1, the switches may be set for any one of 63 addresses (address 00 must not be used); for example,

100101 = address 37, and 111111 (all switches off) = address 63.

Another set of switches also must be set for the bus arbitration number and board address. These are set at the factory but should be verified by the installer before continuing. See figure 2-8 for the switch location.

SWITCH SW2

		Bus Arbi	Itration			Address	Decode
S1	S2	S3	S4	S5	SG	S7	S8
OFF	OFF	OFF	ON	ON	OFF	ON	OFF
OFF	OFF	OFF	ON	ON	ON	OFF	ON

The Local Area Network Controller board now is ready to be Installed in the Base Unit. To do so, proceed as follows:

- 1. Shut down the system, and turn off the Base Unit power.
- 2. Insert a screwdriver, or similar device, in the slot at the bottom right-hand side of the Base Unit cover, and push in to disengage the the latch. Repeat with the left-hand side, and remove the cover.
- 3. Unplug the ribbon cables from the Winchester Drive Controller (WDC) PCBA, located in the card cage at the rear right-hand corner of the Central Microprocessor Board (CMB).

(Note: two of the drive connectors on the WDC PCBA are situated side by side; the right-hand connector [J0] receives the "0" drive cable, and the left-hand connector [J1] receives the "1" drive cable.)

CAUTION

Do not remove this board if power is applied to the Base Unit.

- 4. Unplug the WDC Bus Adapter PCBA and the WDC PCBA (which carries the WDC PCBA) as a single unit from the top of the "stack."
- 5. Plug the Local Area Network Controller PCBA into the CMB (or into the PCBA at the top of the stack) at the rear right-hand corner of the CMB. Line up the connectors, then press down firmly to connect the board, being very careful not to bend the pins.
- 6. Plug the WDC Bus Adapter PCBA and the WDC PCBA (mounted above the component side of the WDC Bus Adapter) into the LANC PCBA.
- 7. Plug the ribbon cables from the Winchester Drive into the WDC PCBA. (Note: the two narrower ribbon connectors on the WDC PCBA are situated side by side; the right-hand connector [J0] receives the "0" cable, and the left-hand connector [J1] receives the "1" cable.)
- 8. Replace the cover on the Base Unit. To do this, line up the side grooves on the front and back panels of the Base Unit with the matching grooves on the side panels of the cover. Now press down. The cover should snap into place. If it does not, remove the cover, and try again.
- 9. Plug the tap cable into the LANC board connector, accessible at the Base Unit rear panel. (The tap cable has a pressure fit connector at one end, which slides onto the LANC board connector.)
- 10. Plug in all connections to the Base Unit, including all previously attached peripherals.

2.5.2 Installing the Tap Box

The Tap Box connects the tap cable to the LAN cable. It is a passive device, designed to allow easy connection of the Base Unit to the LAN cable. Once installed, it should not be removed; to do so will break the network connection. Tap Boxes can be installed anywhere along the network cable, with no minimum or maximum distance between them. The diagram in figure 2-9 shows the layout of the Tap Box, with labels added for reference. Each Tap Box contains five pairs of screw terminals for connecting the network wires. The five pairs are labeled A1-B1, A2-B2, etc., to A5-B5. The A and B sides of each pair are electrically connected. The following instructions are for creating the network tap connection.

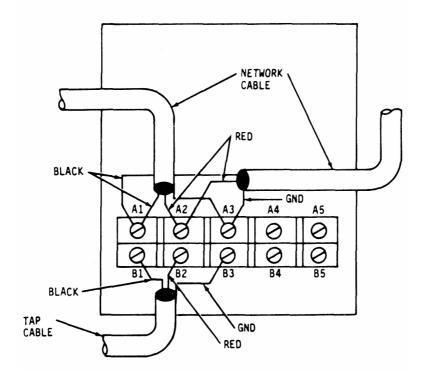


Figure 2-9. Outline of Tap Box, Showing Screw Connections

The following instructionsare for creating the network tap connection.

- 1. Cut the network cable at the place you wish the tap to be, and remove approximately one inch of covering from each of the two ends of the cable. This exposes the red, black and ground wires.
- 2. Slide a rubber grommet over each end of the cable, and strip approximately 3/8 inches of insulation from all four red and black wires.
- 3. Insert the stripped ends of the two black wires into screw terminal A1, and tighten the screw.
- 4. Insert the stripped ends of the two red wires into screw terminal A2, and tighten the screw.
- 5. Insert the ground wires into screw terminal A3, and tighten the screw.
- 6. Slide a rubber grommet over the wire end of the tap cable.
- 7. Insert the stripped black wire into screw terminal Bl, and tighten the screw.
- 8. Insert the stripped red wire into screw terminal B2, and tighten the screw.
- 9. Insert the ground wire into screw terminal B3, and tighten the screw.
- 10. Remove three cutouts from the Tap Box, and install the grommet for each cable into a cutout hole.
- 11. If the Tap Box is to be attached to a wall, use the mounting holes in the back of the Box or the adhesive strip on the back of the Box.
- 12. Place the lid on the Tap Box, and secure it with the four corner screws.

2.5.3 Installing the Repeater

The repeater is an active device (amplifier) designed to compensate for the attenuation of the LAN cable signal after 1,000 feet of travel. A repeater must be installed every 1,000 feet in the LAN cable, after the first 1,000 feet. Hence, three repeaters are required for a maximum length network. (No more than 4,000 feet of LAN cable may be installed.) An additional repeater must be installed at the midpoint of a 1,000-foot segment of cable when more than 32 Base Units are in that segment (63 Base Units per LAN system is maximum). Also, when a branch, or "T" connection to the LAN cable, is required, a repeater must be installed at that point.

Figure 2-10 shows the layout of the repeater box, indicating the position of the two screw connector terminal strips. The terminal strip at the top of the box is for connecting the power transformer. The terminal strip at the bottom of the printed circuit board is for connecting the LAN cables.

TBD

Figure 2-10. Outline of Repeater Unit, Showing Screw Connections

2.5.3.1 Connecting Network Segments

The following procedure may be used as a guide for installing a repeater to connect two network segments.

- 1. Open the repeater by removing the screws at the four corners.
- 2. Strip all wire leads on the two LAN cable segments to be joined.
- 3. Insert the red wire from one segment into the left-hand + connector on the terminal strip at the bottom edge of the repeater printed circuit board, and tighten the screw.
- Insert the black wire from the same segment into the connector immediately to the right of the red wire just connected, and tighten the screw.
- 5. Insert the red wire from the second segment into the right-hand + connector of the terminal strip at the bottom edge of the repeater printed circuit board, and tighten the screw.
- Insert the black wire from the second segment into the connector immediately to the right of the red wire just connected, and tighten the screw.
- 7. Insert the ground wires from both segments into the adjoining "drain" connectors, and tighten the screws.
- 8. If a network branch is desired, continue with the following paragraph. Otherwise, continue with paragraph 2.5.4.3, "Connecting Power to the Repeater."

2.5.3.2 Connecting a Network Branch

A network branch, or "T" connection, may be made by attaching a third cable segment to the repeater. The following instructions assume that the procedure in paragraph 2.5.3.1, "Connecting Network Segments," has been completed. The branch segment cable is shown in figure 2-10 (labeled Segment 3).

To connect a network branch, follow this procedure.

- 1. Verify that the repeater power transformer is disconnected, or unplugged.
- 2. Carefully strip both wire leads on the third segment of the network cable.
- 3. Insert the red wire into the + connector of the middle pair of screw connectors, and tighten the screw.
- 4. Insert the black wire into the connector of the middle pair of screw connectors, and tighten the screw.

- 5. Insert the ground wire into either "drain" connector, and tighten the screw.
- 6. Reconnect the repeater power transformer, or follow the procedure in paragraph 2.5.3.3, "Connecting Power to the Repeater."

2.5.3.3 Connecting Power to the Repeater

The power transformer that was supplied with the repeater unit now may be connected. To do this, follow these instructions:

- Determine how long the power cable must be, and cut it to the desired length. (The maximum length is 100 feet if you use the same type of cable as the network cable.)
- 2. Carefully strip the wire leads at both ends of the power cable.
- 3. Insert a red wire into the connector labeled +V, at the top of the repeater printed circuit board, and tighten the screw.
- 4. Insert the black wire from the same pair into the connector marked GND on the same terminal strip, and tighten the screw.
- 5. Insert the red wire at the other end of the power cable into the connector labeled + on the power transformer, and tighten the screw.
- 6. Insert the remaining black wire into the connector labeled on the power transformer, and tighten the screw.
- 7. Plug the power transformer into the wall outlet.
- 8. Verify that the power connection is good, and that power is being applied to the repeater, by noting whether the LED (light-emitting diode) on the repeater printed circuit board is lighted.
- 9. Unplug the power tranformer, and proceed with the next cable segment installation, if any.
- 10. Plug all power tranformers into wall outlets, check the LEDs, and close the repeater boxes.

2.5.4 Installing the LAN Software

The local area network (LAN) software is supplied on a tape or a floppy diskette. The LAN software must be installed before local area networking can be used on the 2000 Series System.

To install the LAN software, follow the procedure in Chapter 7, MAGNET 2000 Local Area Networking User's Guide, BFISD 6351C.

With the LAN software installed, the customer may use the LAN Configuration Utility, according to his manual, <u>MAGNET 2000 Local Area Networking User's</u> Guide, BFISD 6351B.

2.6 USE AND CARE OF FLOPPY DISKETTE AND DRIVE

The Model 4108 Base Unit may contain no more than two 5-1/4 inch floppy disk drives, mounted one atop the other in the front panel. The drive has approximately 640K bytes of double-density storage per drive (formatted). The floppy disk drives use double-sided, double-density, soft sector diskettes. It is recommended that only diskettes purchased from the following manufacturers be used for optimal performance and data integrity.

Manufacturer	Double-Sided
Dysan	No. 204/2D
Verbatim	No. MD 577-01-18212

2.6.1 Diskette Insertion

Diskettes are inserted into the drive with the label side facing up and the large rectangular notch facing to the left. Gently place the diskette as far into the drive as it will go. Insert the diskettes only in this manner to avoid damage.

Diskettes should never be inserted into the drives when the power is not on; nor should the power be turned off when diskettes are in the drives. Turning the power on and off with diskettes in the drives can result in damage to the diskettes and in loss of data.

A few simple precautions should be taken in handling floppy diskettes to avoid damage to their recording surfaces. They should be treated with the same care you would give to other recording media, such as phonograph records or recording tape. Handle them gently at all times, and do not touch the brown diskette surface.

Do not let them come in contact with liquids, ashes, paperclips, or anything magnetic. Don't bend them out of shape or put heavy weights on top of them. Never use pencils or ball point pens to write on the labels. Use a soft felt-tip pen, or mark the labels before putting them on the diskettes.

Proper storage of diskettes also is important. They should be kept in their protective jackets whenever they are not in use. Diskettes should never be piled on top of each other - it is best to store them <u>upright</u>; the boxes in which they are packaged are good for this purpose.

The user's office supply vendor can provide him with excellent filing and storage containers for his diskettes. With proper care, the user can increase the life of his diskettes and avoid the loss of data.

2.6.2 Write Protection

Each box of diskettes provides a sheet of 3/4-inch foil stickers. These are called write protect tapes and are used to prevent alteration of the contents of the diskettes.

Diskettes that have been write protected can be read by the drives, but no data can be recorded. One use of this feature is to protect backup copies of software or data. It is a good idea to write protect a master diskette and its backup copy, so that neither can be inadvertently erased or altered.

To write protect a diskette, fold a write protect tape over the large rectangular notch, being sure that the entire notch is covered and that the fold lines up with the edge of the diskette. When write protection no longer is desired, simply peel away the tape.

SECTION III

FUNCTIONAL DESCRIPTION

3.1 INTRODUCTION

This section provides a functional description of the Central Microprocessor Board (CMB) in the Model 4108 Base Unit and of the memory array boards, which plug into the CMB. Functional descriptions of the peripheral controller boards and of the various disk drives are contained in other sections of this manual. The functional description of the magnetic cartridge tape streamer used with the Model 4108 Base Unit is in a separate manual.

To fully appreciate the material in this section, the reader should have some exposure through the manufacturers' literature to the Motorola 68010 micro-processor chip and to the input/output controller chips used in the CMB.

3.2 CENTRAL MICROPROCESSOR BOARD (CMB) DESCRIPTION

The CMB is the central processing unit (CPU) for the MAI® 2000 Series Desktop Computer System. The CMB embraces the single-board, integrated bus concept. Architecturally, the CMB logic comprises three major functional sections:

- Central processor
- System memory control
- I/O (input/output)

These are linked primarily by the system bus structure. Figure 3-1 is a block diagram of the CMB logic, highlighting the flow of addresses and data.

The central processor section is based on the 16/32-bit Motorola 68010 microprocessor. The functions of the central processor section include system bus control, timing signal generation, interrupt control, bus arbitration, memory parity error detection, and bus error detection.

In addition to decoding the address space, the system memory control section uses a memory management unit to partition a maximum of two megabytes of main memory into eight variable-length segments; this facilitates the swapping of programs between a hard disk and main memory and provides user program snaring and protection. The memory control section also includes dynamic RAM (random access read/write memory) timing/refresh circuitry for the memory array boards.

Onboard logic and controllers support one or two floppy disk drives. External peripherals are provided for by one parallel and two serial connectors. In addition to the local I/O controllers, the CMB includes a system I/O bus that allows full direct memory access (DMA) operation by plug-in peripheral device controller boards.

TBD

Figure 3-1. Simplified Block Diagram, Central Microprocessor Board

3.2.1 Clock Generator

The 68010 microprocessor subsystem requires a master clock to make the system operate satisfactorily. An 8-MHz clock signal is produced by a 16-MHz master oscillator (5K) whose output is divided in half by a 74S112 J-K flop-flop (5J). (Refer to the CMB Logic Diagram, sheet 5.) Other clocks needed by the system are developed in a 74S161 4-bit binary counter (6J). The 4- and 8-MHz clock signals (K4MHZ-, K8MHZ-, K8MHZ+ and CCLK-) are buffered by a 74S240 tristate inverter (4H), as they are distributed throughout the Central Microprocessor Board to many of the circuits described in the following paragraphs.

3.2.2 Function Code Decoder

In any multi-user computer system, one of the tasks of the operating system software is to provide a common set of input/output (I/O) subroutines for all the users' programs. These are usually accessed from the user program through trap instructions. (A trap is an internally generated [software] interrupt.)

To ensure the efficiency of I/O processing in the system, and the protection of users' programs, the system cannot allow a user to enter the system software partition of main memory (whether accidentally or maliciously). To this end, the 68010 defines all I/O instructions to be <u>privileged instructions</u> and determines two separate <u>modes</u> of operation: <u>user mode</u> and <u>supervisor mode</u>. A bit in the 68010 status register indicates the current mode.

The 68010 allows privileged instructions to be executed only in the supervisor mode. If an attempt is made to execute a privileged instruction in the user mode, the 68010 does not execute it but treats it as an illegal instruction and traps to the operating system. This dual mode operation allows us to be sure that only the (system software) device drivers can perform I/O operations.

Thus when the 68010 makes a reference, it classifies the kind of reference being made by using the encoding of three function code output lines. This allows external translation of addresses, control of access, and differentiation of special processor states, such as interrupt acknowledge. The binary-coded set of function code, or processor cycle status, signals are CFCO+, CFC1+ and CFC2+. These identify the kind of bus activity currently being performed.

Three different kinds of major processor cycles currently are defined in the 68010. The corresponding function code signals are decoded by a 74LS138 l-of-8 decoder (8R). (Refer to the CMB Logic Diagram, sheet 7.) The three outputs of the decoder are as follows:

- a. Function DeCode 2 (FDC2+) when asserted means the 68010 is running user programs
- b. Function DeCode 5 or 6 (FDC5R6+) when asserted means the 68010 is operating in the supervisor mode
- c. Function DeCode 7 (FDC7-) when asserted (low) means the 68010 is processing an interrupt acknowledge cycle

The function code outputs from the 68010 are valid whenever the CPU Address Strobe (CAS-) output is asserted. Therefore, the decoder is gated by CAS- so that the decoding happens only when the function codes are valid. Also, the decoder is disabled when the 68010 has relinquished control of the bus (when the CPU Bus grant ACKnowledge [CBACK-] signal is asserted).

The FDC7- signal, from the function code decoder, also is used to provide an Interrupt ACKnowledge (IACK-) pulse to the system I/O bus. FDC7- is delivered "on time" as IACK- via a NAND gate (6L); however, FDC7- also is input to a D flip-flop (6K) whose Q output goes to the other input of that NAND gate. As a consequence, FDC7- is ORed with a delayed version of itself.

The delay is caused by the K8MHZ- clock triggering the flip-flop on positivegoing edges, which occur at half of a clock cycle after the normal system clock cycle begins. The result is that IACK- is "stretched" by an additional half of a clock cycle after address strobe CAS- is negated. This creates an interrupt acknowledge pulse that is long enough to hold off a new series of bus arbitrations (discussed in paragraph 3.2.11) by the peripheral device controllers, on the system I/O bus.

For local use, the non-decoded function code CFC2+ is buffered in a 74LS04 inverter (7R) to become CFC2+A and CFC2-. When these signals are asserted, they indicate to many circuits on the Central Microprocessor Board that the 68010 either is in the supervisor mode or is processing an interrupt acknowledge cycle (i.e., the 68010 is not in the user mode).

3.2.3 Boot PROM

Independent of the operating system software, the following programs and data are imbedded in read-only memory and may be used in the 68010 supervisor mode.

- Symbolic debugger
- Initialization tests
- Bootstrap instructions
- Diagnostic aids
- Reset/exception recovery pointers

Two EPROMs (6N and 6S) are connected to the main address bus and to the 16-bitwide data bus. (Refer to the CMB Logic Diagram, sheet 18.) A Power-On Reset (POR-) cycle maps the EPROMs throughout the 68010 addressing range. This is necessary because the reset vectors must be located in the eight lowest memory locations, which address RAM during normal system operation.

The first WRITE cycle, however, clears a 74LS112 J-K flip-flop (8T) and negates the BOOT+ signal. The low BOOT+ is input to the address space decoder (7Z, CMB Logic Diagram, sheet 9) to assert PROMCE- (PROM Chip Enable). The EPROMs now may be read at a base address of 4XXXXX (hex), in the 68010 supervisor mode. The Central Microprocessor Board can support three different size EPROMs: 8K bytes, 16K bytes or 32K bytes. Whatever the size used, two EPROMs are wired in parallel with respect to the address bus to give a word size 16 bits wide. The highest boot PROM address depends, of course, on the size EPROMs used; and READ and WRITE cycles above that address are undefined. (Again, the only effect a WRITE cycle to the boot PROMs will have is to change the address space of the EPROMs.)

After the first WRITE cycle, the normal address ranges of the various boot PROM configurations are as follows:

EPROM SIZE	ACCESS RANGE (HEX)	UNDEFINED (HEX)
8K bytes	400000 to 401FFF	402000 to 4FFFFF
16K bytes	400000 to 403FFF	404000 to 4FFFFF
32K bytes	400000 to 407FFF	408000 to 4FFFFF

3.2.4 CMB Diagnostic Hardware

The Central Microprocessor Board contains hardware designed to cooperate with diagnostic programs, in the 68010 supervisor mode. (These diagnostic programs may or may not be imbedded in the operating system software.) This hardware includes the CMB status drivers and the CMB control register.

3.2.4.1 CMB Status Drivers

There are times when the diagnostic program requires a "snapshot" of the status of the Central Microprocessor Board. The CMB status contains information about various conditions in the CMB. This may be obtained by a READ cycle to address 2XXXXA (hex), in the 68010 supervisor mode. Table 3-1 is a list of the status bits, with descriptions.

Two 74LS244 tristate drivers (2M and 3M), when enabled, gate the status of the CMB onto the 68010 data bus. (Refer to the CMB Logic Diagram, sheet 19.) The drivers form a 16-bit-wide, read-only status register, whose address is 2XXXXA (hex). Enable signal CMBSTRE- (CMB STatus REad) comes from the READ status decoder, described in paragraph 3.2.12.1.

3.2.4.2 CMB Control Register

A CMB control register, in the form of a 74LS259 8-bit addressable latch (10M), is provided for testing purposes. (Refer to the CMB Logic Diagram, sheet 19.) The register can be written to at address 2XXXXX (hex), in the supervisor mode, and outputs seven bits. Each bit may be set or cleared by a WRITE cycle to the appropriate unique address for the bit. Writing a value of 1 sets the corresponding bit; writing a value of 0 clears the corresponding bit.

	Table 3-1.	Central Microprocessor Board Status Bits
BIT	NAME	DESCRIPTION
CDOO+	MMERF+	Memory management unit error flag
CD01+	PARITY+	Main memory parity error flag
CD02+	RTCZERO+	Hardware timer count zero interrupt flag
CD03+	PFD+	Power fail flag
CD04+		Always high
CD05+		Always low
CD06+	BUTTON+	Status of manual reset switch
CD07+	SSWARNF+	Memory management unit stack overflow flag
CD08+	RNGA-	Serial Port A ring indicator
CD09+	DSRA-	Serial Port A data set ready
CD10+		Always low
CD11+	RNGB-	Serial Port B ring indicator
CD12+	DSRB-	Serial Port B data set ready
CD13+		Always high
CD14+		Always low
CD15+		Always low

The CMB control register cannot be read. The various bit functions are shown in table 3-2.

3.2.5 Main Memory Fault Detection Circuits

Main memory fault protection is provided by parity generation and checking circuits. Parity bits are stored along with data bits in main memory (i.e., each data byte has an associated parity bit) and are used to guard against the rare faults in a dynamic RAM chip. A parity bit is generated on the Central Microprocessor Board for each WRITE cycle to a main memory byte or word location.

Odd parity is used; so, during a READ cycle, whenever the parity detection circuits receive an <u>even</u> parity from a memory location, a fault signal is generated. (This is an input to the status drivers described in paragraph 3.2.4.1.) Table 3-2. Central Microprocessor Board Control Register Bits

ADDRESS	(HEX)	BIT NAME	FUNCTION
200000		TSTOL	Drives testpoint TP8 high for testing purposes; otherwise it is always low
200002		TSTERL	Drives test point TP9 high for testing purposes; otherwise it is always low
200004		TSTMD+	Inhibits the parallel port drivers; forces erroneous parity to be stored in main memory during WRITE cycles when bit 3 (TSTPE+) of the control register is high
200006		TSTPE+	Forces erroneous parity to be stored in main memory during WRITE cycles when bit 2 (TSTMD+) of the control register is high
200008		TSTSER+	Inhibits the serial port drivers for testing purposes
20000A		LEDON-	Turns on the LED indicator on the Central Microprocessor Board
20000C		PTPMSK-	Inhibits detection of parity errors, by disabling bus error traps caused by parity errors; any parity errors occuring while this bit is low will be ignored; the setting of the parity flag in the CMB status register is not

The base address of the faulty memory chip is saved in a register (discussed in paragraph 3.2.5.1) to facilitate error logging and error recovery. A more obvious response, however, is the bus error trap generated by the parity check, which discontinues user program execution.

affected by this bit

Under normal system operation, each time a main memory location is written to, a parity value is generated and then stored in the corresponding parity RAM bit. (Refer to the CMB Logic Diagram, sheet 39.) The parity value is produced by one of two 74S280 9-bit parity generator/checkers (2V and 3V); which 74S280 will be used depends on which of the two data strobes is active--the upper, the lower, or both. (Data strobes are explained in the 68010 manual.) The EVEN output from these devices is sent to the memory array boards as signals MPARO+ (Memory PARity) and MPAR1+, via connector J3.

Then, when a memory location is read, the parity bits (now labeled MPRO+ and MPR1+) come in from the memory array boards via connector J3. After passing through a PAL (programmable array logic) chip (6Y, CMB Logic Diagram, sheet 40), the signals become IPARO+ (Incoming PARity) and IPAR1+ and enter the parity generator/checker chips (3V and 2V). If a parity error is detected by one, or both, of these chips, then three major events will occur in the CMB:

- a. The base address of the faulty memory chip and two bits of GMB status are stored in a parity error register.
- b. The parity bit to the CMB status driver is set.
- c. A 68010 level 7 interrupt is generated.

3.2.5.1 Parity Error Register

The parity error signals from the 74S280s (2V and 3V) are gated in the parity logic PAL (6Y) to a parity latch (if the memory array boards are enabled [indicated by Memory Upper/Lower Data Strobes MUDS+ and MLDS+ active] and a READ cycle is in progress [indicated by 68010 Memory ReaD strobe MRD+ active]), inside the PAL.

The PAL parity latch output becomes signal SINT7- (Special INTerrupt, level 7) and is used to create the highest priority interrupt to the 68010, if a parity error is detected. The SINT7- output also is inverted by a 74S04 (8W) to become clock signal PERADCK+ (Parity ERror ADdress ClocK). This will clock the base address of the faulty memory RAM, along with two bits of (MB status information, into the parity error register. (Refer to the CMB Logic Diagram, sheet 41.) The parity error register comprises a 74S374 transparent latch (3N) and a 74LS240 inverter (3S).

The inputs to the parity error register include the following:

- The four high-order memory array address bits from the 68010 or from a peripheral device controller, when that controller is bus master
- Signals PERO- (Parity ERror) and PER1-, which indicate which two parity error signals (MPARO+ or MPAR1+) generated the PERADCK+ signal (which clocked the parity error register)
- The non-decoded CFC2+A 68010 function code signal, which, when active, indicates that the 68010 was not in the user mode. If the parity error occurred because of a peripheral device controller fault, this status bit is undefined
- The CPU Bus grant ACKnowledge (CBACK+) signal, which, when active, indicates that a control subsystem other than the 68010 is bus master

The parity error information contained in the parity error register may be obtained by a READ cycle to address 2XXXX2 (hex), in the 68010 supervisor mode.

3.2.5.2 Status Register Parity Bit

The two parity error signals (PERO- and PER1-) from the parity logic PAL (6Y) also are input internally to a parity status flag latch. (Refer to the CMB Logic Diagram, sheet 40.) The latch (inside the PAL) generates signal PARITY+. PARITY+ is an input to the status drivers described in paragraph 3.2.4.1.

3.2.5.3 Parity Error Interrupt Cycle

When a parity error occurs, the SINT7- output from the parity logic PAL (6Y) is asserted. SINT7- latches a flip-flop whose Q output then sends a low to the 7 input of an 8-to-3 priority encoder. (Refer to the CMB Logic Diagram, sheet 22.) The output forms an interrupt request via three 68010 interrupt request lines, IPLO- through IPL2-. Since no other interrupt can have a greater 68010 priority, an interrupt acknowledge cycle will begin upon completion of the current processor instruction.

The 68010 places the interrupt priority level on the lines carrying the three least significant address bits. These are decoded by a 1-of-8 data selector. For interrupt level 7, the CVPA- output is low. In response to CVPA- low, the 68010 generates a vector number based on the interrupt level number. The content of the vector number is fetched from RAM and then loaded into the 68010 program counter, and normal instruction execution commences in an interrupt service routine. (Interrupt logic is discussed further in paragraph 3.2.6.)

System software now can read the status register and discover that it was a memory parity error that initiated the interrupt cycle. The program can then go on to read the parity error register and find the base address of the RAM that caused the memory fault.

3.2.6 Interrupt Logic

There are at least two general strategies for control of input/output (I/O) in a computer system. One is initiated by the processor (program-controlled), and the other is initiated by the I/O port (<u>interrupt-driven</u>). The difference between the two is in the method used to determine when a port has completed an operation. In the case of interrupt-driven I/O, the port provides an <u>interrupt</u> request signal to the processor (CPU) when an operation has been completed.

Then, when the processor is at a point where the program in process can be suspended temporarily, the processor will commence with I/O operations. Upon completion of I/O operations, the processor continues with the suspended program. Since there are several circuits and I/O devices in the Model 4108 Base Unit that require interrupt processing, a technique for identifying the source and the priority level of the interrupt request is provided. The method used is vectored interrupts.

Generally, this means that a device requesting an interrupt is required to send a vector number to the processor for translation into the starting address of the appropriate interrupt service routine. Specifically, the requesting device sends a priority number to the 68010 as part of the interrupt request signal; then it sends the vector number as a separate signal after receiving an interrupt acknowledge signal from the 68010.

There are seven levels of interrupts available on the 68010, with level 7 being the highest priority. In the Base Unit, levels 2 and 4 may be auto-vectored or bus-vectored (both are explained in paragraph 3.2.6.1); levels 1, 3, 5, 6 and 7 are always autovectored. The seven interrupt levels are configured as follows:

LEVEL	SOURCE
1	Parallel port, from the PI/T (local)
2	System I/O bus peripheral device controllers
3	Floppy disk controller (local)
4	System I/O bus peripheral device controllers
5	Serial ports, from the SCC (local)
6	PI/T timer-real time clock count is zero (local)
7	Power fail, reset, parity error (non-maskable interrupt)

3.2.6.1 Interrupt Control Logic

When a device requires interrupt servicing, it asserts one of the seven INT(X)-(INTerrupt level X) signals. These are encoded by a 74LS148 8-to-3 priority encoder (3E). (Refer to the CMB Logic Diagram, sheet 22.) The output constitutes an interrupt request via the three 68010 interrupt request lines, IPLO-through IPL2-. If the priority of the interrupt is greater than the current 68010 priority, then the interrupt acknowledge cycle begins as follows:

Autovectored Interrupts

The 68010 places the interrupt priority level on the lines carrying the three least significant address bits. These are decoded by a 74LS151 l-of-8 data selector (10K). For interrupt levels 1, 3, 5, 6 and 7, the CVPA- (CPU Valid Peripheral Address) output of the data selector is low (active); for interrupt levels 2 and 4, the CVPA- output is active only when the AVTR- (Auto-VecToR) input, from the system I/O bus, also is active.

In response to CVPA- active, the 68010 internally generates a vector number that is determined by the interrupt level number. (The vector number [when multiplied by four] is the address, in the lowest 1K bytes of main memory, containing the beginning address of the routine that handles the interrupt.)

The content of the vector number is fetched and then loaded into the 68010 program counter, and normal instruction execution commences in the interrupt service routine. This is the autovectored interrupt mode of the 68010.

Bus-Vectored Interrupts

Interrupt levels 2 and 4 are bus-vectored when (a) they are selected by the data selector (10K) and (b) data selector input AVTR- (AutoVecToR), from the system I/O bus, is inactive. In this mode, the interrupt priority level on the 68010 lines carrying the three least significant address bits also is used as an address in a 68010 READ cycle. During the cycle, the 68010 obtains an 8-bit vector number from the peripheral device controller that is addressed by those bits.

Then, as in the autovectored case, the content of the vector number (after multiplication by four) is fetched and then loaded into the 68010 program counter, and normal instruction execution begins in the interrupt service routine. This is the bus-vectored interrupt mode of the 68010.

The data selector (10K) thus is used to switch between autovectoring and busvectoring for interrupt levels 2 and 4. The data selector is enabled only when signal FDC7- (Function DeCode 7) is asserted, signifying an interrupt acknowledge cycle is in process.

3.2.6.2 Interrupt Acknowledge Decoder

At the same time that the priority number on the address bus was being decoded to produce CVPA-, a 74LS138 l-of-8 decoder (10L, CMB Logic Diagram, sheet 20) also decoded those address bits. The IACKL3-, IACKL5- and IACKL7- (Interrupt ACKnowledge Levels 3, 5 and 7) signals are direct outputs. IACKL3- is used by the floppy disk controller, IACKL5- enables the byte multiplexer control logic, and IACKL7- is used by the interrupt control logic and the parity logic. Two signals, IACKL5- and IACKL7-, also are decoded with the other decoder outputs to create signals RIACK+ and RIACK- (I/O bus Requester Interrupt ACKnowledge).

RIACK+ provides the Processor Data Transfer ACKnowledge (PDTACK-) signal back to the 68010, and RIACK- provides the data bus direction control. Like the data selector, the decoder (10L) is enabled when FDC7- (Function DeCode 7) is active, and indicates a 68010 interrupt acknowledge cycle is in process.

3.2.7 Reset and Power Fail Detection Logic

The Central Microprocessor Board contains logic circuitry for three forms of reset: (1) power-on, (2) button, and (3) software.

Power-on reset and button reset are electrically similar. Power-on reset is automatic on power-up and generates a 100- to 800-millisecond reset pulse via an NE555 timer (5B). (Refer to the CMB Logic Diagram, sheet 21.) Power-on reset also generates a level 7 interrupt.

Button reset is actuated by the case-mounted switch, which is debounced by a 74LS00 NAND gate (4E). The output is RSTF2+, the master ReSeT Flag signal. The signal becomes POR- (Power-On Reset), which maps the boot PROM in all memory; generates HLT- (HaLT) for the 68010; and generates a RESET- for the system I/O bus and a CRESET- for devices on the Central Microprocessor Board.

The 68010 has a bidirectional reset pin (RST-), which receives the reset signal during a power-on reset or a button reset. On a software-created reset, the 68010 pulls RST- low, which causes the reset circuitry to issue a RESET- to the system I/O bus and a CRESET- for devices on the Central Microprocessor Board.

The signal PFD+ (Power Fail Detect) comes in on the system I/O bus to warn that power supply failure is imminent and generates an INT7- (INTerrupt level 7, the non-maskable interrupt).

3.2.8 System I/O Bus Control Logic

The system I/O bus provides data, address, timing and control functions to the various peripheral device controller boards that connect to the Central Microprocessor Board (CMB). The bus timing/control interface on the CMB includes arbitration logic, address and data gating controls, and bus transaction control signals*

All control lines from the 68010 are driven onto the system I/O bus. (Refer to the CMB Logic Diagram, sheet 14.) Signals CAS- (CPU Address Strobe), CLDS- (CPU Lower Data Strobe), CUDS- (CPU Upper Data Strobe) and CRNW- (CPU Read Not Write) are driven onto the system I/O bus by a 74S244 tristate buffer (1H) to become AS-, LDS-, UDS- and R/W-. These signals are driven on the I/O bus when the 68010 has control of that bus (indicated by signal CBACK+ inactive). Since both ends of the buffer are pulled up by resistors when the 68010 is tristated (indicated by CBACK+ active), the I/O bus end can be driven by a peripheral device controller, when that controller has control of the system I/O bus.

Function code signals CFCO+ through CFC2+ (CPU Function Codes 0 through 2) are driven onto the system I/O bus by a 74S240 tristate inverter (IF) to become FCO-, FC1-, and FC2-. The signals are driven onto the bus when the 68010 has control of the bus, Since the I/O bus end of the buffer is pulled up by resistors when the 68010 is tristated, the I/O bus end can be driven by a peripheral device controller, when that controller has control of the system I/O bus.

The CPU Lower and Upper Data Strobes, CLDS- and CUDS-, are ORed together by a 74S08 AND gate (7T) to provide signal CDS- (Combined Data Strobe), which is asserted when either or both data strobes from the 68010 are asserted. This signal is not driven onto the system I/O bus.

The CRNW- (CPU Read Not Write) signal is buffered and inverted by a 74LS00 NAND gate (9T) to produce RD- (ReaD), which is asserted when the 68010 either is in a READ cycle or is tristated. CRNW- is buffered by a 74LS32 OR gate (9V) reproduce WR- (WRite), which is asserted when the 68010 is in a WRITE cycle.

3.2.9 Non-Volatile RAM

For flexibility; the MAI® 2000 Series system allows the system console to be chosen from several kinds of terminals and to be connected to any available serial port. Likewise, the kind of device used to load, or boot, the operating system and the port location of that device can be chosen from several combinations. Also, a serial or a parallel default printer can be chosen, and the appropriate baud rate can be selected for the serial printer. Finally, a download device (e.g., a tape streamer) and port location may be chosen.

During system initialization, all these hardware configuration parameters must be communicated to the boot program. This is so the correct peripherals are logically connected to the system while, and after, the operating system software is loaded into main (RAM) memory. The following list is a summary of the parameters required by the operating system software while that software is being "booted."

- System boot device, unit number and baud rate
- System console terminal type, port and baud rate
- System printer port and baud rate, if serial
- System download port and baud rate

The Central Microprocessor Board provides a means for inputting the parameters and for storing them while power is off. The parameters are stored in a 64 X 4 non-volatile random-access memory chip (4L), or NVRAM. (Refer to the CMB Logic Diagram, sheet 36.) The NVRAM comprises a read/write RAM section and an electrically-alterable read-only memory (EAROM) data storage section.

The address space in which the NVRAM resides is partitioned into two interlaced segments, each containing 32 addresses (only one segment currently is used). A normal data READ or WRITE cycle is performed by a byte READ or WRITE to one of the (hexadecimal) addresses listed in table 3-3.

The addresses (bits A01+A through A08+A) come from the buffered address lines of the 68010. Since there is no A00 bit from the 68010 with the correct timing for the NVRAM, A08+A is used for the A00 input to the NVRAM (this accounts for the interlaced segments previously mentioned). Also note that the NVRAM does not have A6 and A7 address bit inputs; but the corresponding lines are connected for future expansion to a 256 X 4 NVRAM.

The data lines (BDOO+ through BDO3+) are the buffered data lines of the 68010. The WRite (WR-) signal comes from the buffered CRNW- (CPU Read Not Write) line of the 68010.

Signals NVRCE- (Non-Volatile RAM Chip Enable), NVRST- (Non-Volatile RAM STore), and NVRRC- (Non-Volatile RAM ReCall) are I/O address control lines. They are asserted when the following memory locations are addressed in the 68010 super-visor mode (X = "don't care").

ADDRESS (HEX)	SIGNAL
68X000-68X03E	NVRCE-
68X100-68X13E	NVRCE-
6AXXXX	NVRST-
6CXXXX	NVRRC-

The two additional addresses, 6AXXXX and 6CXXXX, are provided for store cycles and recall cycles. A recall cycle transfers data from the EAROM section of the NVRAM to the RAM section; and a store cycle transfers data from the RAM section to the EAROM section. This allows the programmer to reconfigure the NVRAM to the requirements of the system. After system power-up, data can be read from the NVRAM.

The data must first be recalled from the EAROM section by a supervisor READ to memory location 6CXXXX, which transfers the data to the RAM section. Then, the data may be read by doing supervisor reads to as many 68XOYY locations as is necessary (OYY is the NVRAM internal address). Remember: Bits A01 through A05 address one 32-location segment in the NVRAM; A08 addresses one of the two segments; and A06, A07 and A09 through A16 are "don't cares."

Data can be written to the NVRAM by doing as many supervisor writes to memory locations 68XYYY as is necessary. If the newly-written data is to be stored after power-down, then a store cycle must be done before power-down by a supervisor READ to location 6AXXXX, which transfers the data to the EAROM section. No further accesses of the NVRAM should be attempted for 9 milliseconds after a store cycle.

IMPORTANT

The vendor guarantees the NVRAM for no more than 1,000 store operations.

Each location in the NVRAM is dedicated to a specific parameter. Programming information is contained in tables 3-3 and 3-4.

3.2.10 Data Transfer Acknowledge Generator

As an asynchronous processor, the 68010 requires signal PDTACK- (Processor Data Transfer ACKnowledge) to be returned during every memory bus cycle. This input indicates that the data transfer is completed. When the 68010 recognizes the PDTACK- signal during a READ cycle, data is latched in the 68010, and the bus cycle is terminated; when the 68010 recognizes PDTACK- during a WRITE cycle, the bus cycle is terminated.

This "handshaking" technique allows the 68010 to compensate for the different access times of the various devices on both the local bus and the system I/O bus. If PDTACK- is returned to the 68010 before the end of processor "state 4" (refer to the 68010 manual), then the 68010 will act like a synchronous processor and complete the bus cycle at the maximum possible speed.

However, if PDTACK- is not returned by the end of state 4, then the 68010 will insert wait states until it receives the signal. Moreover, if PDTACK- is not returned within a set amount of time, then a bus error will occur, causing the 68010 to process a bus error exception cycle (i.e., the 68010 is forced to stop processing the current program and begin executing a special service routine).

During normal operation, though, when PDTACK- is returned, the 68010 continues with state 5 and completes the bus cycle. At the end of the bus cycle, PDTACKmust be negated (sent high) when the Address Strobe (AS-) is negated by the 68010, so it does not interfere with the beginning of another bus cycle.

Table 3-3. NVRAM Contents

NVRAM ADDRESS

CONTENT

680000	Boot device type
680002	Boot device unit number
680004	Boot device baud rate (if applicable)
680006	Console device type
680008	Console device unit number
68000A	Console device baud rate
68000C	Printer device type
68000E	Printer device unit number
680010	Printer device baud rate (if applicable)
680012	Download device type
680014	Download device unit number
680016	Download device baud rate
680018	Reserved
68001A	Reserved
68001C	Reserved
68001E	Reserved
680020	Reserved
680022	Reserved
680024	Reserved
680026	Reserved
680028	Reserved
68002A	Reserved
68002C	Reserved
68002E	Reserved
680030	Reserved
680032	Reserved
680034	Reserved
680036	Reserved
680038	Console terminal type
68003A	Not used
68003C	Checksum (left nybble)
68003E	Checksum (right nybble)

Table 3-4. Device Nybble Specifiers

PARAMETER	NYBBLE SPECIFIER
Device Type	
Serial Communications Controller	0
4-Way Controller	1
Floppy Disk Controller	2
Winchester Disk Controller	3
Winchester Disk Controller (NEC)	4
Magnetic Cartridge Streamer Controller	5
Parallel I/O (PI/T)	6
Unit Number	
Serial Communications Controller	0-1
4-Way Controller	0-15
Floppy Disk Controller	0-1
Winchester Disk Controller	0-1
Winchester Disk Controller (NEC)	0-1
Magnetic Cartridge Streamer Controller	0
Parallel I/O (PI/T)	0
Baud Rate	
110	1
150	2
300	3
1200	4
2400	5
4800	б
9600	7
19200	8
Terminal Type	
DUMB	0
EVDT	1
7270	2

Although the main system RAM memory is designed not to require wait states, the various "slower" peripheral chips on the Central Microprocessor Board <u>do</u> need wait states. The following paragraphs describe the hardware that generates the PDTACK- signal, and also introduce the Bus ERRor Flag (BERRF-) signal and include a list of the wait states for the various slave devices.

3.2.10.1 Timing Generation

Circuits on the Central Microprocessor Board (CMB) produce appropriate timing signals for PDTACK-. A 74S299 8-bit shift register (7K, CMB Logic Diagram, sheet 6) generates the timing pulses, which are used throughout the CMB. After selection and gating, the pulses produce PDTACK- signals with differing timing, depending on the device being accessed (discussed in paragraph 3.2.10.2). Before a 68010 bus cycle begins, the shift register is held reset during the following two conditions.

- Before the address strobe (AS-) is asserted during the memory READ or WRITE portion of a normal (READ or WRITE) bus cycle
- A READ-MODIFY-WRITE cycle (a 68010 TAS instruction), between the READ and the WRITE portions of the cycle. AS- stays asserted during this period; therefore, the AND of UDS- and LDS- (Upper and Lower Data Strobes) resets the shift register, both signals being high during the period. The Read/ Write (R/W-) signal is ANDed with UDS- and LDS-, which prevents the shift register from being held reset for an additional clock cycle during the beginning of a normal 68010 WRITE cycle

At the beginning of a READ or a WRITE cycle, address strobe AS- is asserted and sent, via a 74S02 NOR gate (9N) and a 74S08 AND gate (8Y), to the shift register CLEAR input, releasing the cleared condition. The pulled-up high level on the SR input of the register then is shifted right with each K8MHZ+ clock tick.

Since the 68010 does not need PDTACK- for autovectored interrupt acknowledge cycles, the CVPA- signal, active during the autovector interrupt, is ORed in the AND gate (8Y) so that the bus error flip-flop (6K, discussed in paragraph 3.2.10.3) is reset.

3.2.10.2 Timing Selection

To simplify the selection of the appropriate PDTACK- timing pulses, devices requiring the same timing are grouped into common memory address spaces. Since eight spaces are provided (discussed in paragraph 3.2.12), the required timing signal can be selected merely by decoding three high-order address bits A214A through A23+A. (Refer to the CMB Logic Diagram, sheet 6.) This is done with a 74S151 data selector (8K), which selects the shift register output to be used to create the PDTACK- signal. The data selector is enabled only during the 68010 supervisor mode or an interrupt acknowledge cycle (when CFC2- is active).

The following list shows the number of wait states inserted in the 68010 bus cycle for each device addressed.

A23+A-A21+A WAIT	STATES	DEVICE ADDRESSED
000	4	Boot PROM during boot; system memory otherwise
001	0	Local CMB status registers
010	4	Boot PROM
011	14	Local I/O (floppy controller; serial and parallel ports; Baud rate selection)
100	0	Memory management unit control
101	0	Memory management unit control
110	0	Peripheral I/O controllers (external DTACK-)
111	0	Interrupt acknowledge (external DTACK-)

Note: One cycle of the clock equals two wait states (125 nanoseconds).

The actual PDTACK- that goes to the 68010 processor comes from five different sources. Three of these are enabled by 74S38 open-collector NAND gates. One NAND gate (7N) enables PDTACK- for a system I/O bus-vectored interrupt acknowl-edge. Another NAND gate (8J) enables PDTACK- from the data selector (8K); signal CBACK- is ANDed in this gate for the following reason. When the 68010 is tristated (i.e., is no longer bus master), the address and strobe outputs from the 68010 are floating. This causes spurious outputs from the data selector, which would cause spurious PDTACK- signals.

One NAND gate (7N) does nothing. A fourth NAND gate (7N) enables the PDTACKsignal from the floppy buffer memory. This allows only 4 wait states during access of that memory, instead of the 14 wait states required by the floppy disk controller registers.

The fourth PDTACK- source is from the 68230 PI/T, which has a DTACK- generator built in. The fifth PDTACK- source is from a memory array board, and depends on which board is selected and whether or not a memory management error has taken place. The PDTACK- signal from the memory array board is gated onto the system I/O bus by another 74S38 (8J) when a system I/O bus peripheral device controller is bus master (indicated by the CBACK+ signal active).

3.2.10.3 Bus Error Generation

If, after eight shifts, the PDTACK- signal is not active, then the shift register (7K) will act as a "watchdog" timer. The inactive (high) PDTACK- signal is ANDed in a 74LS08 AND gate (9S) with the least significant bit output (H/QH) from the register. The result is latched by a 74S74 D flip-flop (6K), and the Q- output provides the Bus ERRor Flag (BERRF-). (This bus error flip-flop is toggled on the rising edge of the K8MHZ- clock.) The BERRF- signal then is returned to the 68010, forcing it to process the bus error exception cycle. The bus error flip-flop will reset when the shift register (7K) is cleared or the CVPA- signal is asserted. The timing of the shift register and bus error generation is shown in figure 3-2.

When a peripheral device controller is the bus master, the bus error flip-flop Q output is gated onto the system I/O bus as BERR- by the bus grant acknowledge signal (CBACK+, discussed in paragraph 3.2.11), via another 74LS38 NAND gate (3F). After the bus error occurs, the bus error flip-flop is reset by the address strobe (AS-) going high when the bus error exception processing begins.

3.2.11 Bus Arbitration Logic

All peripheral controllers that plug into the Central Microprocessor Board use direct memory access (DMA) techniques to transfer data to and from the system main memory. This means that each controller will need to have complete rule over the system I/O bus at some point in time, for some length of time. The purpose of arbitration is to give that controller a guarantee of conflict-free access to the bus.

To achieve this, the system includes arbitration logic circuits, collectively called the arbiter. Most of the logic is contained on the peripheral controller boards, allowing position-independence of the boards with respect to the system I/O bus slots.

STATE		0	1	2	3	4	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	6	7	0	
K8MHZ+	_	_		_		-		_	_		_	_		-		_		_	_	-	_	-	_	_			
AS-			-										-												-		-
CSTOF+						_																					_
CST1F+																											_
CST2F+													-			-											_
CST4F+																											-
PDTACK-										_																	-
BERRF-																	_								-		-

W = Wait state

Figure 3-2. Timing Diagram, PDTACK- and Bus Error Generation

The arbiter prioritizes bus access requests by devices (i.e., peripheral controllers) aspiring to bus mastership. The design of the arbiter is such that the 68010 always wants the bus, but gets it only when no other device wants it. This means that the 68010 is the lowest-priority device in the system, giving up the bus to any requesting device as soon as possible. Such a scheme allows the highest processing speed, because the 68010 never has to take the time to request the bus-access is automatic upon release by the current master.

Although the 68010 does not prioritize requests for bus accesses by external controller boards, or devices, it nonetheless is part of the arbitration logic circuitry. There are three bus arbitration signals used in the 68010:

- a. Bus Request (BR-1)
- b« Processor Bus Grant (PBG-)
- c, CPU Bus grant ACKnowledge (CBACK-)

(Specific details of the signals can be found in the 68010 manual, under BR-, BG-, and BGACK-.) When the 68010 is using the system I/O bus without competition, input signals BR-1 and CBACK- and output signal PEG- are inactive (high).

System bus arbitration begins when the bus request signal (BR-1) is asserted (low). A bus request can come from a system I/O bus peripheral (on connector J01, pin A13) or from the memory refresh circuitry. (Refer to the CMB Logic Diagram, sheet 8.) The bus request signal is buffered by a 74S244 tristate driver (IE) and sent to the 68010. At the time of the bus request signal, the priority resolution cycle begins.

Bus access prioritization is done with the aid of three parallel arbitration signals: BPRO- through BPR2- (Bus PRiority). These are placed on a special three-line priority bus by the contending devices. The signals represent the priority number of the device, which is set by switches or held in a register. When the device issues the bus request signal, it places the unique priority number on the priority bus and samples the bus signals at the same time.

This is allowed because the bus lines are encoded in such a way that the three lines can represent only four possible numbers. Each line carries the (wire-) OR of corresponding signals from all contending devices. When a device places an asserted signal on a line, the low level pulls down that line, taking precedence over the highs. Thus the signals always indicate the highest number placed on the priority bus. The priority bus signals are synchronized by an 8-MHz Constant CLocK (CCLK-) signal, which is generated on the Central Micro-processor Board. (Refer to the CMB Logic Diagram, sheet 5.)

3.2.11.1 Bus Arbitration Cycle

To minimize the number of priority bus lines required for the arbitration logic to be able to select up to 16 devices, logic is included that samples the three lines \underline{twice} during each arbitration cycle. The resulting two steps in the priority bus examination process are as follows:

- a. The priority bus signals indicate the highest number of four groups of four devices, one or more of which is requesting the system I/O bus. The group with the highest priority number on the bus qualifies to continue with the second step; any competing groups with smaller numbers may continue the bus request signal (BR-1).
- b. During the second half of the clock period, the priority bus signals indicate the highest number of the four devices within the qualified group. At the end of the clock period, the contending device with the highest priority number responds to the bus grant signal (PBG-).

After a system I/O bus device controller or the refresh circuitry has received the bus grant signal (PBG-), the responding device must monitor the following three signals to determine when the system I/O bus actually is available for use.

- Address strobe (AS-) must be negated, indicating that the 68010, or another bus master, has completed the current bus cycle
- Data transfer acknowledge signal (DTACK-) must be negated, indicating that the slave device accessed by the 68010 is no longer on the main memory data bus
- Bus grant acknowledge signal (CBACK-) -must be negated, indicating that no other peripheral device controller presently is using the system I/O bus

The winning device must wait until allthese conditions are met before it may assume control of the system I/O bus. When the conditions are met, the device taking the bus leaves its priority number on the priority bus and asserts the BGACK- signal. BGACK- is buffered by a 74S244 tristate driver (1E) and sent to the 68010 as CBACK-. There is at least a one-clock-period delay between CBACKand PBG-; it is during this period the prospective bus masters arbitrate. (A 74S240 inverter [1Y] increases the drive capability of CBACK+; signals CBACKand CBACK+ are delivered throughout the Central Microprocessor Board to enable various other signals.)

3.2.11.2 Fast Bus Grant

When the asserted bus grant (PBG-) signal was sent to the controllers, it was ORed with signal FBG- (Fast Bus Grant) in a 74LS08 AND gate (7T). The output from the gate is buffered by a 74S244 tristate driver (1E) and then placed on the system I/O bus (connector J01, pin C13), to be delivered to the peripheral device controller boards. The fast bus grant signal is generated to give the controllers more time for bus arbitration during heavy DMA activity.

Signal FBG- is asserted only when a 68010 memory bus cycle is underway and the 68010 would give a bus grant anyway. FBG- is asserted on the falling edge of the K8MHZ- clock when (a) there is a bus request, (b) the address strobe is active, and (c) timing signal CSTOF+ still is low. Although the resulting window is not very long, it can help to speed up heavy DMA activity.

3.2.12 Address Space Decoding Logic

Some devices on the Central Microprocessor Board are meant to be read from and written to, and others are meant to be read-only or write-only. (Table 3-5 shows the address space decoding.) This allows a simplification in design, in that a READ or a WRITE strobe may be combined with the chip enable strobe going to the restricted device.

	Table 3-5.	Address Space Decoding
ADDRESS (HEX)	READ/WRITE	DEVICE ENABLED
OXXXXX	Both	PROM at reset, main memory after first WRIT
2XXXXO	WRITE	Test Point TSTOL
2XXXX2	WRITE	Test Point TSTERL
2XXXX4	WRITE	Inhibit parallel port and parity
2XXXX6	WRITE	Parity data forced
2XXXX8	WRITE	Inhibit serial port drivers
2XXXXA	WRITE	Turn on LED
2XXXXC	WRITE	Inhibit parity response
2XXXX2	READ	Memory Parity Error Upper Register
2XXXX4	READ	Memory Parity Error Lower Register
2XXXXA	READ	CMB Status READ
2XXXXE	READ	CMB general status READ
4xxxxx	READ	System PROM
60XXXX	Both	SCC I/O (serial ports 0 and 1)
62XXXX	Both	PI/T I/O (parallel port)
64XXXX	WRITE	Baud Rate Selector
68XXXX	Both	NVRAM READ/WRITE
6AXXXX	READ	NVRAM store
6CXXXX	READ	NVRAM recall
70xxxx	WRITE	Floppy address counter reset
72XXXX	READ	Floppy status (read only)
76XXXX	WRITE	Floppy control latch WRITE
78XXXX	Both	Floppy controller chip select
7axxxx	Both	Floppy buffer READ/WRITE
8XXXXX	WRITE	MMU base WRITE
AXXXXX	Both	MMU limit write/status READ
CXXXXX	Both	System I/O bus device controllers

This is done with decoder chip 7Z. (Refer to the CMB Logic Diagram, sheet 9.) The chip decodes A20+A, A21+A, A22+A and A23+A, the four high-order address bits from the 68010 (via address drivers). Three decoder outputs are active during READ cycles only; four outputs are active during WRITE cycles only; and one output is active during both READ and WRITE cycles (MDENB+). Except for the MDENB+ (Memory Data ENBable) line, the output lines are enabled only in the 68010 supervisor mode (when signal FDC5R6+ [Function DeCode 5 oR 6, explained in paragraph 3.2.2] is asserted). An address space decoding diagram is shown in figure 3-3.

TBD

Figure 3-3. Address Space Decoding Diagram

3.2.12.1 READ Cycle Decoding

When the decoder chip (7Z) is used for READ cycles, signal RD- must be active, and BOOT+ must be inactive (low), to enable the decoder. BOOT+ active enables the Boot PROMs, rather than the system memory, for all addressing at reset. When the first WRITE cycle is processed, however, BOOT+ is negated; this allows the initial vectors to be obtained from the PROMs at reset time and then to be modified after that. Signal RD- is an inverted R/W- (Read/Write) signal from the 68010.

Another decoder, a 74S138 (4K), generates two status READ strobes, using loworder address bits A01+A, A02+A, and A03+A, from the 68010. These strobes are used to read the CMB status register and the parity error address.

3.2.12.2 WRITE Cycle Decoding

Most of the WRITE cycle outputs from the address space decoder chip (7Z) are used to clock data into registers on the trailing edge. To ensure that the data still is valid when clocked into a register, signal CDS- (instead of a derivative of the address strobe [AS-]) is used as one of the enable inputs for the decoder chip. (CDS- must be asserted to allow WRITE cycle decoding.) CDS-(Combined Data Strobe) is the OR of the upper and lower data strobes (CLDS- and CUDS-) from the 68010. The enable inputs of the WRITE cycle decoder also require an active WR- (WRite) signal, which is the buffered R/W- control signal from the 68010.

3.2.12.3 Memory Select Decoding

Signal MDENB+ (Memory Data ENaBle, explained in paragraph 3.2.15.3), from the address space decoder chip (7Z), goes to the memory array boards. (Refer to the CMB Logic Diagram, sheet 9.) MDENB+, in combination with MAD17+ through MAD20+, on the memory array boards, selects one of a maximum of six boards. MDENB+ is enabled by one of three possible conditions.

The three conditions are as follows:

- A peripheral has control of the system I/O bus all communication with the Central Microprocessor Board is through memory; signal CBACK- (Cpu Bus grant ACKnowledge, explained in paragraph 3.2.11) is active during this condition and is an input to the address space decoder (7Z).
- o The 68010 is in user mode all accesses are to memory rather than I/O; signal CFC2+A (Function Code 2 from the 68010, explained in paragraph 3.2.2) is inactive during the user mode and is an input to the address space decoder (7Z).
- o The 68010 is in supervisor mode except during boot, all accesses to addresses 000000 through 1FFFFF are to memory. FDC5R6+ (Function DeCode 5 oR 6, explained in paragraph 3.2.2) is active during the supervisor mode and is an input to the address space decoder (7Z).

When MDENB+ is inactive, column address strobes are prevented from going to the memory array boards, thereby deselecting the main memory. (A column address strobe is one of two enable signals required by a dynamic RAM chip--the other signal is the row address strobe [both are explained in paragraph 3.2.15].)

3.2.12.4 Local I/O Decoding

Some of the local I/O devices (e.g., floppy disk controller, PI/T, etc.) must receive single, rather than separate, enable strobes for both READ cycles and WRITE cycles. These are provided by the local I/O decoder chip (8Z). (Refer to the CMB Logic Diagram, sheet 10.) Address bits A04+A, A05+A, A08+A, and A17+A through A23+A are input to the decoder chip. In addition, READ signal RD-, Combined Data Strobe CDS-, Processor Data Transfer ACKnowledge strobe PDTACK-, and the Function DeCode 5 oR 6 (FDC5R6+) control signal are input to the local I/O decoder chip to further qualify the chip's output signals. The resulting strobes, with their qualifying (hex) addresses, are as follows:

CMBRE- (read CMB status)	2XXXXX/3XXXXX
Z80IO- (byte mix/floppy control)	6XXXXX/7XXXXX
SCCCE- (serial ports)	60XXXX
PITCE- (parallel port)	62XXXX
ENBRREG- (Baud rate selector)	64XXXX
NVRCE- (NVRAM READ/WRITE)	68XXXX
NVRST- (NVRAM store)	бахххх
NVRRC- (NVRAM recall)	6CXXXX

3.2.13 Byte Interface Control Logic

An 8-bit-wide local data bus is present on the Central Microprocessor Board. All the local byte-wide chips operate off this bus. These include the Floppy Disk Controller (FDC), the Serial Communications Controller (SCC), the Parallel Interface/Timer (PI/T), and the non-volatile RAM (NVRAM). The byte-wide local data bus is controlled by strobes LUDS- (Local Upper Data Strobe) and LLDS-(Local Lower Data Strobe). (Refer to the CMB Logic Diagram, sheet 25.)

The 16-bit data bus from the 68010 is multiplexed by two 74LS245 bidirectional buffers (2L and 3L), whose direction is controlled by WR-, the READ/WRITE signal. A buffer is enabled when the 68010 is either accessing local I/O (Z80IO-active) or processing an Interrupt ACKnowledge Level 5 (IACKL5- active).

3.2.14 Memory Address Bus

The address bus to the memory array boards consists of eight multiplexed address lines and four memory array board select lines. (The multiplexed address lines are required by the dynamic RAM chips [explained in paragraph 3.2.15]. High-order ["column"] addresses or low-order ["row"] addresses are placed on the multiplexed lines; signal CADSEL+, from the dynamic memory support logic, selects between the two groups.) The address lines and board select lines are explained in the following paragraphs.

3.2.14.1 Memory Array Board Selection

MAD17+ through MAD20+ are the memory array board select strobes. (Refer to the CMB Logic Diagram, sheet 39.) The strobes are generated in one of two ways:

- When the 68010 is in the supervisor mode, or a system I/O peripheral device controller is the bus master, system I/O bus address bits AB17-through AB20- are driven onto the memory address bus; the driver is a 74S240 tristate inverter (1Y), enabled by signal PAENB- asserted.
- When the 68010 is in the user mode, address bits A17+A through A20+A, translated by the memory management unit, are driven onto the memory address bus; the driver is a 74S244 (1Z) enabled by PAENB+ inactive.

Signal PAENB- (Physical Address ENaBle) is derived from the OR of CBACK- and CFC2-. (The two signals are ORed in a 74LS08 AND gate [7W, CMB Logic Diagram, sheet 38].) PAENB- active indicates either the 68010 is in the supervisor mode (CFC2- active) or a peripheral controller is the bus master (CBACK- active). Address bits MAD18+ through MAD20+ select a memory array board, and bit MAD17+ selects between two 128K-byte banks of 64K X 1 RAM chips on the board. Note that signal MDENB+ also must be low for a memory array board to be selected.

3.2.14.2 Memory Address Bus Multiplexing

When the dynamic RAM memory timing circuit first asserts the row address strobe (MRAS+), the CADSEL+ (Column ADdress SELect) strobe is low. (Refer to the CMB Logic Diagram, sheets 37 and 38.) This enables a 74S244 tristate driver (IV) and places low-order address bits AB01- through AB08- onto the memory address bus (which carries the multiplexed address bits [MAI- through MA8-] to the memory array boards). Address bits AB01- through AB08- come from one of the following three sources. (Refer to the CMB Logic Diagram, sheets 12, 13 and 24).

- The 68010, via a 74LS244 driver (4S)
- A system I/O bus peripheral device controller, via connector J02
- The dynamic RAM refresh circuitry, via 74LS240 inverters (1T and 1Y)

Then, after a 60-nanosecond delay, CADSEL+ goes high and the 74S244 driver (1V) delivering the low-order address bits turns off. Now the memory address bus receives high-order addresses from one of the following two sources.

- System I/O bus address bits AB09- through AB16-. These come from the 68010, when it is in the supervisor mode, or from an I/O bus peripheral device controller, when that controller is the bus master; the driver is
- а

74S244 (1W) enabled by an OR of those conditions (CBACK+ or CFC2+A high).

• Address bits A09+A through A16+A. These are translated addresses from the memory management unit (explained in paragraph 3.2.16.5) and are selected with the 68010 in the user mode; the driver is a 74S240 (IX, CMB Logic Diagram, sheet 30) enabled by a NAND of signals PAENB- and CADSEL+ high.

3.2.15 Dynamic Memory Support

The memory array boards, which plug into the Central Microprocessor Board, use dynamic RAM chips. Interfacing with these is more complex than for static RAM chips. This is because the dynamic RAM chips require address multiplexing, for which timing is more critical. The dynamic RAM chips are arranged internally in two-dimensional arrays of bits; each has a row address and a column address. Both addresses share common lines; hence the requirement for the multiplexing of addresses.

The multiplexing of addresses requires one more pin for control than on static RAM chips. The chip select of a static RAM chip has been replaced by row and column selects. These indicate which address is on the address lines when the chip is selected. (The low-order address bits from the bus master become the row address, and the high-order bits become the column address.)

Input signals to the row and column selects are called row and column address strobes. The timing of the strobes and the address bits is critical. The row address has to be held long enough to satisfy setup and hold-time constraints; then it has to be removed quickly enough to let the column address set up.but the memory timing circuitry needs to keep the row address timing short to meet the memory cycle time requirements. The timing for the control signals is presented in figure 3-4.

	ROW	COLUMN	RC	DW	COLUMN
Address					
ROW SELECT L					
COLUMN SELECT L					
WRITE L					
DATA OUT					
DATA IN					
	READ cyc	cle		WRITE	cycle
L = Low = asserte	ed signal				

Figure 3-4. Timing Relationships for the Signals of a Dynamic RAM Chip

Finally, unlike static RAMs, dynamic RAM chips cannot retain data indefinitely without external support logic. This is because data is stored as electrical charge in small "capacitors," and the charge tends to dissipate over a period of time. Hence it is necessary to refresh memory periodically.

For these reasons, and because the memory system is designed to operate without 68010 wait states, memory timing can be rather involved. To make the design less critical, however, the memory timing circuitry has been centralized on the Central Microprocessor Board, as opposed to including separate timing circuits on each memory array board. A simplified block diagram of the dynamic memory support subsystem is shown in figure 3-5. The following paragraphs describe the memory timing circuitry.

3.2.15.1 Memory Timing

High-speed logic multiplexes the eight address lines from one of three sources: the high address bits, the low address bits, or the refresh counter (discussed in subsequent paragraphs). Delays are generated from a tapped delay line and are designed to satisfy the setup times for the row and column addresses. An asserted address strobe from either the 68010 or a peripheral device controller indicates the beginning of a memory bus cycle.

A 100-nanosecond, 10-tap delay line (DL2, CMB Logic Diagram, sheet 37) determines all the subsequent memory timing. The Address Strobe (AS-) comes from Central Microprocessor Board connector J02, pin A31. Either a system I/O bus peripheral device controller or the 68010 can drive AS-. AS- is inverted by a 74S240 (6X) and sent to the delay line.

3.2.15.2 Row Address Strobe

Signal MRAS+ (Memory Row Address Strobe) is driven onto the memory array bus connector (J03, pin Cl2) by a 74AS1000 NAND gate (6V). The gate ORs two possible conditions to create MRAS+: One input to the gate is an AND (in a 74S00 NAND gate [8X]) of the 10-nanosecond delay line tap output and the complement of signal AS-. The resulting delay of MRAS+ provides an additional 10 nanoseconds of row address strobe precharge for the dynamic RAMs. (Chip specifications require a minimum quiescent time for the precharge of internal circuits.)

The other input to the NAND gate is refresh signal REFADRS- (REFresh ADdRess Strobe)-since memory refresh cycles need only row addresses, REFADRS- inputs directly to the gate to create the MRAS+ signal. When MRAS+ is asserted, the low-order address bits are multiplexed onto the eight memory address bus lines, by two 74S244 tristate drivers (1V and 1W, CMB Logic Diagram, sheet 38).

3.2.15.3 Column Address Strobes

During non-refresh cycles, signal CADSEL+ (Column ADdress SELect), from the 50nanosecond delay line tap, disables the row addresses and enables the column addresses. These are now multiplexed onto the memory array bus address lines. TBD

Figure 3-5. Simplified Block Diagram, Dynamic Memory Support Subsystem

Because 8-bit or 16-bit (byte or word) data are accessible in one memory cycle, two column address strobes are required: MCASL- (Memory Column Address Strobe Lower) and MCASU- (Memory Column Address Strobe Upper). Two 74S22 NAND gates (6Y and 6Z) decode both column address strobes: one pair is for memory write cycles, and one pair is for memory read cycles, determined by the R/W- (Read/ Write) signal. The strobes are driven onto connector J03, pins C15 and C16.

A read cycle upper/lower column address strobe is gated by four signals:

- o the 80-nanosecond tap from the delay line (high),
- o MRD+ (Memory ReaD) asserted,
- o MDENB+ (Memory Data ENaBle) asserted, and
- o the appropriate upper or lower data strobe (MUDS+ or MLDS+) asserted.

A write cycle upper/lower column address strobe is also gated by four signals:

- o the 80-nanosecond tap from the delay line (high),
- R/W+ (Read/Write) asserted (high),
- o MWINH- (Memory Write INHibit) inactive, and
- o the appropriate upper or lower data strobe (MUDS+ or MLDS+) asserted.

Signal MRD+ is the complement of R/W+; R/W+ is the complement of R/W-. R/W- comes from the system I/O bus and, when asserted (low), indicates that either the 68010 or an I/O bus peripheral device controller is doing a write cycle.

Signal MDENB+ inactive deselects the memory by preventing the column address strobe from going to the memory array boards during an access beyond the memory address space (above address 1FFFFF [hex] [paragraph 3.2.12]). Signal MWINH- asserted prevents main memory from being written during certain situations (by preventing a write strobe from producing a column address strobe).

Signals LDS- (Lower Data Strobe) and UDS- (Upper Data Strobe) come from the system I/O bus and are generated by the 68010 or an I/O bus peripheral device controller. The two signals are inverted by a 74S240 tristate inverter (10Y) to generate signals MLDS+ (Memory Lower Data Strobe) and MUDS+ (Memory Upper Data Strobe). Note that, during a 68010 write cycle, the data strobes are active one clock cycle after the address strobe is asserted. This means that the data strobes, rather than the 80-nanosecond delay line output, become the main gating factor into the 74S22 NAND gates (6Y and 6Z). Figure 3-6 shows the memory control timing.

3.2.15.4 Memory Refresh

Dynamic memory refresh is accomplished by reading each cell in the 64K-bit RAM memory periodically, about every 4 milliseconds.

TBD

Figure 3-6. Memory Control Timing Diagram

To make this burden more tolerable, dynamic memory chips are arranged in twodimensional arrays of bits, so that all bits in a row are refreshed when one bit in that row is read. Hence, refreshing requires only that each row of bits be read every 4 milliseconds. Since a 64K-bit RAM chip is arranged in arrays of 256 X 256, refresh must be done at the rate of 256 reads per refresh period (1 read per 15 microseconds).

3.2.15.5 Refresh Address and Request Generation

To generate a sequence of addresses for refresh cycles, a 74LS393 4-bit binary counter (2T) is used as a modulo (divide by) 256 counter. (Refer to the CMB Logic Diagram, sheet 24.) One of the 4-bit counters in the 74LS393 is clocked at the end of the refresh cycle by signal REFADRS+ (REFresh ADdResS), and the other counter is clocked by the overflow from the first counter. With each tick of the refresh clock, the counter advances and the controller generates a memory request at the new (row) address. The outputs from both counters are driven onto the system I/O bus (by a 74S240 [1T]). (The counter may be cleared and held by pulling RAMDIS- high [may be done for testing purposes].)

A 74LS161 4-bit synchronous counter (9J) is used to generate a RFREQ+ (ReFresh REQuest) signal every 15 microseconds. (Refer to the CMB Logic Diagram, sheet 24.) The counter is clocked by a continuous, 1-megahertz clock (K1MHZ+), and the input is hard-wired for binary 1. When the count reaches binary 15, the ripple carry output goes high. Inverted by a 74LS04 (10V), this output is fed back to the LOAD input of the counter. Consequently, on the next low-to-high transition of the K1MHZ+ clock, the counter is loaded with an input value of binary 1, the ripple carry output goes low, and counting resumes from 1.

The ripple carry output is asserted (high) for 1 clock cycle, or 1 microsecond. This is ANDed with the negative-going half cycle of the clock to produce the RFREQ+ signal, with a 500-nanosecond assertion time. (Jumper R can be inserted to eliminate refresh cycles during testing.)

3.2.15.6 Refresh Arbitration

All refresh cycles require a system I/O bus arbitration procedure. The refresh circuitry has the highest priority on the system I/O bus; but this circuitry will not get the bus until the current bus master gives itup. (Refer to the CMB Logic Diagram, sheet 23.)

All system I/O bus arbitration, including refresh arbitration, is synchronized with an 8-megahertz clock (K8MHZ-). In the refresh arbitration circuitry, this clock toggles five 74S112 J-K flip-flops (5G, 5H and 5J). The flip-flops form a simple state machine that sequences through the signals required for system I/O bus arbitration.

The memory refresh arbitration cycle begins when the refresh request (RFREQ+) signal (explained in paragraph 3.2.15.5) goes high. The asserted RFREQ+ signal is latched by one the 74S112 flip-flops (5J), and the Q output is driven onto the system I/O bus by a 74S38 open-collector NAND gate (2G); there it becomes the Bus Request (BR-) signal and is sent to the 68010.

When the 68010 returns the BGNT-A (Bus GraNT) signal, and the current bus cycle is not an interrupt acknowledge cycle, signal SRFSHFO+ is created in a 74LS260 NOR gate (7J). SRFSHFO+ is latched by another of the flip-flops (5G). The Q output pulls down the three bus priority lines (BPRO-, BPR1- and BPR2-) through three 74S38 open-collector NAND gates (2G). (The bus priority lines are discussed in paragraph 3.2.11.) Note: the interrupt acknowledge signal (IACK+) is factored into SRFSHFO+ because the bus priority lines also are used by the peripheral device controllers for interrupt acknowledge arbitration.

When the current bus master cycle has completed (indicated by MAS+ and CBACK+ released), signals BGACK- (Bus Grant ACKaowledge), IBGACK- (Internal Bus Grant ACKnowledge) and REFADRS+ (REFresh ADdRess Strobe) are created by the remaining flip-flops (5G and 5H) according to the timing diagram in figure 3-7.

Signal BGACK-, driven by a 74LS38 open-collector NAND gate (8J), notifies all peripheral device controllers and the 68010 that the system I/O bus is in use; IBGACK- enables the refresh address on the I/O bus; and REFADRS- generates a row address strobe to the memory array boards.

In summary, the sequence of events that takes place for a refresh cycle is as follows:

- o Fifteen microseconds elapse, and the refresh arbitration circuits request the system $\ensuremath{\text{I/O}}$ bus.
- o System I/O bus arbitration takes place, and, after the current cycle is completed, the system I/O bus is granted.

- The refresh circuitry acknowledges the bus grant and drives the modulo 256 counter output (8 bits) onto the system I/O bus.
- o The refresh circuitry issues a row address strobe, 250 nanoseconds in length, to the memory array boards.
- o The refresh circuitry releases the system I/O bus.
- o The modulo 256 counter is incremented.

3.2.16 Memory Management Unit

A Memory Management Unit, or MMU, on the Central Microprocessor Board, includes the necessary hardware for the implementation of the memory management scheme used by the operating system software. The MMU hardware provides for the two cooperating memory management techniques known as segmentation and swapping.

3.2.16.1 Segmentation

One function of the MMU is to logically partition system memory into a set of variable-length, numbered segments. To achieve this the MMU translates logical addresses into physical addresses. (Logical addresses are the outputs of the 68010 address lines; physical addresses are real memory locations, including RAM, ROM and memory-mapped I/O addresses.)

TBD

Figure 3-7. Refresh Timing Diagram

The starting location and length of each segment are defined by the contents of segment registers on the Central Microprocessor Board (CMB). A logical address from the 68010 specifies the segment number and the offset into that segment. The content of the selected segment register then determines the actual memory location to be accessed by the 68010. (A simplified block diagram of the MMU is shown in figure 3-8.) Segmentation facilitates the exchange of programs between main memory and a disk, a process called "swapping."

3.2.16.2 Swapping

Another function of the MMU is to allow programs located on a disk to be transferred to the system (main) memory for execution. This ability is necessary when there is limited main memory (as there always is) and a multiprogramming environment is desired. Swapping works in conjunction with segmentation; it is transparent to the programmer (or user).

"Swapping" is the term used because segments in main memory can be exchanged with segments on the disk. However, unless a segment in main memory has been written to, there is no point in wasting overhead storing it on the disk if an image of the segment already exists there. The reporting of a segment having been written to is yet another function of the MMU hardware.

3.2.16.3 Other MMU Functions

The MMU will report (flag) user access violations of the physical address space to the operating system. This occurs when an attempt is made to do one of the following accesses.

- o A write to a read-only segment
- o An instruction fetch from a data segment
- o An access to a non-existent segment
- o An access to an address beyond the length of a segment
- o An access to an address beyond the end of a stack
- o An access to an address in the warning area of a stack

(The MMU also will flag separately any legal write cycle to any segment, for the reason explained in paragraph 3.2.16.7.) Each of these six violations, when detected, causes the following three major events to occur, in the order presented.

- a. A write cycle to main memory is prevented.
- b. A bus error condition is created, forcing the 68010 to process an exception and force the program to branch to the appropriate service routine in the operating system software.
- c. The latched violation flags are read by the system software to determine the cause of the MMU error.

TBD

Figure 3-8. Simplified Block Diagram, Memory Management Unit

All of these detection functions can be set in CMB hardware. (A logical block diagram of the MMU error detection and status reporting functions is shown in figure 3-9.) How the CMB hardware performs these and the other functions discussed in previous paragraphs is explained in the following paragraphs.

3.2.16.4 Supervisor and User Access of the MMU

It is important to remember that the MMU is in use only while the 68010 is in user mode; and the base address, limit address and segment attribute registers (described in subsequent paragraphs), which are part of the MMU, can be updated only in supervisor mode. Also, all DMA (Direct Memory Access) transfers are physical address transfers and do not use the MMU.

Address translation (also called address mapping) by the MMU when the 68010 is in user mode and no DMA transfers are in progress is enabled by signals PAENB-(Physical Address ENaBle) high and PAENB+ low. PAENB+ low also enables the MMU errors (described in paragraph 3.2.16.8). (Refer to the CMB Logic Diagram, sheets 30 and 31.)

TBD

Figure 3-9. Logical Block Diagram, MMU Status Reporting/Error Detection

3.2.16.5 MMU Address Translation

The MMU translates address bits A09+ through A23+ from the 68010. Bits A01+ through A08+ are not translated but go directly to the memory (thus setting the inimum segment size to 512 bytes). (Address bit A00 does not exist outside the 68010. This bit is used internal to the 68010, in conjunction with the data size specification of each instruction, to generate the two UDS- and LDS- signals [Upper Data Strobe and Lower Data Strobe]. These determine which byte of a 16-bit [word-wide] memory location is being addressed.)

The resulting address translation provides each user with eight variable-length memory segments (which are transparent to the user), in physical memory (RAM). Each segment has associated with it a 12-bit base address, a 12-bit limit address, 4 bits of segment attributes and 4 bits of segment status. These 32 bits of information (called a segment descriptor) are stored at one address in eight 74S189 16- X 4-bit storage registers (3W, 3X, 3Y, 3Z, 4X, 4Y, 4Z and 7X). (Refer to the CMB Logic Diagram, sheets 30 through 34.)

The eight registers are in parallel with respect to the address lines connected to them. Only eight of the sixteen available 4-bit registers in each of the eight storage registers are used. Hence, all of the A3 address inputs to the 74S189s are pulled low.

Each of the eight segment registers is addressed by signals MFA1+, MFA2+, and MFA3+. These come from a 74S157 1-of-2 data selector (3T). (Refer to the CMB Logic Diagram, sheet 32.) Address bits A01+A, A02+A, and A03+A are selected when the 68010 is in the supervisor mode; A21+, A22+, and A23+ are selected in the user mode. Thus, when in the supervisor mode, the 68010 addresses the segment registers to update the segment descriptors; and, when in the user mode, the 68010 addresses these registers to perform address translation. The CFC2-(CPU Function Code 2, explained in paragraph 3.2.2) signal into the data selector (3T) performs the selection. In the multi-user mode, the operating system software loads the next user's segment descriptors into the segment registers with each context switch.

Base Address

The base addresses are stored in three 74S189 storage registers (3X, 3Y, and 3Z). (Refer to the CMB Logic Diagram, sheets 30 and 31.) The operating system software does this (in the supervisor mode) by writing to the input/output address (8XXXXX [hex]) that enables signal MMBWE- (paragraph 3.2.12.2). The segment base descriptor word format is as follows:

- 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
- R X TYPE A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A09

(Attributes R, X and TYPE are explained in paragraph 3.2.16.6.) During a 68010 memory cycle, the physical addresses represented by bits A09 through A20 are obtained by summing the base address, contained in the three storage registers, with the logical addresses represented by bits A09 through A20, from the 68010.

The addition is done in three 74S283 4-bit full adders (2X, 2Y and 2Z). (Refer to the CMB Logic Diagram, sheets 30 and 31.) The summed A09 through A16 are the column addresses for the memory array (MA1- through MA8-); these are driven onto the memory address bus by a 74S240 tristate inverter (IX), enabled by the NAND of PAENB- (Physical Address ENaBle) and CADSEL+ (Column ADdress SELect). The summed A17 through A20 are the memory array bank and board selects (MAD17+ through MAD20+); these are driven onto the memory address bus by a 74S244 tristate driver (1Z), enabled by PAENB+.

Limit Address

Once a base address is established, the segment length is defined by a logical limit address, and any access that violates this limit will generate an error signal. This violation detection function is required for the prevention of user programs from accidentally (or otherwise) destroying any other users' programs located in other segments.

The limit addresses for the eight segments are stored in three 74S189 storage registers (4X, 4Y and 4Z). (Refer to the CMB Logic Diagram, sheets 32 and 33.) The system software does this (in the supervisor mode) by writing to the input/ output (I/O) address (AXXXXX [hex]) that enables MMLWE- (paragraph3.2.12.2). The segment limit descriptor word format is as follows:

- 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
- 0 0 0 0 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A09

In a 68010 memory cycle, the logical address from the 68010 is compared with the limit address stored in the 74S189 registers by three 74S85 magnitude comparators (5X, 5Y, and 5Z). These devices create signals ADEQLM+ (ADdress EQual to LiMit), when the logical address is equal to the limit address, and ADLTLM+ (ADdress Less Than LiMit), when the logical address is less than the limit.

3.2.16.6 Segment Attributes

One 74S189 storage register (3W) holds the segment attributes. (Refer to the CMB Logic Diagram, sheet 31.) When a segment is to be read only, the bit corresponding to the D03 output of the 74S189 is a logical 1 (high). If a write is attempted in that segment, then the high output of D03 will be ANDed with SEGWRT+ (SEGment WRiTe) and PAENB- to produce the MMWERR+ and MMWERR- (Memory Management Write ERRor) signals.

Similarly, when a segment is to be data only, the bit corresponding to the D04 output of the 74S189 is a logical 1. If a program fetch is attempted in that segment, then the high output of D04 will be ANDed with FDC2+ (Function DeCode, user mode) to create MMXERR+ and MMXERR- (Memory Management eXecute ERRor).

Finally, bits D01 and D02 of the 74S189 are decoded by a 74S139 l-of-4 decoder (4T) to generate four error signals, all of which translate into the Memory Management ERRor (MMERR-, explained in paragraph 3.2.16.8) signals.

These are the ABSEG- (ABsent SEGment) and SEGDC(X)- (SEGment DeCode) signals:

D02	D01	SIGNAL	EXPLANATION
0	0	ABSEG-	Generates a memory management error (MMERR-) when an absent segment is addressed
0	1	SEGDC1-	Generates a memory management error when the logical address is equal to or greater than the limit address
1	0	SEGDC2-	Generates a memory management error when the logical address is less than the limit address. Used for stack overflow
1	1	SEGDC3-	Generates a memory management error when the logical address is less than or equal to the the limit address. Used for stack overflow (less than) and for warning of an impending stack overflow (equal to)

3.2.16.7 Segment Status

BIT

Each MMU segment has an associated 4-bit status word that is readable by the 68010 in supervisor mode. The status word is generated and then stored in a 74S189 storage register (7X) during the time a segment is accessed (in the user mode). (Refer to the CMB Logic Diagram, sheet 34.) The status word is not decoded. Each bit in the status word, when a logical 1, means the following:

EXPLANATION

D01	A segment has been written to (not an error condition)
D02	A segment execute error has occurred (error)
D03	A segment write error has occurred (error)
D04	A segment limit or absent segment error has occurred (error)

The status word, driven onto the buffered data bus (DBOO- through DBO3-) by a 74S240 tristate inverter (6X), is enabled by signal MMSTRE- (Memory Management STatus REad). The status word is read by the system software after a memory management error has occurred, to determine which of the foregoing three error conditions has taken place (DO2, DO3 or DO4).

Bit D01 of the segment status word is the one bit in the word that is not used for reporting an error condition. In a multiprogramming system that uses program swapping (such as this one), a record must be kept of any segment having been written to, or modified. This is so that, when swapping occurs, the contents of that segment will be stored on a disk (backing store) instead of being overwritten by the incoming program. Hence the segment status word is read by the system software during context switch to check for the segment-written bit before loading the next program.

(Refer to the (MB Logic Diagram, sheet 34.) The W output of a 74LS151 l-of-8 data selector (7V) is the input to the segment-written bit of the 74S189 (7X). The W output always is high while the 68010 is in the supervisor mode. This is to allow the segment-written bit to be initialized before the 68010 switches to the user mode.

In the user mode, when a segment is written to, W is goes low and is stored in the 74S189. If the segment subsequently is read, then W will be the inverted value of the flip-flop (7S), which has been storing the segment-written bit of the 74S189. Thus the segment-written bit is preserved, even when a segment-read cycle occurs during the same segment access period. Timing signal CSTOF+ clocks the segment-written bit, in the status word register, into the flip-flop at the beginning of each memory access cycle.

A 74LS10 NAND gate (8S) and a 74LS08 AND gate (7W) create a write pulse for the status word register during user mode access or supervisor mode initialization. These gates AND signal CSTOF+ with PAENB- and the complement of CST1F+ to produce a 125-nanosecond pulse. The pulse is gated through to the 74S189 status word register (7X) Write Enable input during a user mode memory access. During a supervisor mode write to the base address register, however, MMBWE- asserted provides the Write Enable input to the status word register.

Signal SEGWRT+ (SEGment WRiTe) is asserted when a memory write cycle occurs during the user mode. SEGWRT+ generates the Memory Management Write ERRor signal (MMWERR+/MMWERR-) described in paragraph 3.2.16.8. This can occur only when the bit corresponding to output D03 of the 74S189 segment attribute register (3W) is set (refer to paragraph 3.2.16.6).

3.2.16.8 MMU Error Generation

The IvMERR- (Memory Management ERRor) signal is generated by any one of six MMU error conditions, as listed in paragraph 3.2.16.3. A 74S30 NAND gate (10X) ORs those conditions. (Refer to the CMB Logic Diagram, sheet 35.) MMERR- goes to the memory array stack via connector J03, pin Cll. If the signal is asserted at the selected memory array board, then the PDTACK- (Processor Data Transfer ACKnowledge, required by the 68010 to complete a memory cycle) signal is block-ed from returning to the Central Microprocessor Board; the absence of PDTACK- creates a bus error exception signal, which is sent to the 68010, as described in paragraph 3.2.10.

Signal MMERR+ is latched and held by a 74LS109 flip-flop (10R) at the end of the current cycle. The latched error becomes signal MMERF+ (Memory Management ERror Flag) and is read in a (MB status read cycle, as described in paragraph 3.2.4. The error is reset at the end of the read, because the input of the flip-flop is low from CMBSTRE- ((MB STatus REad) asserted.

Signal SEGOVF- (SEGment OVer Flow) is generated by two MMU error conditions:

a. The memory access is a normal program fetch or data access (indicated by SEGDC1+ asserted), and the address is equal to, or greater than, the limit address (indicated by ADLTLM+ inactive).

b. The memory access is a stack access (indicated by SEGDC2- or SEGDC3asserted), and the address is less than the limit address (the stack address is out of bounds, indicated by ADLTLM+ asserted).

SEGOVF-, ORed with ABSEG-, produces the SAERR- (Segment Access ERRor) signal, which is written to the segment status word register, as described in paragraph 3.2.16.7. (ABSEG- also is one of the ORed error conditions that generates the MMERR- signal.)

Signals MMWERR+ (Memory Management Write ERRor) and MMXERR+ (Memory Management eXecute ERRor) are inverted by two 74S00 NAND gates (8X) to produce signals SWERR- (Segment Write ERRor) and SXERR- (Segment eXecute ERRor).

Signal SSWARN- (Stack Segment overflow WARNing) is the NAND (74LS08 [9S] and 74LS04 [7R]) of SEGDC3+ and ADEQLM+ (logical ADdress EQual to LiMit address). SSWARN- indicates a stack segment is in the warning area (i.e., the last 512 bytes before overflow). (SSWARN- is one of the ORed error conditions that generates the MMERR- signal.)

SSWARN- also is latched and held by a 74LS109 J-K flip-flop (7S) (to become SSWARNF- [Stack Segment overflow WARNing Flag]) until the flip-flop is read by a CMB STatus REad (CMBSTRE-) signal. The flip-flop then is reset at the end of the status read cycle, when the K- input is low from the CMBSTRE- signal.

Signal RAMDIS- (RAM DISable) is provided to disable the MMU registers during "bed of nails" testing. (Refer to the CMB Logic Diagram, sheet 30.) When the input of the 74LS04 inverter (4V) is pulled low by the tester, RAMDIS- goes high and disables the outputs of the 74S189 storage registers in the MMU.

3.2.17 Serial Ports

The following paragraphs cover detailed information on the serial interfacing of the Model 4108 Base Unit to peripheral devices. Controller circuitry that will support two serial I/O ports is contained on the Central Microprocessor Board, inside the Base Unit. Each port is an independent, O- to IM-bit-persecond, full-duplex RS 232 channel. The ports can have different baud rates for transmitting and for receiving, and each port can support a printer, modem or terminal. Figure 3-10 shows a simplified block diagram of the serial port circuitry, and the following circuit descriptions begin with a brief review of some basic serial interfacing principles.

3.2.17.1 Serial/Parallel Conversion

The serial port controller contains a bus interface through which the 68010 can send commands to the ports, read port status, and access input and output data registers in the ports. An interrupt line notifies the 68010 of the completion of an operation. As in any serial port, a conversion takes place between the serial and the parallel data streams. Hence the interface with the 68010 is a parallel interface through which eight data bits are transmitted during a single transaction.

TBD

Figure 3-10. Simplified Block Diagram, CMB Serial Ports

The interface with a serial peripheral device, on the other hand, is a serial interface in which those same data bits are transmitted on a single output line or received on a single input line, one bit at a time. The conversion occurs in the LSI serial communications controller chip, on the Central Microprocessor Board. The serial communications controller chip is a Zilog 8530 (2C). (Refer to the CMB Logic Diagram, sheet 28.) The chip is a byte-wide device, residing on the byte-wide I/O data bus (described in paragraph 3.2.13). It is a multiprotocol and dual-channel device; and each independent channel, or port, can handle 0- to 1M-bits-per-second data transfer rates and full-duplex operation. A simplified block diagram of the 8530 chip is presented in figure 3-11.

Within the serial communications controller chip, an output register is loaded in parallel from the byte-wide data bus. This register, in turn, provides a parallel dump to a shift register. Hence data is loaded into the parallel register, then passed to the shift register, where the bits are collected until the register is full. Conversely, input data from a serial peripheral device are passed in parallel from an input shift register to an input data register and then to the 68010, via the byte-wide data bus.

TBD

Figure 3-11. Simplified Block Diagram, 8530 SCC Chip

Serial Data Reception

The receive and transmit sections each have separate data registers because of a need to buffer data in transit through the port. There is a variable delay between the receipt of a byte-wide datum from a peripheral and the availability of a 68010 bus cycle that will accept that datum. Hence, the receive register accepts the datum and holds it during the time the input shift register is receiving the next character. As each successive bit of the next arriving character appears, the shift register shifts its present content to make room for the new datum.

This prevents the leading bits of the next character from overwriting the received datum. When the final bit of a character is received, the completed byte passes to the input buffer register, thus freeing the shift register to accept the next byte of serial information.

Serial Data Transmission

A similar, but reverse, series of events occurs during the transmit cycle. The benefit in this case stems from the elimination of idle time between character bytes on the serial output line. The moment the final bit of a character byte leaves the output port, a new data byte is moved into the output shift register from the output buffer register. Now the 68010 has the entire 8-bit character interval to reload the output buffer register. This ability to eliminate idle time between characters is of fundamental importance in synchronous communications protocols.

3.2.17.2 Communications Protocol Selection

A communications protocol is a convention for data transmission that includes at least the following functions.

- o Timing
- o Formatting
- o Control
- o Representation of data

The Model 4108 Base Unit provides flexibility in configuring the transmit and receive parameters of the serial ports for various protocols. The ports can support three catagories of serial protocols. Each port can be configured as

- o synchronous,
- o standard asynchronous, or
- o asynchronous, with programmable split baud rate (i.e., transmit and receive can be at different rates, from 150 baud to 19.2K baud).

Synchronous Protocol

In the synchronous mode, each successive datum in a data stream is controlled by a master data clock. Hence the clock controls not only the bits within a character byte, but the character-to-character spacing as well. (One benefit of this method is higher communication speed, as an entire block of data may be exchanged, with only normal bit spacing between characters.) The master clock is received as an additional signal, separate from the incoming data stream. This clock appears at the Port A DB-25 connector (J09, pin 17) as signal RTXCA+ (Receive/Transmit Clock, Port A).

From there it is routed, via a 74LS153 l-of-4 data selector (2J), to the RTXCAinput of the serial communications controller chip, or SCC. (Refer to the CMB Logic Diagram, sheets 28 and 29.) A similar path is found from the Port B DB-25 connector (J10, pin 17) to the SCC.

Standard Asynchronous Protocol

The standard asynchronous mode selects the 3.6864 MHz clock from a local oscillator (2K) and feeds that to the SCC via the same data selectors (2H and 2J). In asynchronous serial data transmission, each character is treated as an individual message; each appears in the data stream at an arbitrary time. Thus it is the responsibility of each character to inform the receiving serial port of the beginning and the end of that character. It does this with start bits and stop bits. When no data is being transmitted, the data line carries a logic 1 level (high voltage).

When a datum appears on the line, the first bit received is a logic 0 (low); this commands the SCC to begin sampling the datum. The next 8 bits are data bits, and the final 1, 1-1/2, or 2 bits are stop bits. The stop bits are always at logic 1 (high).

Split Baud Rate Asynchronous Protocol

The split baud mode allows serial transmission at one data rate and reception at another. The mode is selected by system software using data bits CD02+ and CD03+ (or CD00+ and CD01+ for Port B). These data bits are latched in a 74S373 transparent latch (3K). Refer to the CMB Logic Diagram, sheet 29.) The local baud rate clock for transmitting data is selected by data bits CD05+, CD06+ and CD07+, latched in the same 74S373. The SCC is programmed directly to set the baud rate of the receive clock.

A 74LS163 binary counter (3G) divides by 8 the output of a 4.915 MHz oscillator (4G). A 74LS393 binary counter (3H) generates 8 clock rates, each equal to 16 times the frequency of the requested baud rate. These are the clocks that are selected by data bits CD05+ through CD07+.

Data bits CD05+ through CD07+ are decoded in a 74LS151 l-of-8 data selector (3J). The other data bits select which of the three possible clock sources is to be used for each port on the SCG.

They are selected by the 74LS153 data selectors that were mentioned earlier (2J and 2H). The control and data bits are available to the SCC when the SCC is selected by the local I/O address decoder (discussed in paragraph 3.2.12.4) in the Central Microprocessor Board.

3.2.17.3 Electrical Configuration Selection

To further define the asynchronous serial communications protocol used in the Model 4108 Base Unit, we separate the logical conventions from the electrical connection requirements. The electrical connections used in asynchronous protocols usually are referred to as one of the following:

- o RS-232-C
- o 20 mA current loop
- o RS-422, RS-423, or RS-449

Of these, the Base Unit uses only RS-232-C and RS-422.

RS-232-C

The RS-232-C standard originally was intended to provide a specification for using modems (modulator/demodulator) to connect remote devices to computers, via the telephone network. The standard now is used to connect the computers directly to terminals and to serial printers, in addition to modems.

The RS-232-C standard defines 21 signals and a 25-pin electrical connector for asynchronous serial data communication. In order to accommodate terminals and serial printers in addition to modems the serial port circuitry in the Central Microprocessor Board must be electrically configured for the desired peripheral device. Hence that circuitry contains several connections for jumpers to allow the necessary reconfiguration. Table 3-6 shows the signal names, their corresponding cable pin number, jumper reference letters, and the circuit board pin numbers of the pins that must be connected together by the jumper wires for a particular configuration.

Note that only kind of one cable is needed to support printers, terminals or modems. All signal switching is done on the Central Microprocessor Board via the jumpers. The RS-232 cable is a pin-for-pin connection; no signals or pins are cross-connected.

RS-422

The RS-422 standard describes the electrical characteristics of a port that is designed to allow a higher signaling rate bandwidth over longer distances than is provided by the RS-232-C. This standard defines a double-ended electrical interface that can signal at data rates well in excess of the 20-kHz bandwidth allowed by RS-232-C (20 kHz = 20K data bits/second).

Table 3-6. Serial Port Electrical Configuration Jumper Connections

PORT A:

MODEM			TERMI	NAL	PRINTER		
Name	Jumper A	Cable	Jumper A	Cable	Jumper A	Cable	
CTS	7 and 8	pin 5	7 and 9	pin 4	7 and 9	pin 4	
DSR	3 and 4	pin 6	*1 and 3	pin 20	1 and 3	pin 20	
DTR	1 and 2	pin 20	*2 and 4	pin 6	2 and 4	pin 6	
RTS	9 and 10	pin 4	8 and 10	pin 5	8 and 10	pin 5	
RXD	11 and 12	pin 3	11 and 13	pin 2	11 and 13	pin 2	
TXD	13 and 14	pin 2	12 and 14	pin 3	12 and 14	pin 3	
RNG	In Place	pin 22					
TRXC	In Place	pin 15					
DCD	In Place	pin 8					

PORT B:

MODEM			TERMINA	L	PRINTER		
Name	Jumper B	Cable	Jumper B	Cable	Jumper B	<u>Cable</u>	
CTS DSR DTR RTS RXD TXD	1 and 2 9 and 10 13 and 14	pin 6 pin 20 pin 4 pin 3	7 and 9 3 and 1 2 and 4 8 and 10 13 and 15 14 and 16	pin 6 pin 5	13 and 15	pin 20 pin 6 pin 5 pin 2	
	Jumper G		Jumper G		Jumper G		
RXD DCD TRXC		pin 3 pin 8 pin 15		pin 8	15 and 16	pin 2	
	Jumper H		Jumper H				
DCD	1 and 2		1 and 2				
	Jumper K		Jumper K		Jumper K		
D422	*1 and 2		*1 and 2		*1 and 2		

NOTE: Be sure to disconnect all unused jumper positions on port B.

*This jumper disables the RS-422 drivers.

In the Model 4108 Base Unit, only Port B can be configured for RS-422; although either port may be used as a synchronous data channel, it may be advantageous to use port B, because of the balanced link associated with the RS-422 configuration. In the serial port input/output circuitry, the RS-422 line drivers are 26LS31s (4D), and the receivers are 26LS32s (4C). (Refer to the CMB Logic Diagram, sheet 28.1.)

3.2.17.4 Addressing and Control

The 8530 SCC chip (20) is enabled with a 68010 supervisor read or write to address 60XXXY (hex). The internal registers of the SCC chip are addressed by address bits A014A and A02-fA, from the 68010. Port A is selected when A02+A is high; Port B is selected when that bit is low. Address bit A01+A. informs the the SCC that either data or control parameters are being sent.

The read and write strobes to the SCC are synchronized by ANDing their complements with the CST4F+ timing signal to meet SCC timing requirements. This is done by a 74LS51 combination gate (9M). (Refer to the CMB Logic Diagram, sheet 25.) A reset on RSTF2+ will cause both a read and a write to be sent to the SCC, creating the required reset condition. Table 3-7 shows the data bus bit patterns required for selecting the various serial port logical configurations and data rates.

Once a port has been selected and configured, and data transfer is in progress, the system software needs to be informed of when a datum has been transferred between a shift register and a buffer register in the SCC chip. This is so that a driver routine can either load a new byte into the transmit buffer or transfer the new byte in the receive buffer to the 68010.

When a byte of data has been tranferred between a buffer register and a shift register, control logic in the SCC chip activates the interrupt pin (INT-) of the chip. (Refer to the CMB Logic Diagram, sheet 28.) When this pin is low, signal INT5- (INTerrupt level 5) is encoded by a 74LS148 8-line-to-3-line priority encoder (3E). (Refer to the CMB Logic Diagram, sheet 22.) This constitutes an interrupt request to the 68010.

Thus an interrupt request level 5 is encoded on the 68010 interrupt request lines (IPLO- through IPL2-). If the priority of the interrupt is greater than the current processor priority, then the interrupt processing sequence begins. The 68010 places the interrupt priority number on the lines carrying the three least significant address bits. These are decoded by a 74LS151 1-of-8 data selector (10K, CMB Logic Diagram, sheet 22).

For priority number 5, the CVPA- (CPU Valid Peripheral Address) output of the data selector is low (active). In response to CVPA-, the 68010 internally generates a vector number that is determined by the interrupt level number. (The vector number [when multiplied by four] is the address in the lowest 1K bytes of main memory that contains the beginning address of the routine that will handle the interrupt.) The content of the vector number is fetched and loaded into the 68010 program counter, and normal instruction execution commences in the interrupt service routine.

CD03+	CD02+	CD01+	CDOO+	LOGICAL PORT CONFIGURATION
0	0	Х	Х	Port A, Synchronous
0	1	Х	Х	Port A, Asynchronous
1	0	Х	Х	Port A, Split Baud Rate
Х	Х	0	0	Port B, Synchronous
Х	Х	0	1	Port B, Asynchronous
Х	Х	1	0	Port B, Split Baud Rate
CD07+	CD06+	CD05+	CD04+	TRANSMIT BAUD RATE
0	0	0	Х	19,200
0	0	1	Х	9,600
0	1	0	Х	4,800
0	1	1	Х	2,400
1	0	0	Х	1,200
1	0	1	Х	600
1	1	0	Х	300
1	1	1	Х	150

Table 3-7. Bit Patterns for Serial Port Configuration and Data Rate Selection

DATA BUS

Note: 1 = High; 0 = Low; X = Don't care

The program now can read the status register in the SCC to determine whether the interrupt was due to the transmission or reception of data; then the 68010 can move data to or from the SCC chip.

At the same time that the priority number on the address bus was being decoded to produce CVPA-, a 74LS138 1-of-8 decoder (10L, CMB Logic Diagram, sheet 20) also decoded those address bits. The output is the IACKL5- signal. This interrupt acknowledge signal is synchronized to the system clock in a 74LS74 D flip-flop (10J). (Refer to the CMB Logic Diagram, sheet 25). The output of the flip-flop is the SCC INT- input to the SCC chip, which resets the interrupt logic in the chip.

3.2.18 Parallel Port

In the following paragraphs we discuss the interfacing of external devices to the Model 4108 Base Unit through the parallel I/O port. Controller circuitry to support the parallel port is contained on the Central Microprocessor Board, inside the Base Unit. Although the port is a general-purpose I/O channel that can be used for a variety of 8-bit parallel interfaces, it usually will be used to interface a printer with the CentronicsTM "standard" interface. The following detailed discussion assumes that such a printer is connected to the port.

The parallel port uses a Motorola 68230 Parallel Interface/Timer, or PI/I. The PI/T (5D) is a byte-wide device and resides on the byte-wide I/O data bus (described in paragraph 3.2.13). (Refer to the CMB Logic Diagram, sheet 26.) The PI/T has two 8-bit ports and also has a timer with a separate interrupt output. The PI/T is permanently configured with Port A as the output port and Port B as the input port.

3.2.18.1 Addressing and Control

The 68230 PI/T chip (5D) is enabled with a 68010 supervisor read or write to address 62XYYX (hex). This provides the PI/T Chip Select (CS-) input with an enable strobe that is the AND of signals PITCE- and CST1F+ (from a 74LS00 NAND gate [4E]. Signal PITCE- (PI/T Chip Enable) comes from the local I/O decoder described in paragraph 3.2.12.4. Signal CST1F+ is a timing signal that comes from the timing generator described in paragraph 3.2.10.1. The two signals are ANDed so that the PI/T can start the strobes on a clean clock edge (CST1F+).

The internal registers of the PI/T chip are addressed by address bits A044A through A084A, from the 68010. The read and write strobe to the PI/T is the CRNW- (CPU Read Not Write) strobe from the 68010. The pin labeled DTACK provides a Processor Data Transfer ACKnowledge (PDTACK-) signal, required by the 68010 during a bus cycle to indicate the number of wait states, if any, to insert in the cycle (this is discussed in paragraph 3.2.10). Pins HI and H2 are for input and output "handshake" strobes.

Pin H4 is tied to pin B7, which receives the high-order bit (PB07+) of the input parallel port; this is a BUSY bit from the printer, which is used to generate an interrupt. The parallel control ports are wired for interrupt level 1 (INT1-), and the timer for interrupt level 6 (INT6-).

(Although the parallel port has the lowest interrupt priority [level 1], the timer in the PI/T chip has the highest priority, next to the power fail detect interrupt. This is because the interrupt generated by that timer is used to provide the "time slices" required for multi-user operation.)

When the printer is ready toreceive a byte of data, the BUSY bit (PB07+), from the printer, goes goes high. Since this bit also enters pin H4 of the PI/T, the chip asserts the interrupt signal from the pin labeled PIRQ-. This signal signal (INT1-) is encoded by a 74LS148 8-line-to-3-line priority encoder (3E). (Refer to the CMB Logic Diagram, sheet 22.) The output of the encoder constitutes an interrupt request to the 68010. Thus an interrupt request level 1 is encoded on the 68010 interrupt request lines (IPLO- through IPL2-). If the priority of the interrupt is greater than the current processor priority, then the interrupt processing sequence begins. The 68010 places the interrupt priority number on the lines carrying the three least significant address bits. These are decoded by a 74LS151 l-of-8 data selector (10K, CMB Logic Diagram, sheet 22).

For priority number 1, the CVPA- (CPU Valid Peripheral Address) output of the data selector is low (active). In response to CVPA-, the 68010 internally generates a vector number that is determined by the interrupt level number. (The vector number [when multiplied by four] is the address in the lowest 1K bytes of main memory that contains the beginning address of the routine that will handle the interrupt.)

The content of the vector number is fetched and loaded into the 68010 program counter, and normal instruction execution commences in the interrupt service routine. The program now can write a data byte to the data register in the PI/T, for transmission to the printer.

3.2.18.2 Data Transmission to a Printer

The output data format from the parallel port is ASCII (American Standard Code for Information Interchange); it's the same format used in the serial ports. The parallel data output is asynchronous, and the data transfer rate is determined by the transfer program, which normally is interrupt driven. The drivers and receivers in the parallel port circuitry are 74LS244s (4B and 5A). (Refer to the CMB Logic Diagram, sheet 27.) These are connected to J13, the parallel port connector, which has 37 pins. Table 3-8 is a list of the J13 signals. A printer connected to the Model 4108 Base Unit parallel port typically will use the so-called "Centronics parallel interface standard." Table 3-9 gives a description of the Centronics protocol.

3.2.19 Floppy Disk Controller

Two floppy disk(ette) drives may be mounted inside the Model 4108 Base Unit of the MAI® 2000 SeriesDesktop Computer System. The driven diskettes are 5.25 inches in diameter, contain 96 tracks per inch (TPI) of diskette radius and are double-sided. Controller circuitry to support both floppy drives is provided on the Central Microprocessor Board. The circuitry provides for soft-sectored and double-density recording techniques. Figure 3-12 shows a simplified block diagram of the controller, and the following paragraphs describe the circuitry, beginning with a very brisk review of a few basic disk recording principles.

3.2.19.1 Soft Sectoring

Soft-sectoring means there are no sector holes in the diskette to identify the head position with respect to a track. Instead, a single hole provides a physical reference point, and sector information is recorded magnetically on the disk within each sector.

Each sector contains an identifier field that appears on the data stream just before the data field. To read data, the head is first positioned at the correct track, where it reads the data stream continuously. When the read/write head detects an identifier with the correct sector number, the data block following that identifier is accepted.

To write a new data block, the disk controller first reads data continuously until an identifier is located with a matching sector number. The controller then rewrites the new data over the existing data block in that sector. The identifiers, however, are never rewritten during normal operation, though the controller has the capability of writing those identifiers onto a blank diskette when that diskette is being initialized for first use. The soft-sectoring technique is so called because the system software can revise the sector format of a diskette by rewriting the sector identifiers.

Table 3-8. Parallel Port (J13) Connector Signals

PIN	PI/T SIGNAL	DRIVER/RECEIVER SIGNAL	FUNCTION
1	PAOO+	PDTOO+	
2	PA01+	PDT01+	
3	PA02+	PDT02+	
4	PA03+	PDT03+	
5	PA04+	PDT04+	
6	PA05+	PDT05+	
7	PA06+	PDT06+	
8	PA07+	PDT07+	
9	PBOO+	PDTIO+	
10	PB01+	PDTI1+	
11	PB02+	PDT12+	
12	PB03+	PDTI3+	PAPER EMPTY
13	PB04+	PDTI4+	SAFETY SWITCH
14	PB05+	PDTI5+	SELECT
15	PB06+	PDTI6+	
16	PB07+	PDTI7+	BUSY
17-27		GND	
28		DTISTB1+	
29		GND	
30		DTOSTB1-	
31-35		GND	
36		+5V	
37		N/C	

Table 3-9. Centronics Protocol

SIGNAL	DESCRIPTION	CONNECTOR (J13) PIN
Data Strobe	Sent by the Model 4108 Base'Unit to cause the printer to accept information on the data lines. The data lines must stabilize at least 50 nanoseconds before the Data Strobe is sent. The Data Strobe must be present for at least 100 nanoseconds and must be removed at least 50 nanoseconds before the data is taken from the data lines	30
Busy	Sent by the printer to indicate that the printer cannot accept data	16
ACKNLG-	Sent by the printer to indicate that a character or a function code has been accepted	28
Data Bit 1	Sent by the Model 4108 Base Unit	1
Data Bit 2	Sent by the Model 4108 Base Unit	2
Data Bit 3	Sent by the Model 4108 Base Unit	3
Data Bit 4	Sent by the Model 4108 Base Unit	4
Data Bit 5	Sent by the Model 4108 Base Unit	5
Data Bit 6	Sent by the Model 4108 Base Unit	6
Data Bit 7	Sent by the Model 4108 Base Unit	7
Data Bit 8	Sent by the Model 4108 Base Unit to control the optional character set	8
SS	Always at 0 volts	??13??
PE	Sent from the printer to indicate ar out-of-paper condition or that the printer cover is open. A positive level is logical true	n ??12??
SLCT	Sent from the printer when the +5V supply is on, the paper is loaded, the front cover is closed, and the operator has activated ON LINE	??14??

TBD

Figure 3-12. Simplified Block Diagram, CMB Floppy Disk Controller

A hard-sectored format, on the other hand, allows somewhat greater data density than does a soft-sectored. This is because no identifier field occupies space that otherwise is usable for data. However, the advantages of a soft-sectored format are many, and the double-density disk recording techniques, described in paragraph 3.2.19.2, more than compensate for the data density problem.

3.2.19.2 Double-Density Recording

The double-density recording scheme also is known as <u>MFM</u> (modified-frequency modulation) encoding. This encoding scheme may best be understood by first reviewing the Kansas City Standard (KSC) for cassette recording. The KSC encoding technique is shown in figure 3-13. A binary 0 is recorded as four full cycles of a 1200-Hz square wave. A binary 1 is recorded as eight full cycles of a 2400-Hz square wave. Clearly, with this encoding scheme the transmission rate for one data bit is 1/8 of 2400 Hz, or 300 data bits/second.

The transitions that are common to both the binary 0 and the binary 1 are used to synchronize a local oscillator to the incoming data rate, when the data are recovered from the recording. Therefore, when a transition occurs between the clock ticks, the data recovery circuitry may assume that a 1 is encoded; otherwise the circuitry may assume the code is a binary 0.

TBD

Figure 3-13. Signal Encoding and Derived Clock, Kansas City Standard

The transmission rate of the Kansas City Standard can be increased by simply using fewer transitions to encode each datum. Figure 3-14(a) shows a binary 1100 sequence encoded at a transmission rate of 1200 bits/second. Here the binary 0 requires one full cycle of 1200 Hz, and the binary 1 requires two cycles of 2400 Hz. Figure 3-14(b) shows the standard pushed to the maximum data rate of 2400 bits/second. In this scheme a binary 0 is recorded as half a cycle of 1200 Hz, and a 1 is recorded as a full cycle of 2400 Hz.

Regardless of the data rate, the information in Kansas City Standard recordings is in the transitions of the recorded data. At a maximum data transfer rate, the derived clock rate is identically equal to the frequency of the logic 1 cycle. Therefore, the logic 1 cycle has a transition in the middle of a clock cycle. On the other hand, the logic 0 cycle has no such transition. A maximum data transfer rate is used in FM encoding. The FM encoding technique records on the disk only the transitions of the data square waves, as shown in figure 3-15. This means that the clock frequency can be increased to pack the data bits more closely on the disk track than can be done when the entire square wave is recorded, as with cassette recording.

This is not the final limit, however. There is a way of recovering the clocking information without wasting half the bits, thereby doubling the number of information bits on a disk. The method is called both <u>double-density</u> and <u>MFM</u> encoding. With this scheme, the encoder discards the clock bits so that only the data bits are present in the output bit stream.

TBD

Figure 3-14. Maximum Data Rate Recording, Kansas City Standard

TBD

Figure 3-15. Encoded Data for FM Recording

Clearly, both the data transfer rate and the amount of data on the diskette now can be doubled with respect to the (single-density) FM method. To recover the data, the detector section of the disk controller circuitry generates a pulse stream equal in frequency to the data rate. These narrow pulses create a bit window in which a logic 1 is detected as a flux transition in the middle of that window, and a logic 0 is detected as an absence of a transition. So the controller can be sure of the location of each 0 in a long string of 0s, the encoder section records (on the diskette) the clocking information by inserting a clock transition between two adjacent 0s, as shown in figure 3-16.

Hence, the MFM detector is more complex than the FM detector, because it must respond to the inserted clock bits, which appear coincident with the bit window pulses. The FM and MFM detectors usually are called data separators, because the detector works with a phase-locked loop to separate the composite clock and data signal into clock-only and data-only signals.

3.2.19.3 MFM Data Separation

Data separation in the case of MFM is somewhat different from that of FM. In FM data separation, the data and the clock components of the composite signal are truly separated: only data pulses go to the controller data input. On the other hand, in MFM data recovery, the data input to the controller comprises all the original bits from the disk, both data and clock.

The clock input to the floppy disk controller is not the clock pulses contained in the composite signal but is a synthesized version, generated by a local oscillator in a phase-locked loop. The clock pulses from that phase-locked loop create a window during which a data bit is expected. The data input from the diskette to the controller is gated from that window. Separation of the data bits from the clock bits takes place inside the floppy disk controller chip (paragraph 3.2.19.5), where the actual window gating occurs. (In FM detection the gating usually takes place in the data separator.) Figure 3-16. Encoded Data for Modified FM (MFM) Recording

TBD

Phase Detection

Data separation is enabled by the VCOE+ (VCO Enable) signal input to a 74LS51 combination gate (13X). (Refer to the CMS Logic Diagram, sheet 51.) The VCOE+ signal comes from the floppy disk controller chip and is asserted (high) when the chip is ready to transfer data to or from the diskette. The pin 6 output of the combination gate directs the data from the diskette (DSKDAT-A [DiSKette DATa]) to a 74LS221 one-shot (14Z). The one-shot delays the data pulse so that a phase detector can detect any clock pulse (generated by a local oscillator) occuring prior to the delayed data pulse, for synchronization purposes. (After the delay, the data pulse is regenerated by another 74LS221 one-shot after another short delay through the other section of the combination gate [pin 8]).

At the moment the one-shot is toggled by a data pulse, the Q output (pin 5) enables the phase detector logic of the phase-locked loop, by clocking a 74LS74 D flip-flip (14X, pin 3) to a cleared condition. Before or after the one-shot clears, a clock pulse from the local oscillator will trigger another 74LS74 D flip-flop (14X, pin 11)--this is guaranteed because this clock pulse represents twice the data transfer rate. When the one-shot clears, the Q- output clocks yet another 74LS74 D flip-flop (14V), which indicates the leading edge of the delayed data pulse.

The Q- outputs from the last two flip-flops mentioned are ANDed in a 74LS02 NOR gate (14W). Any time these outputs are coincident (both low), the NOR gate output sets the flip-flop (14X, pin 4) that enabled the phase detector logic. This flip-flop, in turn, clears the other two flip-flops (14V and 14X), effectively turning off the phase detector.

Thus the phase detector is enabled and disabled once for every pulse on the data line from the diskette. This allows synchronization of the clock to the data even though the data input to the phase-locked loop is not a square wave with a 50% duty cycle, but rather a stream of narrow pulses, with many pulses missing from their nominal location.

A simplified and generalized block diagram of the phase detector logic is shown in figure 3-17. To help the reader to understand the phase detector logic, the block diagram contains only generic logic blocks, and all signals are positive logic (active high), regardless of their true active voltage level. State changes occur only on rising edges.

Clearly, there was some delay between the time one flip-flop was triggered by the data pulse and the time the other flip-flop was triggered by the clock. The delay is indicated by a low output from the NOR gate (14W, pin 10), which allows the phase detector to continue working. The delay also is represented by positive-going pulses from one of the phase detector flip-flops and by neg-ative-going pulses from the other.

These PUMP UP (negative-going) and PUMP DOWN (positive-going) signals, when filtered, drive a voltage-controlled oscillator, or VCO. PUMP UP tends to increase the average frequency of the VCO, and PUMP DOWN does the opposite. This action indicates the outcome of the race between a pulse in the incoming data stream and a VCO clock pulse.

TBD

Figure 3-17. Simplified Block Diagram, Data Separator Phase Detector Logic

For example, if the VCO clock pulse (via a 74LS161 synchronous 4-bit counter [15T]) toggles the flip-flop (14X) connected to it before the pulse from the diskette toggles the other flip-flop, then PUMP DOWN will produce a pulse. The pulse informs the VCO that it is generating too high a frequency, and the pulse will bring down the voltage reference going to the MC4024 VCO chip. The pulse will be active for the time between the leading edge of the VCO clock pulse and the leading edge of the delayed data pulse, indicated by the Q- output of the one-shot (14Z, pin 12) going low.

The opposite happens when a delayed data pulse appears before the clock ticks. In this case, PUMP UP is a negative pulse, whose width is proportional to the error between the two pulses. The clock used for comparison is taken from the third bit of a synchronous 4-bit counter (15T) to provide a clock frequency of two times the actual bit transfer rate. This is so the VCO will synchronize with both the data bits and the inserted clock bits in the input data stream (the inserted clock bits occur at twice the data bit rate).

(To maintain a nominal VCO frequency when no data is being transferred to or from the diskette, the VCO is synchronized with a signal (2XWRCLK+ [2X Write CLocK]) that is twice the frequency of the clock used to send data to the diskette. When the VCOE+ signal goes low, the pin 6 output of the 74LS51 combination gate (13X) replaces the data with the 2XWRCLK+ signal, and synchronization occurs as before.)

Analog Error Detection

The pulse width of the PUMP UP and PUMP DOWN error signals is proportional to the required amount of frequency correction. Each of these pulse trains looks like a pulse-width-modulated replica of the input data stream. The difference in the average voltages of the pulse trains determines the output frequency of the VCO, which is an MC4024 (15V). Only one of these error signals is active at any given time; neither is active when synchronization is exact. However, when synchronization is exact, both flop-flops will be set when the data pulse and the clock pulse arrive at the CLOCK inputs to the flip-flops. This means that both flop-flops will be set for a short period of time, until the low output from a NOR gate (14W) turns off the phase detector logic and resets them.

During this time, the high pulse on the PUMP DOWN line is supplied through a diode (CR4) and series resistance to a capacitor (Cl25). The capacitor charges to a positive level. The charge creates an "automatic bias" for the base of one of the transistors (Q2) used to adjust the VCO control voltage. This nominal bias level sets the reference voltage for the VCO. The bias increases (becomes more positive) when a positive pulse comes in on the PUMP DOWN line; but,

when a negative pulse (actually a low positive pulse) arrives on the PUMP UP line, the bias charge will "leak" out through the other diode (CR3), to ground, and thereby decrease the bias to the error amplifier input transistor.

The error amplifier is a dc amplifier consisting of two 2N2222 transistors connected in a superalpha configuration, for proper impedance matching and good stability. An RC (R33/C124) negative feedback loop helps filter the high frequencies in the pulse transitions. Thus the error amplifier and phase detector logic circuits provide necessary corrections to the VCO frequency to ensure synchronous clocking of data bits from the diskette into the floppy disk controller chip. However, certain activity occurs during the writing of data onto the diskette that degrades the read data and that cannot adequately be compensated for by the data separator. The phenomenon is known as "bit-shifting."

3.2.19.4 Bit-Shifting

A problem peculiar to magnetic disk recording, especially MFM recording, is that the high bit densities cause the recovered data to appear shifted from their nominal position. Figure 3-18 shows the phenomenon as it appears to the floppy disk controller chip. The upper trace shows five data pulses recorded on the diskette at the <u>apparent</u> positions indicated. When the pulses are read back from the diskette, they are shifted in time from their apparent recorded position (i.e., some pulses appear later; o.thers appear earlier), as shown in the lower trace.

Several factors, which include nonlinearities in the pickup electronics and magnetic interactions, are responsible for bit-shifting. For example, the data pulses correspond with magnetic domains on the diskette. As shown in the upper trace of figure 3-18, the leftmost bit has a bit on its right but not on its left. Therefore, its magnetic domain is influenced by a like magnetic pole on the right, but not on the left. The magnetic flux of the leftmost bit thus is distorted and tends to move away from the nearby right-hand pole. Also, the situation may be aggravated by a real movement of the domain to the left.

TBD

Figure 3-18. Bit Shifting

Consequently, the read head, responding to the magnetic flux lines of the recorded data bit, sends the bit to the drive electronics as if it were repelled by the bit that will arrive after it (which is the bit to its right in figure 3-18). This means that the bit seems to arrive early.

The data separator circuits (discussed in paragraph 3.2.19.3) cannot adequately compensate for bit-shifting; this is because the phase-locked loop in the data separator is a feedback-control system that cannot follow sudden changes in input frequency, but rather settles over a period of time to its steady-state behavior .

Therefore, another means of bit-shift compensation is provided. The method used does not actually compensate for the bit shifting of recorded data; but rather it compensates for the <u>anticipated</u> bit shift, before data actually is recorded. The method is called "precompensation."

Precompensation

Fortunately, the data bit flux transitions appear early or late in a completely predictable manner. Their time of arrival (at the read electronics) depends on the location of other bit transitions in their immediate vicinity. Since the floppy disk controller chip holds a byte of data before that data goes to the diskette, the controller is in a position to analyze the locations of the data bits within that byte and, in turn, to determine which bits will suffer from bit-shifting.

For example, if a data bit is a 0 and has a 1 bit on each side of it, then the neighboring bits will be shifted toward the missing data pulse when they are recorded on the diskette. Hence, the first bit should be written early and the second bit should be written late, to compensate for the shifting. The appropriate commands for this are provided by the floppy disk controller chip and delivered to the precompensation logic.

Precompensation Control

The amount of precompensation is determined by a 74LS195 4-bit parallel-access shift register (13S). (Refer to the CMB Logic Diagram, sheet 49.) Each time a data pulse (WD4- [Write Data]) arrives from the floppy disk controller chip, the pulse is synchronized with FDCCLK+ (Floppy Disk Controller CLocK) and clock signal K4MHZ- (origin of both is in the clock generator section of the Central Microprocessor Board). This gives the broadside input logic, of the shift register enough time to set up before it latches the timing control commands from the floppy disk controller chip and begins shifting.

If the shift register receives an EARLY+ command from the controller chip, then that command becomes the data bit and is shifted out of the shift register 125 nanoseconds earlier than the nominal write time. This will compensate for the shift that occurs when that bit is written to the diskette. (The EARLY+ command is gated through a 74LSOO NAND gate [13R] to input C of the shift register.)

Likewise, if the shift register gets a LATE+ command from the controller chip, then that command becomes the data bit and is shifted out of the shift register 125 nanoseconds later than the nominal write time. (The LATE+ command is gated through the 74LSOO NAND gate [13R] to input A of the shift register.)

However, if both commands are inactive (low), then they are ANDed by the 74LS00 NAND gate (13R) and sent to input B of the shift register. In this case, that ANDed signal becomes the data bit and is shifted out at the nominal write time. The data bit output of the shift register is taken from the QD- pin and is sent to the drive electronics via a 7406 open-collector inverter (14J, pin 8).

Although the preceding discussions have assumed the reader is acquainted with the WD1793 floppy disk controller chip, such an acquaintance is not absolutely mandatory to understand the material up to this point. However, as we continue with functional descriptions of the remaining circuits in the floppy controller section, it becomes more important to understand the basic architecture of the chip. An overview of the chip is presented in the following paragraph.

3.2.19.5 Floppy Disk Drive Control

The floppy disk controller section of the Central Microprocessor Board is based on the WD1793 floppy disk controller chip (14R). (Refer to the CMB Logic Diagram, sheet 50.) The chip has the capability to read and write in single or double density. But it is used only in the double-density mode in our system.

The chip controls head motion by issuing step pulses and head-load commands to the drive. Step pulses move the read/write head arms from from track to track. The head-load command makes the head contact the diskette surface. (When the head is not loaded, it is physically lifted from the diskette surface.) The chip also combines the clock and the data bits to form a composite serial data stream, to be recorded on the diskette. And it also assembles the separated data and clock bits into 8-bit bytes for transmission the 68010.

Note that only a few external chips are required to interface the controller to the floppy diskette drive, since almost all aspects of diskette control are embedded in the controller chip. It operates on its own 2 MHz clock and has an on-chip processor designed for disk drive control. The chip occupies four memory addresses: the internal command/status, track, sector and data registers each have unique addresses, and can be read from and written to. (The register layout is shown in figure 3-19.)

The track register contains the track number of the arm position of the diskette drive that is presently selected. When a new drive is selected, the track register momentarily is incorrect. But when a system software command is given to the controller chip to read the diskette, the track identifier, as it passes under the head, is loaded into that register.

The sector register indicates which sector is to be read from or written to. When the controller executes a read or a write instruction, it first puts the head in contact with the diskette (it "loads the head"). Then it reads the sector IDs at the present arm position. TBD

Figure 3-19. Register Layout, WD1793 Floppy Disk Controller Chip

The controller checks each ID for a match against the contents of the track and sector registers. As the disk rotates, the correct sector arrives under the head. This is indicated by a match of the ID to the track and the sector registers. Now the controller is ready to read or write the data immediately following the sector ID. The data read from the diskette are accumulated bit by bit in the controller until a full byte is present. The byte is in the data register (in the chip) and will be passed to the 68010 over the byte-wide data bus.

Data to be written to the diskette flow from the 68010 to the controller chip over the same byte-wide data bus. These data are stored in the data register (in the chip) by parallel 8-bit write cycles. They then are output as a serial bit stream to the diskette drives.

The remaining two registers are the command register and the status register. These occupy a single address in the floppy controller I/O address space. Data read from this address are status reports to be returned to the 68010; data written to this address are commands interpreted by the controller chip. There are 11 commands available on the WD1793; they are listed in table 3-10. The Type I commands move the arm to the correct track. STEP IN and STEP OUT commands move the arm one track in or out. The STEP command moves the arm one track in the same direction as the last arm movement. The SEEK command allows the arm to be moved several tracks in a single step. This command accepts a target track number, contained in the data register, and then issues the correct number of step pulses to move the head arm from the present track to the target track.

The Type I commands generate the appropriate signals at the controller chip pins labeled STEP+ and DIRECTION*. In addition to these arm control signals, there are four output signals for writing data:

- o WD+ (Write Data)
- o WGATE+ (Write GATE)
- o TG43 (Track Greater than 43)
- o HLD (Head LoaD)

The WGATE+ signal asserts when WD+ contains the combined clock and data serial bit stream to be recorded. Signal TG43 forces the drive to reduce the recording current on tracks 44 and higher to reduce bit-shifting (discussed in paragraph 3.2.19.4). However, this function is not used in the Model 4108 Base Unit.

Table 3-10. Command List, WD1793 Floppy Disk Controller Chip

TYPE	COMMAND		
I	RESTORE		
I	SEEK		
I	STEP		
I	STEP IN		
I	STEP OUT		
II	READ SECTOR		
II	WRITE SECTOR		
III	READ ADDRESS		
III	READ TRACK		
III	WRITE TRACK		
IV	FORCE INTERRUPT		

Signal HLD commands the drive to load the read/write heads. In the Model 4108 Base Unit, however, the heads are automatically loaded whenever motor power is on; so the HLD signal is sent directly to the HLT input of the floppy disk controller chip.

Type II commands are used to read and write data. They function when a drive has been selected, the arm has been moved to the correct track, and the track and the sector registers have been loaded with track and sector numbers. The Type III and IV commands are used for several additional functions, such as diskette memory allocation, initialization, diagnostics and interrupts.

There also are five status signals:

- o WPRT- (Write PRoTect)
- o TROO- (TRack number 00)
- o IP- (Index Pulse)
- O READY
- o HLT (Head Load Timeout)

Signal WPRT- is asserted to abort any attempts to write to the diskette if the diskette is notched for such protection. Signal TROO- is asserted when the arm is located on the outermost track of the diskette. Signal IP- is asserted each time the index hole on the diskette passes under a photosensitive diode. The controller uses this signal to count diskette revolutions and abort incomplete operations if they do not finish inside of the allotted number of revolutions.

Signal READY usually is connected the drive power or to a switch on the door of the drive. The signal informs the controller chip that the diskette is in the proper position inside the drive, the door is closed, and power is applied to the drive. However, in the Model 4108 Base Unit, the READY signal is synthesized by a 74LS32 OR gate (12J).

The READY input to the controller is the OR of two MOTORON(X)+ signals from the gate. Note that the presence of the READY signal does not guarantee that the correct drive has the motor on, nor does it check to determine whether the selected drive is up to speed. Signal HLT informs the controller chip that the head has been properly loaded and to commence read or write operations.

For additional, more detailed, information on the Western Digital WD1793 floppy disk controller chip, the reader should refer to the manufacturer's literature. The next few paragraphs discuss how data is transferred to and from the flopp disk controller chip.

3.2.19.6 Buffered Data Transfer

To improve system throughput, all data involved in transfers between the floppy controller chip and the 68010 are buffered in the floppy sector buffer.

Since the transfer of data between the system memory and the floppy disk controller is under program control, this method allows the shortest data transfer time. The buffer memory is a 6116 2K X 8 static RAM chip (12S), which holds data for a complete sector. (Refer to the CMB Logic Diagram, sheet 46.) A jumper (D) can select an optional 8K X 8 RAM by bringing in an extra address line and by moving the Write Enable line to accommodate the larger RAM. Normal operation is with the jumper going from 2 to 3, for a 2K X 8 static RAM. Data transfer between the sector buffer and the floppy disk controller chip is controlled by DMA (direct memory access) logic. This is so that the transfer rate between the sector buffer and the floppy disk controller chip can keep up with the transfer rate of the serial data moving to and from the diskette.

The sector buffer RAM receives read/write strobes from a 74LS157 1-of-2 data selector (11R). Signal BUFCS- to the data selector controls the source of the read/write signals. The read/write inputs to the data selector may originate from the 68010, when the 68010 is filling or emptying the buffer, or from the DMA logic, when the buffer is under DMA control and the data flow is between the floppy disk controller chip and the buffer RAM.

Floppy Sector Buffer Addresses and Data

During data transfers between the floppy sector buffer and the floppy disk controller chip, a local address counter generates the range of addresses needed to access the entire sector of information. This 12-bit counter consists of four cascaded 74LS393 4-bit counters (UN and 12K). (Refer to the CMB Logic Diagram, sheet 45.)

Signal INC BUFADR+ (INCrement BUFfer ADdRess), which is asserted at the end of every completed DMA state machine cycle (described in later paragraphs), serves to increment the address counter throughout the entire range. The address then is latched into two 74LS374 transparent latches (12L and 12N), whose Q outputs are the sector buffer RAM address lines.

In addition to the addresses from the floppy buffer address counter, the sector buffer also receives addresses from the 68010, when data transfer is between it and the sector buffer. The lower 12 address lines from the 68010 and the eight data lines from the byte-wide data bus are buffered for the sector buffer RAM and the controller chip. The address lines are buffered by a pair of 74LS244 tristate drivers (11L and 11M), enabled by signal BUFCS+ (BUFfer Chip Select), from the DMA state machine. (Refer to the CMB Logic Diagram, sheet 42.) The byte-wide data bus is bidirectional and is buffered by a 74LS245 transceiver (13M), controlled by the RD- (Read) signal. The data bus is active only when the floppy sector buffer or the floppy disk controller chip is being addressed.

Once an address is set up on the sector buffer address lines, two decoders (a 74LS139 [12W] and a 74S138 [12X]) generate the appropriate read or write strobe with the correct timing for the static RAM. (Refer to the CMB Logic Diagram, sheet 44.) Signal FMEMWE- (Floppy MEMory Write Enable) is the write enable for the sector buffer RAM. The signal is asserted when LCIOWE- (LoCal I/O Write Enable) goes active for a period between the time that timing signal CST1F+ is asserted and timing signal CST2F+ is asserted (125-nanosecond write window).

Signal FMEMRE- (Floppy MEMory Read Enable) is the read enable for the sector buffer RAM. This signal is asserted from the 74LS139 (12W) when LCIORE- (LoCal I/O Read Enable) is active. Both FMEMWR- and FMEMRE- require MEM- (MEMory) to be asserted; MEM- is generated by the floppy controller address decoder (discussed in a later paragraph). Signals FMEMWR- and FMEMRE- are selected for use as the sector buffer read and write strobes by a 74LS157 l-of-2 data selector (11R). The corresponding output signals are MEMWE- (MEMory Write Enable) and MEMRD- (MEMory ReaD). (Refer to the CBM Logic Diagram, sheet 46.) These are enabled by BUFCS- (BUFfer Chip Select), from the state machine described next.

Floppy Sector Buffer Control

The transfer of data between the floppy sector buffer and the floppy disk controller chip is controlled by the floppy buffer state machine. (Refer to the CMB Logic Diagram, sheet 43.) The floppy buffer state machine functions as a DMA sequencer; it comprises a 74LS164 8-bit serial-to-parallel converter (11W); a 74LS175 quad D flip-flop (11T); and a 74LS157 l-of-2 data selector (US). At the beginning of the state machine operation, a single bit is loaded into the serial-to-parallel converter.

The bit then is shifted at the K2MHZ+ clock rate from one output of the converter to the next; and each output defines a single machine state. One output directly increments the sector buffer address counter, and some other outputs are first ORed and then latched in a D flip-flop, on the falling edge of the K2MHZ+ clock. Another output is both ORed and latched directly, also on the falling edge of the K2MHZ+ clock.

Finally, several of those flip-flop outputs are used directly for chip control while others are decoded further by the data selector. All the state machine's operations are controlled by data bits BDOO+ and BDO1+, from the byte-wide data bus. Bit DBOO+ comes out of a floppy drive interface D flip-flop (discussed in paragraph 3.2.19.7) as BUFW/R- (BUFfer Write/Read); likewise, DBO1+ is latched in that interface as CMD+ (CoMmanD). BUFW/R- controls the direction of the data transfer between the sector buffer and the floppy disk controller chip; CMD+ enables the state machine logic.

A third signal, DRQ+A (Data ReQuest), produced by the floppy controller chip, commands the state machine to begin operations. DRQ+A is asserted when the floppy disk controller chip is ready to transfer a byte of data to or from the buffer.

When the state machine is enabled by CMD+, each occurrence of DRQ+A transfers a data byte between the floppy sector buffer and the floppy disk controller chip. Thus the 74LS164 serial-to-parallel converter (11W) starts shifting when CMD+ and DRQ+A are both active. CMD+ informs the state machine that a disk read or a disk write cycle is requested, and DRQ+A indicates that no floppy controller chip interrupt is pending. If one or both of these signals is low, the state machine will remain in an idle loop. Note that the state machine is not resettable in the middle of a cycle, as the BUSY- signal must be released for the sequencing to begin. (A list of the machine states is presented in table 3-11.) Each state lasts 500 nanoseconds, and the states are as follows:

- <u>State 1</u> Latch buffer address (LTCHBUFADR+): latches the sector buffer addresses in two 74LS374 8-bit latches (12L and 12N). (Refer to the CMB Logic Diagram, sheet 45.) The local address bus is disabled from the main address bus. The BUSY- line is asserted to prevent the state machine from restarting while it is in the middle of a cycle.
- <u>State 2</u> Assert chip select, enable address: signal BUFCS- asserts to enable the 8-bit latches (12L and 12N), sending the address to the sector buffer RAM. BUFCS- also outputs signal FDCCS- from
 - 74LS157 l-of-2 data selector (11R), and enables the controller chip. (Refer to the CMB Logic Diagram, sheet 46.)
- State 3 Assert read and write enables: sector buffer RAM enable signals BUFMEMWE- and BUFMEMRE- go low at the outputs of another 74LS157 (US). (Refer to the CMB Logic Diagram, sheet 43.)
- State 4 Removes write enable: BUFMEMWE- releases.

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- State 5 Removes read enable: BUFMEMRE- releases.
- State 6 Removes local address enables: BUFCS- and BUFCS+ release.
- State 7 Increments the local address counter: INCBUFADR+ asserts.

Table 3-11. State Machine States

OUTPUT SIGNAL	STATE 1	STATE 2	STATE 3	STATE 4	STATE 5	STATE 6	STATE 7
	<u>R</u> <u>W</u>	<u>R</u> <u>W</u>	<u>R</u> <u>W</u>	<u>R W</u>	<u>R</u> <u>W</u>	<u>R</u> <u>W</u>	<u>R</u> <u>W</u>
BUSY-	1 1	1 1	1 1	1 1	1 1	0 0	0 0
INCBUFADR+	0 0	0 0	0 0	0 0	0 0	0 0	1 1
BUFCS+	0 0	1 1	1 1	1 1	1 1	0 0	0 0
BUFCS-	0 0	1 1	1 1	1 1	1 1	0 0	0 0
LTCHBUFADR+	1 1	0 0	0 0	0 0	0 0	0 0	0 0
BUFMEMRE-	0 0	0 0	1 0	1 0	0 0	0 0	0 0
BUFMEMWE-	0 0	0 0	0 1	0 0	0 0	0 0	0 0
BUFFDCRE-	0 0	0 0	0 1	0 0	0 0	0 0	0 0
BUFFDCWE-	0 0	0 0	1 0	1 0	0 0	0 0	0 0
R = Read cycl	e 1	= Assert	ed signal				

W = Write cycle 0 = Inactive signal

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Thus the floppy buffer state machine controls data flow between the floppy disk controller chip and the floppy sector buffer. When the state machine is not in control of the buffer, however, the operating system software may fill or empty it under program control, as mentioned earlier. Also, at that time, the system software may issue commands to, or receive status information from, the floppy disk controller section of the Central Microprocessor Board.

3.2.19.7 Floppy Disk Controller Section Control

All control of the floppy disk controller section of the Central Microprocessor Board is by the operating system software; the software controls the following:

- o The transfer of all control information from the 68010 to the floppy disk controller section. This includes (a) the reset for the floppy sector buffer local address counter; (b) the enable and the selection of read or write for the floppy buffer state machine; (c) the selection of a drive and of the side of the diskette within that drive; (d) the power to the selected drive motor; (e) the selection of FM or MFM at the floppy disk controller chip; (f) the selection of double density or standard density recording; and (g) all commands to the floppy disk controller chip command register.
 - o The transfer of all status information from the floppy disk controller section to the 68010. These include (a) interrupt and data requests from the controller chip; (b) the index hole pulse from the drive; (c) the busy signal from the floppy buffer state machine; and (d) reset and interrupt enable status.
 - o All data flow between the floppy sector buffer and the 68010.

Controller Section Programming

The floppy disk controller section options are programmed through the use of a 74LS273 octal D flip-flop (13J). (Refer to the CMB Logic Diagram, sheet 47.) The flip-flop is accessed at address 70XXXX (hex) and latches the control bit pattern from the byte-wide I/O data bus that determines the direction of data flow in the floppy sector buffer state machine. Floppy drive recording density and encoding format also are chosen here.

The recording density is selected when the HD/SD- (High Density/Standard Density) signal from the flip-flop (13J) selects the appropriate clock outputs from a 74LS157 l-of-2 data selector (11J, CMB Logic Diagram, sheet 48). The chosen clock output signals go to both the floppy disk controller chip and the data separator logic.

Floppy Drive Control

Another 74LS273 (13K) is the floppy control latch that holds control signals for the drive. (Refer to the CMB Logic Diagram, sheet 47.)

It latches the control bit pattern from the byte-wide I/O data bus that determines which drive is to be used (SELO-/SEL1- and MOTORONO-/MOTORON1-) and which side of the diskette in the chosen drive is to be used (SIDE-). The latch is mapped in with a write to FLOPLTCH-, at address 76XXXX (hex). The DOORLOCK(X)signals do not apply to the drives presently used in the Model 4108 Base Unit.

Status Transfer Control

To decide when to send the control signals, the system software must receive certain status information from the floppy disk controller section. Address 72XXXX (hex) activates the STATUS- signal. This signal, along with the LCIORE-(LoCal I/O Read Enable) signal, enables a 74LS373 transparent latch (13L, CMB Logic Diagram, sheet 47).

Unlike the two latches used for programming and drive control, this latch receives information from the floppy disk controller section and then drives that information on the byte-wide I/O data bus. Thus the latch provides the system software with a "snapshot" of the floppy disk controller section status. The various status signals are listed in a preceding paragraph.

Status Interrupt Control

When the system software needs to be informed of when a byte of data is being transferred to or from the diskette or when the floppy disk controller chip has completed an entire transfer of sector data, an appropriate signal is generated at the chip and may be used to interrupt the 68010. A 74LS51 combination gate (10W) collects the two kinds of interrupts (INTR+A [INTeRrupt] and DRQ+A [Data ReQuest]) from the floppy disk controller chip. (Refer to the CMB Logic Dia-Diagram, sheet 44.)

The two signals are enabled by ENBINTR+ (ENaBle INTERrupt) and ENBDRQ+ (ENaBle Data ReQuest). When one, or both, of these signals is enabled, and the corresponding interrupt is active, then a 74LS74 D flop-flop (14V) asserts signal INT3- (INTerrupt level 3). The flip-flop holds the interrupt until the 68010 returns an interrupt acknowledge signal (IACKL3- [Interrupt ACKnowledge Level 3]).

When the INT3- signal is asserted, it is encoded by a 74LS148 8-line-to-3-line priority encoder (3E). (Refer to the CMB Logic Diagram, sheet 22.) This constitutes an interrupt request to the 68010. Thus an interrupt request level 3 is encoded on the 68010 interrupt request lines (IPLO- through IPL2-). If the priority of the interrupt is greater than the current processor priority, then the interrupt processing sequence is started: The 68010 places the interrupt priority number on the lines carrying the three least significant address bits. These are decoded by a 74LS151 1-of-8 data selector (10K, CMB Logic Diagram, sheet 22).

For priority number 3, the CVPA- (CPU Valid Peripheral Address) output of the data selector is low (active). In response to CVPA-, the 68010 internally generates a vector number that is determined by the interrupt level number.

(The vector number [when multiplied by four] is the address in the lowest 1K bytes of main memory that contains the address of the routine that will handle the interrupt.) The content of the vector number is fetched and loaded into the 68010 program counter, and normal instruction execution commences in the interrupt service routine.

At the same time that the priority number on the address bus was being decoded to produce CVPA-, a 74LS138 1-of-8 decoder (10L, CMB Logic Diagram, sheet 20) also decoded those address bits. The output was the IACKL3- signal mentioned above. This is the interrupt acknowledge signal required to reset the flip-flop that generated 1NT3-.

3.3 MEMORY ARRAY BOARD FUNCTIONAL DESCRIPTION

This information will be available at a later date.

3.4 BASE UNIT POWER SUPPLY FUNCTIONAL DESCRIPTION

This information will be available at a later date.

SECTION IV

MAINTENANCE

4.1 INTRODUCTION

This section contains maintenance information for the Central Microprocessor Board (CMB), Base Unit Power Supply and peripheral controller boards contained in the Model 4108 Base Unit of the MAI® 2000 Series Desktop Computer System.

Included are procedures for preventive maintenance and trouble analysis, along with a diagrammed presentation of a system power-up check and a discussion of diagnostic programs. (Refer to Sections VII, VIII and IX in this manual for preventive maintenance and trouble analysis of the disk drive systems.)

It is recommended that the service representative become thoroughly familiar with the material contained in this manual before performing the following preventive maintenance and trouble analysis procedures.

4.2 SPECIAL TOOLS

Maintenance procedures contained in this manual require no special tools or special test equipment.

4.3 PREVENTIVE MAINTENANCE (INCOMPLETE)

Preventive maintenance consists of performing recommended inspection, cleaning and adjustments at regular intervals to prevent equipment failures. Because of the electronic structure of the equipment, preventive tasks consume little of the service representative's time and are well worth the effort in terms of the increase in equipment reliability. The preventive maintenance procedures are summarized in table 4-1.

Table 4-1. Preventive Maintenance Summary

EQUIPMENT	INTERVAL	ACTION	REFERENCE
Base Unit Power Supply	months	Check voltage tolerance, adjust as required	Table 4-2
Winchester Drives	months	Verify/adjust power supply voltages, inspect cables, clean and adjust	Sections VIII and IX in this manual
Floppy Disk Drive	months	Verify/adjust power supply voltages, inspect cables, clean and adjust	Section VII in this manual

Table 4-2. Base Unit Power S	Supply Voltage	Adjustments
------------------------------	----------------	-------------

MEASUREMENT	TEST POINT	VOLTAGE	ADJUSTMENT
1	TPx	+xx.x V to +xx.x V	Rxx
2	TPx	+xx.x V to +xx.x V	None
3	TPx	+xx.x V to +xx.x V	None
4	TPx	+xx.x V to +xx.x V	None

4.4 TROUBLE ANALYSIS

The steps that follow provide an organized, general approach toward troubleshooting the system. Proceed as follows:

- 1. Obtain an accurate description of the malfunction from the operator or other responsible person; then verify the problem.
- 2. Perform the System Power-Up Check (paragraph 4.5) as secondary verification of the suspected problem or as confirmation that basic system functions are in order.
- 3. If the problem is of an intermittent nature, run the appropriate diagnostic program in an effort to induce the problem on a controlled basis.
- 4. Perform a visual inspection and verify that all cabling is connected properly (including ground wires) and all connectors and PCBAs are seated properly.
- 5. Check the ac line as a possible cause of problems, i.e., sharp drops in voltage, transients and poor grounds are common problems. Check dc voltage levels on power supply test points (refer to table 4-2).
- Verify that all switches and jumpers on controller PCBAs are properly configured, i.e., device addresses, DMA numbers, etc. (refer to section V of this manual).
- 7. Disconnect the suspected peripheral from the system, and operate it off-line to isolate the problem or to confirm proper operation.
- 8. When replacing a PCBA appears to solve the problem, reinstall the suspected faulty PCBA to verify that the problem was not caused by bad contacts or poor seating.
- 9. After the suspected problem has been solved, run the applicable diagnostic programs before placing the entire system back in its normal operation.
- 10. Refer to the appropriate disk drive sections (VII, VIII, IX) in this manual for trouble analysis of suspected disk drive problems.

NOTE: The remaining maintenance information will be furnished at a later date.

SECTION V

REMOVAL/REPLACEMENT

5.1 INTRODUCTION

This section provides detailed procedures for replacing major subassemblies, and includes jumper/switch installation/settings and cable part numbers.

5.2 REPLACING THE CENTRAL MICROPROCESSOR BOARD (CMB)

To remove the Central Microprocessor Board, proceed as follows:

- 1. Shut down the system, and turn the Base Unit power OFF.
- Unplug all connections to the Base Unit, including all attached peripherals.
- 3. Insert a screwdriver, or similar device, into the slot at the bottom right-hand side of the Base Unit cover, and push in to disengage the the latch. Repeat with the left-hand side, and remove the cover.
- 4. Remove the Memory Array PCBAs, located in the front right-hand corner of the CMB, by simply lifting the "stack" of PCBAs away from the CMB, unplugging the bottom memory array PCBA from the CMB.
- 5. Unplug the ribbon cable(s) going from the Winchester Drive(s) to the Winchester Drive Controller (WDC) PCBA, located in the card cage at the rear right-hand corner of the CMB. (Note: two of the drive connectors on the WDC PCBA are situated side by side; the right-hand connector [J0] receives the "0" drive cable, and the left-hand connector [J1] receives the "1" drive cable.)
- 6. Remove the controller PCBA(s) by lifting the PCBA(s) away from the CMB, unplugging the (bottom) PCBA from the CMB. (When more than one PCBA is present, the entire stack may be removed as a unit.)
- 7. Remove the front and rear facias by pulling up slightly on each plastic card holder until the corresponding facia is disengaged from the card holder.
- 8. Remove the Winchester drive(s) as follows:
 - a. Using a screwdriver, or similar tool, push back the two (2) plastic latches at the bottom rear of the Winchester drive chassis, while lifting the back of the drive to clear the latches.
 - b. Unplug the 4-pin power plug, located at the bottom rear left-hand corner of the drive chassis, on the Master Electronics PCBA.

- c. Push the drive slightly toward the rear of the CMB so that the flange at the bottom front of the drive clears the slot in the Base Unit bottom panel, and lift the Winchester drive chassis from the CMB.
- 9. Remove the floppy drive(s) as follows:
 - a. Unplug the 4-pin power connector at the rear of the drive chassis.
 - b. Using a screwdriver, or similar tool, push back the two (2) plastic latches at the bottom rear of the floppy drive chassis, while lifting the back of the drive to clear the latches.
 - c. Push the drive slightly to the rear so that the flange at the bottom front of the drive clears the slot in the Base Unit panel.
 - d. Unplug the ribbon cable from the CMB, and lift the floppy drive chassis from the CMB. (Note: the two floppy drive connectors on the CMB are situated side by side. The right-hand connector receives the "0" cable; the left-hand connector receives the "1" cable.
- 10. Remove the Base Unit Power Supply by removing the two (2) Phillips head screws at the bottom right-hand side of the Power Supply and lifting the Supply from the CMB, unplugging the Supply from the CMB.

The Central Microprocessor Board now may be removed from the Base Unit bottom panel. To install the replacement CMB, proceed as follows (refer to figure 5-1 for jumper locations and to figure 5-2 for cable part numbers):

- 11. Connect jumper N between points 1 and 2. (This jumper allows the master oscillator to be disconnected from the dividers and buffers. An external oscillator can be injected at this point. Normal operation is with jumper N installed.)
- 12. Connect jumpers C and P. These jumpers configure the board to accept four different size EPROMs, used for system diagnostics and the debugger. The Central Microprocessor Board can handle 2732, 2764, 27128 and 27256 EPROMs. As received, the CMB has jumpers in etch to handle either 2732s or 2764s; no modification is necessary. To use the other size EPROMs, or to switch back to the 2732 or the 2764, after using a larger EPROM, follow the chart below.

EPROM	JUMPER C	JUMPER P
2732 (4K x 8)	1 and 2	1 and 2
2764 (8K x 8)	1 and 2	1 and 2
27128 (16K x 8)	2 and 3	1 and 2
27256 (32K x 8)	2 and 3	2 and 3

NOTE: An earlier version of the CMB (Rev. 1) could only handle 2716s and 2732s. On this CMB, jumper C must be connected as follows:

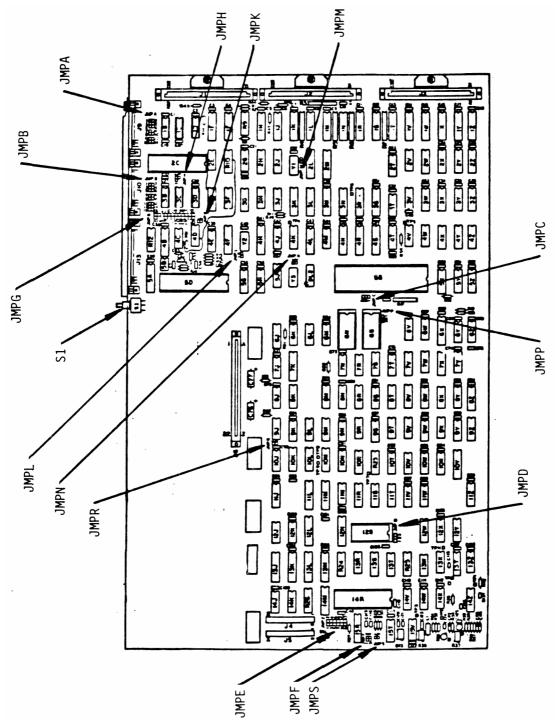


Figure 5-1. Location of Jumpers on Central Microprocessor Board

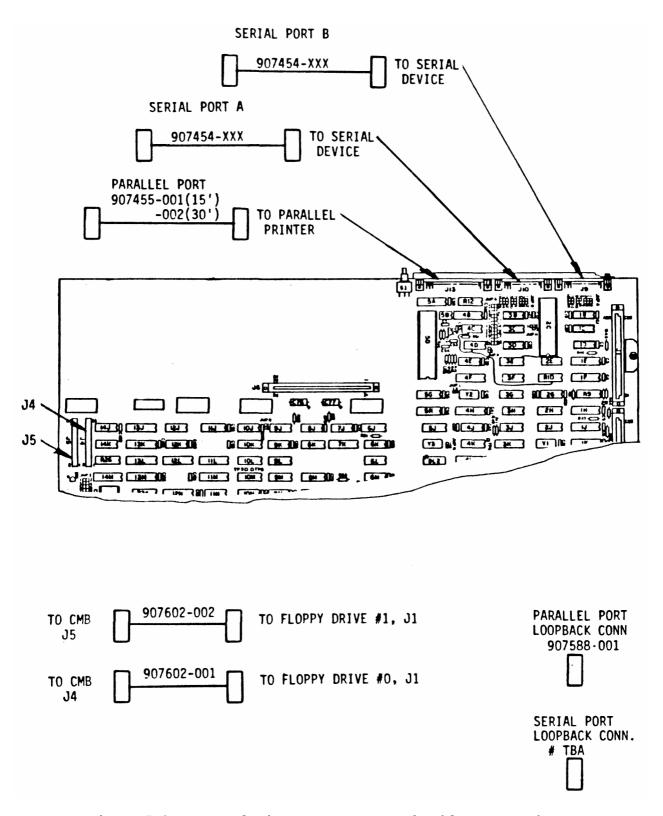


Figure 5-2. Central Microprocessor Board Cable Part Numbers

EPROM		JUMPER C
2716 (2K x 2732 (4K x	•	2 and 3 1 and 2

- 13. Connect jumper R. (This jumper, when disconnected, disables the memory refresh circuitry, thereby allowing easier debugging of memory and bus arbitration circuits. Normal operation is with jumper R connected between points 1 and 2.)
- 14. Connect jumpers A, B, G, H and K according to the following tables. (The serial port has two programmable ports. Each can be configured as RS-232 and support a modem, a printer or a terminal. Additionally, port B supports X-21. Note that only one cable is needed to support printers, terminals or modems. All signal switching is done on the Central Microprocessor Board via the jumpers. The RS-232 cable is a pin-for-pin connection. No signals or pins are cross-connected.)

10101 111	MODEM		TERMINAL		PRINTER	
Name	Jumper A	Cable	Jumper A	Cable	Jumper A	Cable
CTS DSRA DTR RTSA RXDA TXDA RNGA TRXCA DCDA	7 and 8 3 and 4 1 and 2 9 and 10 11 and 12 13 and 14 In Place In Place In Place	pin 6 pin 20 pin 4 pin 3 pin 2 pin 22 pin 15	7 and 9 *1 and 3 *2 and 4 8 and 10 11 and 13 12 and 14	pin 20 pin 6 pin 5 pin 2	7 and 9 1 and 3 2 and 4 8 and 10 11 and 13 12 and 14	pin 20 pin 6 pin 5 pin 2
PORT B:	MODEM		TERMII	NAL	PRINTE	R
Name	Jumper B	Cable	Jumper B	Cable	Jumper B	Cable
CTSB	7 and 8	pin 5	7 and 9	pin 4	7 and 9	pin 4

CTSB	7 and 8	pin 5	7 and 9	pin 4	7 and 9 pin 4
DSRB	3 and 4	pin 6	3 and 1	pin 20	3 and 1 pin 20
DTRB	1 and 2	pin 20	2 and 4	pin 6	2 and 4 pin 6
RTSB	9 and 10	pin 4	8 and 10	pin 5	8 and 10 pin 5
RXDB	13 and 14	pin 3	13 and 15	pin 2	13 and 15 pin 2
TXDB	15 and 16	pin 2	14 and 16	pin 3	14 and 16 pin 3
	Jumper G		Jumper G		Jumper G
RXDB	15 and 16	pin 3	15 and 16	pin 2	15 and 16 pin 2
DCDB	17 and 18	pin 8	17 and 18	pin 8	-
TRXCB	10 and 20	pin 15	19 and 20	pin 15	
	23 and 24		23 and 24		

	Jumper H	Jumper H	
DCDB	1 and 2	1 and 2	
	Jumper K	Jumper K	Jumper K
D422	*1 and 2	*1 and 2	*1 and 2

NOTE: Be sure to disconnect all unused jumper positions on port B.

PORT B - RS-422:

Jumper	Cor	nnect	-	AND	Jumper	Connect
G	1	and	2		В	11 and 12
G	3	and	4		В	15 and 16
G	5	and	6		Н	2 and 3
G	7	and	8			
G	9	and	10			
G	11	and	12			
G	13	and	14			
G	21	and	22			

NOTE: When RS-422 is used in port B, be sure that jumpers

G:15 and 16, G:19 and 20, and K: 1 and 2

are disconnected.

*This jumper disables the RS-422 drivers.

- 15. Connect jumpers L and M. (The serial ports are capable of communicating at a number of different speeds and can communicate both synchronously and asynchronously. Jumper L connects the master clock to the Baud rate generator, used for asynchronous input/output. Jumper M connects the synchronous clock to the port. These clocks are disconnectable for service purposes. Normal operation is with both jumpers [L and M] inserted, connecting pins 1 and 2 on each jumper block.)
- 16. Connect jumper D according to the following table. (The floppy disk drive support logic, on the Central Microprocessor Board, can support both 2K x 8 and 8K x 8 static buffers. This RAM is used as a sector buffer to speed up overall system performance when using the floppy drive. In addition, an optional 8K x 8 buffer may be used so that an entire track of information may be input/output to the 68010 microprocessor at one time without the processor having to read from the disk sector by sector.)

RAM SIZE JUMPER D 2K x 8 2 and 3 8K x 8 1 and 2

17. Connect Jumper E. (The floppy disk controller, located on the Central Microprocessor Board, has three different data separators available: the Analog, the Standard Microsystems Corp. [SMC], and the Western Digital [WD]. The installation of the jumper depends on which data separator is used.)

SEPARATOR:

Analog			SMC	WD	WD		
Data	1 and 2	Data	3 and	4	Data	5 and	6
Clock	7 and 8	Clock	9 and	10	Clock 1	.1 and	12

18. Connect jumper F according to the following table. (This jumper selects between Standard Density and High Density decoding on the Western Digital data separator. The system described in this manual uses Standard Density disk drives.)

MEDIA	JUMPER F

Standard Density	1	and	2
High Density	3	and	4

- 19. Verify that jumper S is <u>not</u> connected. (This jumper is only to be used when calibrating the Western Digital data separator. The jumper grounds the VFOE input to the WD1691, simulating a read condition. Normal operation is the jumper disconnected.)
- 20. For a standard Central Microprocessor Board configuration, recheck the jumper installation by referring to the jumper configuration table (5-1). The following assumptions are made:

2732 or 2764 EPROMs 2K x 8 sector buffer Standard RS-232 DCE on serial ports A and B Analog Data Separator Standard density disk drives

- 21. Reinstall the Central Microprocessor Board onto the Base Unit chassis.
- 22. Plug the Base Unit Power Supply into the Central Microprocessor Board, and replace the two (2) Phillips head screws at the bottom right-hand side of the Power Supply.
- 23. Reinstall the floppy disk drives(s) by completing the following steps.
 - a. Lower the floppy drive chassis into position on the CMB.

JUMPER	Table 5-1. CONNECT	CMB Jumper Configuration FUNCTION
A	7 and 9	Serial Port A - CTS
А	8 and 10	Serial Port A - RTS
A	11 and 13	Serial Port A - RXDA
A	12 and 14	Serial Port A - TXDA
В	1 and 3	Serial Port B - DSRB
В	2 and 4	Serial Port B - DTRB
В	7 and 9	Serial Port B - CTS
В	8 and 10	Serial Port B - RTSB
В	13 and 15	Serial Port B - RXDB
В	14 and 16	Serial Port B - TXDB
С	None	EPROM Size Select - 2732, 2764
D	2 and 3	Floppy Sector Buffer Size Select - 2K x 8
E	1 and 2	Floppy Data Separator Select - Data
E	7 and 8	Floppy Data Separator Select - Clock
F	1 and 2	Floppy Density Select
G	15 and 16	Serial Port B - RXDB
G	17 and 18	Serial Port B - DCDB
G	19 and 20	Serial Port B - TRXCB
G	23 and 24	Serial Port B - TRXCB
Н	1 and 2	Serial Port B - DCDB
K	1 and 2	Serial Port B - RS-422 Disconnect
L	1 and 2	Baud Rate Generator Connect
М	1 and 2	Serial Communications Synchronous Clock Connect
Ν	1 and 2	Master Oscillator Connect
P	None	EPROM Size Select - 2732, 2764
R	None	Refresh Enable
S	None	WD Data Separator Enable (Floppy Calibrate)

- b. Plug the ribbon cable into the CMB. (Note: the two connectors on the CMB are situated side by side. The right-hand connector receives the "0" cable; the left-hand connector receives the "1" cable.
- c. Pull the drive slightly to the front of the CMB so that the flange at the bottom of the drive chassis enters the slot in the Base Unit front panel.
- d. Lower the back of the drive chassis so that it pushes back the two(2) plastic latches on the CMB at the bottom rear of the drive.The drive chassis will "snap" in place.
- e. Connect the 4-pin power plug to the connector located at the top right-hand corner of the floppy drive chassis.
- 24. Reinstall the Winchester drive(s) by completing the following steps.
 - a. Lower the Winchester drive chassis into position on the CMB, and pull the drive slightly to the front of the CMB so that the flange at the bottom of the drive chassis enters the slot in the Base Unit front panel.
 - b. Connect the 4-pin power plug to the connector located at the bottom rear left-hand corner of the drive chassis, on the Master Electronics PCBA.
 - c. Lower the back of the drive chassis so that it pushes back the two(2) plastic latches on the CMB at the bottom rear of the drive.The drive chassis will "snap" in place.
- 25. Replace the front and rear facias by reversing the removal procedure in Step 7.
- 26. Reinstall the controller PCBA(s) into the card cage at the rear righthand corner of the CMB by plugging the PCBA into the CMB. (When more than one controller PCBA is present, the entire "stack" may be reinstalled as a unit.)
- 27. Plug the ribbon cables from the hard disk drive(s) into the Winchester Drive Controller (WDC) PCBA, at the top of the card cage. (Note: the two narrower ribbon connectors on the WDC PCBA are situated side by side; the right-hand connector [J0] receives the "0" drive cable, and the left-hand connector [J1] receives the "1" drive cable.)
- 28. Reinstall the Memory Array PCBAs into the card cage at the front right-hand corner of the CMB by plugging the bottom PCBA into the CMB. (The entire stack may be reinstalled as a unit.)
- 29. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to snap in place.

30. Plug In all connections to the Base Unit, including all previously attached peripherals.

5.3 REPLACING THE BASE UNIT POWER SUPPLY

To replace the Base Unit Power Supply, proceed as follows:

- 1. Shut down the system, and turn the Base Unit power OFF.
- 2. Insert a screwdriver, or similar device, into the slot at the bottom right-hand side of the Base Unit cover, and push in to disengage the the latch. Repeat with the left-hand side, and remove the cover.
- Disconnect the 4-pin power plug from the connector located at the bottom left-hand corner of the Winchester drive(s) chassis, on the Master Electronics PCBA.
- 4. Disconnect the 4-pin power plug from the connector located at the top right-hand corner of the floppy drive(s) chassis.
- 5. Unplug all connections to the Base Unit, including all attached peripherals.
- 6. Unplug the ribbon cable(s) going from the Winchester Drive(s) to the Winchester Drive Controller (WDC) PCBA, located in the card cage at the rear right-hand corner of the OMB. (Note: two of the drive connectors on the WDC PCBA are situated side by side; the right-hand connector [J0] receives the "0" drive cable, and the left-hand connector [J1] receives the "1" drive cable.)
- 7. Remove the controller PCBA(s) by lifting the PCBA(s) away from the CMB, unplugging the (bottom) PCBA from the CMB. (When more than one PCBA is present, the entire stack may be removed as a unit.)
- 8. Remove the rear facia by pulling up slightly on the plastic card holder until the facia is disengaged from the card holder.
- 9. Remove the Base Unit Power Supply by removing the two (2) Phillipshead screws at the bottom right-hand side of the Power Supply and lifting the Supply from the CMB, unplugging the Supply from the CMB.

To install the replacement Base Unit Power Supply, proceed as follows :

NOTE

The correct Base Unit Power Supply for the available power line voltage must be installed. See the parts listing for the part numbers.

- 10. Reinstall the Base Unit Power Supply by lowering the Supply into the Base Unit, onto the CMB, and plugging the Supply into the CMB.
- 11. Replace the two (2) Phillips-head screws at the bottom right-hand side of the Power Supply.
- 12. Replace the rear facia by reversing the removal procedure in Step 8.
- 13. Reinstall the controller PCBA(s) into the card cage at the rear righthand corner of the (MB by plugging the PCBA into the CMB. (When more than one controller PCBA is present, the entire "stack" may be reinstalled as a unit.)
- 14. Plug the ribbon cable(s) coming from the Winchester Drive(s) into the Winchester Drive Controller (WDC) PCBA, at the top of the card cage. (Note: the two narrower ribbon connectors on the WDC PCBA are situated side by side; the right-hand connector [J0] receives the "0" drive cable, and the left-hand connector [J1] receives the "1" drive cable.)
- 15. Connect the nearest 4-pin power plug to the connector located at the top rear right-hand corner of the floppy drives(s) chassis.
- 16. Connect the nearest 4-pin power plug to the connector located at the bottom rear left-hand corner of the Winchester Drive(s) chassis.
- 17. Turn the Base Unit power ON.
- 18. Connect the positive test probe of a digital multimeter (DMM) to the +5VDC test point on the Power Supply. This point is accessible from the top of the Power Supply cover , through the square hole near the front left-hand corner. (An edge of a printed circuit board can be seen through this hole, and the test points for the voltages produced by the supply are located near this edge; they are clearly marked.)
- 19. Adjust the +5-volt supply output for a DMM reading of 5.05040.010 volts dc. (This adjustment may be made by using a small, non-conductive screwdriver to turn the +5VDC adjust potentiometer. This potentiometer is accessible through the [round] hole at the top of the Power Supply cover, at the front left-hand corner.
- 20. Turn the Base Unit power OFF.
- 21. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to "snap" into place.
- 22. Plug in all connections to the Base Unit, including all previously attached peripherals.

5.4 REPLACING THE MEMORY ARRAY MODULES

To replace the Memory Array PCBAs, proceed as follows:

CAUTION

Do not remove these boards when power is applied to the Base Unit.

1. Shut down the system, and turn the Base Unit power OFF.

- 2. Insert a screwdriver, or similar device, into the slot at the bottom right-hand side of the Base Unit cover, and push in to disengage the the plastic latch. Repeat with the left-hand side, and remove the cover.
- 3. Remove the Memory Array PCBAs, located in the front right-hand corner of the CMS, by simply lifting the "stack" of PCBAs away from the CMB, unplugging the bottom memory array PCBA from the CMB.

To install the replacement Memory Array PCBA(s), proceed as follows:

4. Set the appropriate switches for the desired physical address of the Memory Array PCBA. See table 5-2 for a listing of switch settings, and refer to figure 5-3 for switch locations. Be careful not to duplicate addresses of existing Memory Array PCBAs; compare the switch settings of all the PCBAs.

ADDRESS (K Bytes)	S1	S2	S3	S4	S5	S6
0 to 256	ON	ON	DON'T CARE	ON	ON	ON
256 to 512	ON	ON	DON'T CARE	ON	ON	OFF
512 to 768	ON	ON	DON'T CARE	ON	OFF	ON
768 to 1024	ON	ON	DON'T CARE	ON	OFF	OFF
1024 to 1280	ON	ON	DON'T CARE	OFF	ON	ON

Table 5-2. Memory Array Module Address Switch Settings

Note: OFF = OPEN and ON = CLOSED

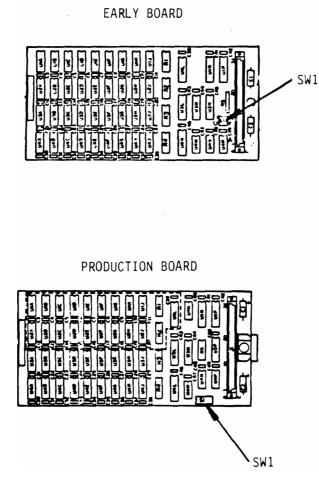


Figure 5-3. Location of Address Switches on Memory Array Module

- 5. Reinstall the Memory Array PCBAs into the card cage at the front right-hand corner of the CMB by plugging the bottom PCBA into the CMB. (Each board may be plugged into another, and the entire stack may be installed as a unit.)
- 6. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to "snap" into place.
- 7. Plug in all connections to the Base Unit, including all previously attached peripherals.

5.5 REPLACING THE 4-WAY CONTROLLER BOARDS

To replace the 4-Way Controller PCBA(s), proceed as follows:



Do not remove these boards when power is applied to the Base Unit.

- 1. Shut down the system, and turn the Base Unit power OFF.
- 2. Insert a screwdriver, or similar device, into the slot at the bottom right-hand side of the Base Unit cover, and push in to disengage the the plastic latch. Repeat with the left-hand side, and remove the cover.
- 3. Unplug the WDC Bus Adapter PCBA and the WDC PCBA (which carries the WDC PCBA) as a single unit from the top of the "stack." (This step may not be necessary; refer to step 4.)
- 4. Unplug from the stack any other controller PCBAs that might be present (after first disconnecting their cables) until the desired 4-Way Controller PCBA is accessible. Record the order of board removal. (When more than one device controller board is present, the entire stack may be removed as a unit, and the 4-Way Controller PCBA[s] then may be removed from the stack while it is outside of the Base Unit.)

The 4-Way Controller PCBA(s) now may be removed from the Central Microprocessor Board, or from the PCBA it is plugged into. To install the replacement 4-Way Controller PCBA(s), complete the following steps.

5. Set the appropriate switches on the 4-Way Controller PCBA for the controller board address/DMA arbitration number and for the kind of peripheral(s) served by the Base Unit according to the listings shown in table 5-3. See figure 5-4 for the location of the switches. Table 5-3. 4-Way Controller PCBA Switch Settings

SWITCH S1

	_	_ DMA Arbitration						PCBA	Address	_
	Sl	S2	S3	S4	S5	S6	S7	S8	S9	S10
Board 1	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON
Board 2	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
Board 3	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	ON
Board 4	ON	OFF	OFF	ON	ON	ON	OFF	OFF	ON	OFF

SWITCHES PGM1-4*

For PGM1 through PGM4, connect the pins according to the PCB detail used:

PCB detail 904741-001 (current production)

TERMINAL/PRINTER	MODEM
1 to 7	1 to 2
2 to 8	3 to 4
3 to 4	7 to 8
9 to 10	9 to 10
13 to 15	13 to 14
14 to 16	15 to 16

PCB detail 904943-001 (future production)

TERMINAL/PRINTER	MODEM
1 to 3	1 to 2
2 to 4	3 to 4
9 to 11	9 to 10
10 to 12	11 to 12
13 to 15	13 to 14
14 to 16	15 to 16

*PGM1 through 4 are actually jumpers (as opposed to switches) enclosed in plastic rectangular "boxes." Each box may be pulled from its. position and then reinstalled to connect any two adjacent pins. There is one PGM "group" per controller port, six boxes per PGM group, and 16 pins per PGM group.

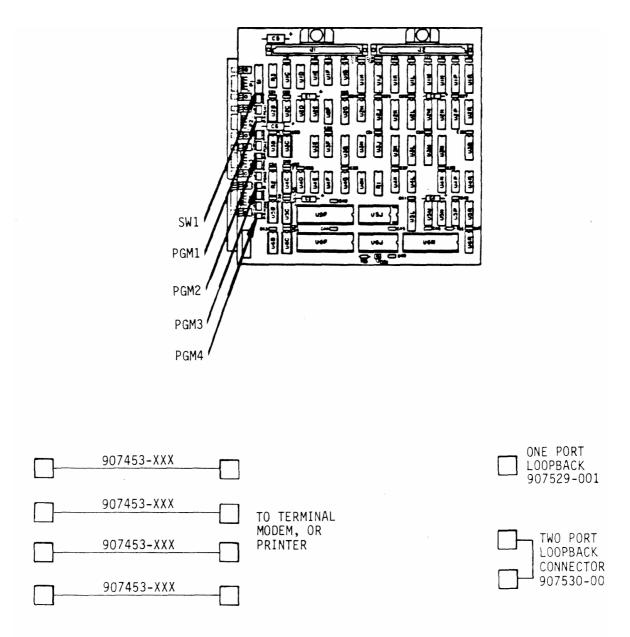


Figure 5-4. Location of Switches on 4-Way Controller PCBA

- Plug the 4-Way Controller PCBA into the CMB (or into the PCBA from which the original was removed) at the rear right-hand corner of the CMB. Replace any other boards that were removed in step 4, in the order recorded in that step.
- 7. Plug the WDC Bus Adapter PCBA and the WDC PCBA (mounted above the component side of the WDC Bus Adapter) into the PCBA at the top of the stack.
- 8. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to "snap" into place.
- 9. Plug in all connections to the Base Unit, including all previously attached peripherals that may have been removed during this procedure.
- 5.6 REPLACING THE WINCHESTER DRIVE CONTROLLER (WDC) BOARD

To replace the WDC PCBA, proceed as follows (2-PCBA configuration only):

CAUTION

Do not remove this board when power is applied to the Base Unit.

- 1. Shut down the system, and turn the Base Unit power OFF.
- 2. Insert a screwdriver, or similar device, into the slot at the bottom right-hand side of the Base Unit cover, and push in to disengage the the plastic latch. Repeat with the left-hand side, and remove the cover.
- 3. Unplug the ribbon cable(s) going from the Winchester Drive(s) to the Winchester Drive Controller (WDC) PCBA, located in the card cage at the rear right-hand corner of the Central Microprocessor Board (CMB). (Note: two of the drive connectors on the WDC PCBA are situated side by side; the right-hand connector [J0] receives the "0" drive cable, and the left-hand connector [J1] receives the "1" drive cable.)
- 4. Unplug the 4-pin power connector from J3 on the WDC PCBA.
- 5. Unplug the ribbon cable (connecting the WDC PCBA to the WDC Bus Adapter) from J4 on the WDC PCBA.
- 6. Remove the WDC PCBA from the WDC Bus Adapter PCBA by releasing the retainers on the (4) plastic standoffs at each corner of the WDC PCBA and lifting the WDC PCBA upward.

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To Install the replacement Winchester Drive Controller PCBA, proceed as follows:

7. Verify that the jumpers listed below are not installed, for normal operation. See figure 5-5 for the location of the jumpers.

Jumper	А	to	В	
Jumper	С	to	D	
Jumper	Е	to	F	
Jumper	G	to	Η	
Jumper	0	to	Ρ	

- 8. Lower the WDC PCBA onto the WDC Bus Adapter PCBA so that the Winchester Drive connectors (JO, Jl, J2, J3) are facing the front of the Base Unit and the four standoffs enter the holes in the WDC PCBA. Push down on each corner of the WDC PCBA until the retainers on the standoffs hold it in place on the WDC Bus Adapter PCBA.
- 9. Plug the ribbon cable coming from the WDC Bus Adapter into connector J4 at the rear of the WDC PCBA.
- 10. Plug the 4-pin power connector coming from the WDC Bus Adapter PCBA into connector J3 at the front right-hand corner of the WDC PCBA.
- 11. Plug the ribbon cable(s) coming from the Winchester drive(s) into the WDC PCBA. (Note: the two narrower ribbon connectors on the WDC PCBA are situated side by side; the right-hand connector [J0] receives the "0" drive cable, and the left-hand connector [J1] receives the "1" drive cable.)
- 12. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to "snap" into place.
- 13. Plug in all connections to the Base Unit, including all previously attached peripherals.
- 5.7 REPLACING THE MAGNETIC CARTRIDGE STREAMER CONTROLLER (MCSC) BOARD

To replace the Magnetic Cartridge Streamer Controller PCBA, proceed as follows:

CAUTION

Do not remove this board when power is applied to the Base Unit.

1. Shut down the system, and turn the Base Unit power OFF.

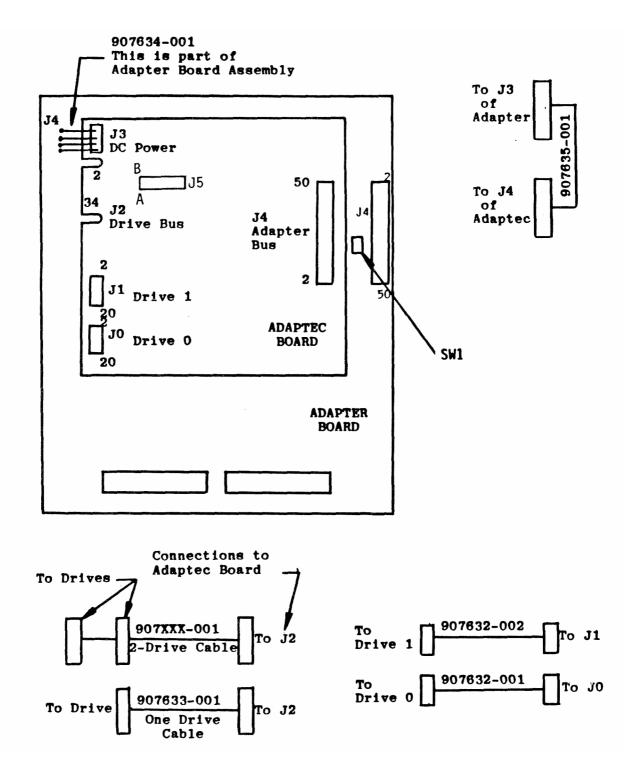


Figure 5-5. Location of Jumpers on the Winchester Drive Controller PCBA

- 2. Insert a screwdriver, or similar device, into the slot at the bottom right-hand side of the Base Unit cover, and push in to disengage the the plastic latch. Repeat with the left-hand side, and remove the cover.
- 3. Unplug the WDC Bus Adapter PCBA and the WDC PCBA (which carries the WDC PCBA) as a single unit from the top of the "stack." (This step may not be necessary; refer to step 4.)
- 4. Unplug from the stack any other controller PCBAs that might be present (after first disconnecting their cables) until the Magnetic Cartridge Streamer Controller (MCSC) PCBA is accessible. Record the order of board removal. (When more than one device controller board is present, the entire stack may be removed as a single unit, and the MCSC PCBA then may be removed from the stack While it is outside of the Base Unit.)

To install the replacement MCSC PCBA, complete the following steps.

5. Set the appropriate switches on the MCSC PCBA for the correct bus arbitration number and mode according to the listing shown below. See figure 5-6 for the location of the switches.

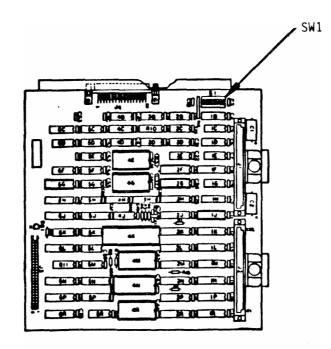
SWITCH SW1

		Bus Arbi	tration				
<u>s1</u>	<u>S2</u>	<u></u>	<u></u>	<u>S5</u>	<u></u>	<u>S7</u>	<u>S8</u>
ON	ON	ON	ON	OFF	OFF	ON	ON

- 6. Plug the Magnetic Cartridge Streamer Controller PCBA into the CMB (or into the PCBA from which the original MCSC PCBA was removed) at the rear right-hand corner of the CMB. Replace any other PCBAs that were removed in steps 3 and 4 of this procedure, in the order recorded in those steps .
- 7. Plug the WDC Bus Adapter PCBA and the WDC PCBA (mounted above the component side of the WDC Bus Adapter) into the PCBA at the top of the stack.
- 8. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to "snap" into place.
- 9. Plug in all connections to the Base Unit, including all previously attached peripherals.

5.8 REPLACING THE WINCHESTER DRIVE CONTROLLER (WDC) BUS ADAPTER BOARD

To replace the Winchester Drive Controller Bus Adapter PCBA, proceed as follows:



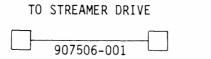


Figure 5-6. Location of Switch on Magnetic Cartridge Streamer Controller PCBA

CAUTION

Do not remove this board when power is applied to the Base Unit.

- 1. Shut down the system, and turn the Base Unit power OFF.
- 2. Insert a screwdriver, or similar device, into the slot at the bottom right-hand side of the Base Unit cover, and push in to disengage the the plastic latch. Repeat with the left-hand side, and remove the cover.
- 3. Unplug the WDC Bus Adapter PCBA and the WDC PCBA (which carries the WDC PCBA), as a single unit, from the CMB or from the top of the "stack," if other device controller boards are present.
- 4. Unplug the 4-pin power connector from J3 on the WDC PCBA.
- 5. Unplug the ribbon cable (connecting the WDC PCBA to the WDC Bus Adapter) from J4 on the WDC PCBA.
- 6. Remove the WDC PCBA from the WDC Bus Adapter PCBA by releasing the retainers on the (4) plastic standoffs at each corner of the WDC PCBA and lifting the WDC PCBA upward.

To install the replacement Winchester Drive Controller $% \left({{\mathbb{T}}_{{\mathbb{T}}}} \right)$ Bus Adapter PCBA, proceed as follows :

 Set the appropriate switches on the WDC Bus Adapter PCBA for the correct bus arbitration number according to the listing shown below. See figure 5-5 for the location of the switches.

SWITCH SW1

	В	us Arbitra	tion				
<u>S1</u>	<u>S2</u>	<u>S3</u>	<u>S4</u>	<u>S5</u>	<u>S6</u>	<u>S7</u>	<u>58</u>
OFF	OFF	OFF	ON	ON	ON	DON'T CA	RE

- 8. Lower the WDC PCBA onto the WDC Bus Adapter PCBA so that the Winchester drive connectors (JO,J1,J2,J3) are facing the front of the Base Unit and the four standoffs enter the holes in the WDC PCBA. Push down on each corner of the WDC PCBA until the retainers on the standoffs hold it in place on the WDC Bus Adapter PCBA.
- 9. Plug the ribbon cable coming the WDC Bus Adapter into connector J4 at the rear of the WDC PCBA.

- 10. Plug the 4-pin power connector coming from the WDC Bus Adapter into J3 on the WDC PCBA.
- 11. Plug the WDC Bus Adapter PCBA into the CMB (or into the PCBA from which it was removed) at the rear right-hand corner of the CMB.
- 12. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to "snap" into place.
- 13. Plug in all connections to the Base Unit, including all previously attached peripherals.
- 5.9 REPLACING THE LOCAL AREA NETWORK (LAN) BOARD

To replace the Local Area Network PCBA, proceed as follows:

CAUTION

Do not remove this board when power is applied to the Base Unit.

- 1. Shut down the system, and turn the Base Unit power OFF.
- 2. Insert a screwdriver, or similar device, into the slot at the bottom right-hand side of the Base Unit cover , and push in to disengage the the plastic latch. Repeat with the left-hand side, and remove the cover.
- 3. Unplug the WDC Bus Adapter PCBA and the WDC PCBA (which carries the WDC PCBA) as a single unit from the top of the "stack." (This step may not be necessary; refer to step 4.)
- 4. Unplug from the stack any other controller PCBAs that might be present (after first disconnecting their cables) until the Local Area Network Controller (LANC) PCBA is accessible. Record the order of board removal. (When more than one device controller board is present, the entire stack may be removed as a single unit, and the LANC PCBA then may be removed from the stack while the stack is outside the Base Unit.)

To install the replacement LANC PCBA, proceed as follows:

5. Set the LANC board station address. The address uniquely identifies this station to all other stations on the network. To set it, first locate and identify the address switch on the LANC board. It will be found next to the cable connector (J3), as shown in figure 5-7.

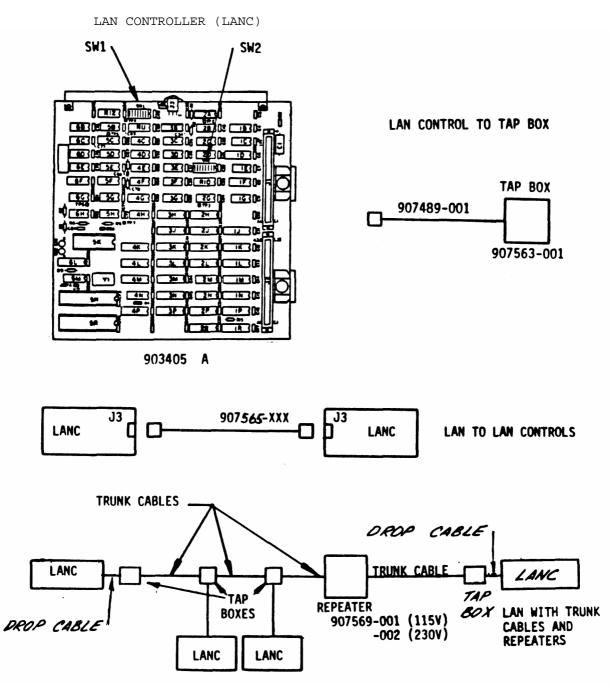


Figure 5-7. Location of Switches on Local Area Network Controller PCBA

The address switch comprises eight smaller switches, and each switch is set individually. <u>The "off" position of each switch represents</u> binary 1.

Bias	Terminator						
S1	S2	S3	S4	S5	S6	S7	S8
*	* *	↑	↑	Ŷ	¢	Ŷ	Ť

SWITCH SW1

- * represents the "bias." Switch 1 is set to 1 (off) on only one IAN controller board in a network; all other LAN controllers must have this switch set to 0 (on). A maximum of two LAN controller boards per Base Unit is allowable, but one per Base Unit is the normal configuration.
- ** represents the terminator setting. Only two controllers, one at each end of the network, may have this switch on; all other controllers must have the switch off.
- ↑ represents the binary coded station address bit positions. Switch S8 is the least significant bit, and switch S3 is the most significant bit. Each LAN controller board has one unique address: the first address is 000001, and the 63rd address is 111111 (i.e., all switches turned off). (Note: 000000 is illegal.)

Switch S1 is the Bias switch and normally is set to the on position; however, for each part of a network cable that connects two repeaters, one station must have this switch turned off to bias the line. Switch S2 is on only at the ends of a network; all other controllers must have this switch off.

Switches S3 through S8 are set for the desired address; these may be treated as a 6-bit binary word, with switch no. 8 as the least significant bit. There are 64 possible combinations of settings. With on = 0 and off = 1, the switches may be set for any one of 63 addresses (address 00 must not be used).

For example:

```
100101 = address 37
```

111111 (all switches off) = address 63.

Another set of switches also must be set for the bus arbitration number and board address. These are set at the factory but should be verified by the installer before continuing. See figure 5-7 for the switch location.

SWITCH SW2

Bus Arbitration						Address	Decode
<u>S1</u>	<u>S2</u>	<u>S3</u>	<u>S4</u>	<u>S5</u>	<u>S6</u>	<u>S7</u>	<u>S8</u>
OFF	OFF	OFF	ON	ON	OFF	ON	OFF
OFF	OFF	OFF	ON	ON	ON	OFF	ON

Note: The top line is for for a single board; a second board normally is used only with diagnostics.

The Local Area Network Controller board is now ready to be installed.

- 6. Plug the Local Area Network Controller PCBA into the CMB (or into the PCBA from which the original LANC PCBA was removed) at the rear righthand corner of the CMB. Replace any other PCBAs that were removed in steps 3 and 4 of this procedure, in the order recorded in those steps.
- 7. Plug the WDC Bus Adapter PCBA and the WDC PCBA (mounted above the component side of the WDC Bus Adapter), if they are present, into the board at the top of the stack.
- 8. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to "snap" into place.
- 9. Plug in all connections to the Base Unit, including all previously attached peripherals.

5.10 REPLACING THE WINCHESTER DRIVE

To replace the Winchester Drive(s), proceed as follows:

- 1. Shut down the system, and turn the Base Unit power OFF.
- 2. Insert a screwdriver, or similar device, into the slot at the bottom right-hand side of the Base Unit cover, and push in to disengage the the plastic latch. Repeat with the left-hand side, and remove the cover.
- 3. Remove the Memory Array PCBAs, located in the front right-hand corner of the CMB, by simply lifting the "stack" of PCBAs away from the CMB, unplugging the bottom memory array PCBA from the CMB.
- 4. Remove the front facia by pulling up slightly on the plastic card holder until the facia is disengaged from the card holder.
- 5. Unplug the ribbon cable(s) going from the Winchester Drive(s) to the Winchester Drive Controller (WDC) PCBA, located in the card cage at the rear right-hand corner of the CMB.

(Note: two of the drive connectors on the WDC PCBA are situated side by side; the right-hand connector [JO] receives the "0" drive cable, and the left-hand connector [J1] receives the "1" drive cable.)

- 6. Using a screwdriver, or similar tool, push back the two (2) plastic latches at the bottom rear of the Winchester Drive chassis, while lifting the back of the Drive to clear the latches.
- 7. Unplug the 4-pin power plug, located at the bottom rear left-hand corner of the Drive chassis, on the Master Electronis PCBA.
- 8. Push the Drive slightly toward the rear of the CMB so that the flange at the bottom front of the Drive clears the slot in the bottom panel of the Base Unit.
- 9. Lift the Winchester Drive chassis from the CMB.

To install the replacement Winchester Drive, complete the following steps.

- 10. Refer to Section VIII (20 MB drive) or Section IX (50 MB drive) in this manual for jumper information and other data, if necessary.
- 11. Lower the Winchester Drive chassis into position on the CMB.
- 12. Pull the Drive slightly to the front of the CMB so that the flange at the bottom of the Drive chassis enters the slot in the Base Unit front panel.
- 13. Connect the 4-pin power plug to the connector located at the bottom left-hand corner of the Drive chassis, on the Master Electronics PCBA.
- 14. Lower the back of the Drive chassis so that it pushes back the two (2) plastic latches on the CMB at the bottom rear of the Drive. The Drive chassis will "snap" in place.
- 15. Plug the ribbon cables from the Winchester Drive(s) into the WDC PCBA. (Note: the two narrower ribbon connectors on the WDC PCBA are situated side by side; the right-hand connector [J0] receives the "0" drive cable, and the left-hand connector [J1] receives the "1" drive cable.)
- 16. Replace the front facia by reversing the removal procedure in Step 4.
- 17. Reinstall the Memory Array PCBAs into the card cage at the front right-hand corner of the CMB by plugging the bottom PCBA into the CMB. (The entire stack may be reinstalled as a unit.)
- 18. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to snap into place.
- 19. Plug in all connections to the Base Unit, including all previously attached peripherals.

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5.11 REPLACING THE FLOPPY DISK DRIVE

To replace the floppy disk drive(s), proceed as follows:

- 1. Shut down the system, and turn the Base Unit power OFF.
- 2. Insert a screwdriver, or similar device, into the slot at the bottom right-hand side of the Base Unit cover, and push in to disengage the the latch. Repeat with the left-hand side, and remove the cover.
- 3. Remove the Memory Array PCBAs, located in the front right-hand corner of the CMB, by simply lifting the "stack" of PCBAs away from the CMB, unplugging the bottom memory array PCBA from the CMB.
- 4. Remove the front facia by pulling up slightly on the plastic card holder until the facia is disengaged from the card holder.
- 5. Unplug the 4-pin power connector at the rear of the drive chassis.
- 6. Using a screwdriver, or similar tool, push back the two (2) plastic latches at the bottom rear of the floppy drive chassis, while lifting the back of the drive to clear the latches.
- 7. Push the drive slightly toward the rear of the CMB so that the flange at the bottom front of the drive is out of the slot in the bottom panel of the Base Unit.
- 8. Unplug the ribbon cables from the CMB. (Note: the two floppy drive connectors on the CMB are situated side by side; the right-hand connector receives the "0" drive cable, and the left-hand connector receives the "1" drive cable.)
- 9. Lift the floppy disk drive chassis from the CMB.

To install the replacement floppy disk drive(s), complete the following steps.

- 10. Refer to Section VII in this manual for jumper information and other data, if necessary.
- 11. Lower the floppy disk drive chassis into position on the CMB.
- 12. Plug the ribbon cable into the CMB. (Note: the two connectors on the CMB are situated side by side. The right-hand connector receives the "0" drive cable, and the left-hand connector receives the "1" cable.)
- 13. Pull the drive slightly to the front of the CMB so that the flange at the bottom of the drive chassis enters the slot in the Base Unit front panel.
- 14. Lower the back of the drive chassis so that it pushes back the two (2) plastic latches on the CMB at the bottom rear of the drive. The drive chassis will "snap" in place.

- 15. Connect the 4-wire power cable to the connector located at the top right-hand corner of the floppy drive chassis.
- 16. Replace the front facia by reversing the removal procedure.
- 17. Reinstall the Memory Array PCBAs into the card cage at the front right-hand corner of the CMB by plugging the bottom PCBA into the CMB. (The entire stack may be reinstalled as a unit.)
- 18. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to snap into place.
- 19. Plug in all connections to the Base Unit, including all previously attached peripherals.

SECTION VI

ILLUSTRATED PARTS LIST

6.1 INTRODUCTION

This section provides parts list information for the assemblies/subassemblies recommended for replacement at the field level.

NOTE

Refer to Engineering Change Notices and appropriate documents for changes to the parts list and for drawings not included. All changes should be kept with this manual.

6.2 INDEX OF ASSEMBLIES

The following is an index of the assemblies/subassemblies covered in this section:

FIGURE/ TABLE	TITLE	PAGE
6-1	Central Microprocessor Board PCBA	6-2/3
6-2	Memory Array PCBA	6-8/9
6-3	WDC Bus Adapter PCBA	6-10/11
6-4	4-Way Controller PCBA	6-14/15
6-5	MTCS Controller PCBA	6-18/19
6-6	LAN Controller PCBA	6-22/23
6-7	Winchester Drive (Single-Board) Controller PCBA	6-26/27
6-8	Power Supply Input Module PCBA	6-28/29
6-9	Power Supply Output Module PCBA	6-32/33
6-10	Power Supply Control Module PCBA	6-35/36

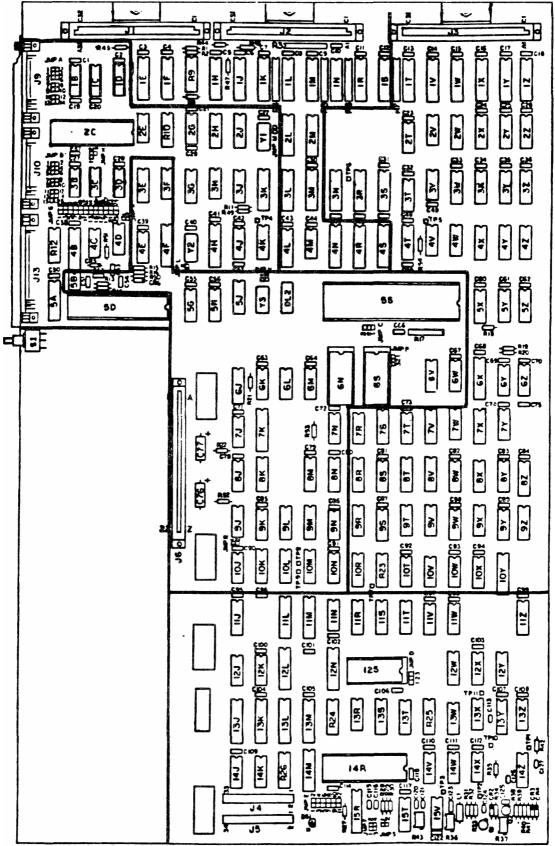


Figure 6-1. CMB PCBA

Table 6-1. CMB PCBA (MM531011) Parts List

DESCRIPTION

REFERENCE DESIGNATION

903441-001	PCBA, CMB (MM531011)
903442-001	PCB, CMB
	Diagram, Schematic

Capacitors

104001-002	Capac, Ceram Z5U 1000 pFD 5V 20%	C125
104001-016	Capac, Ceram Z5U 0.47 MFD 50V 20%	C52
104003-006	Capac, Ceram X7R 0.01 MFD 100V 10%	C124
104003-007	Capac, Ceram X7R 0.1 MFD 100V 10%	C115
104004-010	Capac, Ceram COG 39 pFD 5V 5%	C120,127
104004-013	Capac, Ceram COG 82 pFD 5V 5%	C113,121,126
104010-001	Capac, Ceram Z5U Axial 0.1 MFD 50V +80/-20%	C1-51,53-57,59-64,
		66-75, 78-112, 114,
		117,118,122,123
102000-012	Capac, Tant 33MFD 10V 20%	C76,77

Connectors

300091-002	Conn, D Fml Rt Ang PC MT Metal Face 25-Pos	J9,10
300091-003	Conn, D Fml Rt Ang PC MT Metal Face 37-Pos	J13
300093-001	Conn, DIN Male 3x32 0.025Sq 64 Pos A&C	Jl,2,3
300032-002	Conn Hdr, 0.025Sq Dbl Row 100 6-Pos	JMPA.JMPB (2 REQD)
300032-003	Conn Hdr, 0.025Sq Dbl Row 100 4-Pos	JMPA (2 REQD) JMPB,
		JMPF
300032-008	Conn Hdr, 0.025Sq Dbl Row 100 12-Pos	JMP E
300032-010	Conn Hdr, 0.025Sq Dbl Row 100 24-Pos	JMP G
300032-016	Conn Hdr, 0.025Sq Dbl Row 100 34-Pos	J4,5
325026-001	Conn Hdr, Sgl Row 1-Pos 100 Tail	TP1-11,JMPH
325026-002	Conn Hdr, Sgl Row 2-Pos 100 Tail	JMPH,K,L,M.N,R,S
325026-003	Conn Hdr, Sgl Row 3-Pos 100 Tail	JMPC, D, P, MOUNT ON S1
300017-006	Conn PCB, Dbl Readout 22/44	J6

Diodes

130006-001	Diode, Switching 1N914B	CR2,3,4,5,6
152001-001	LED, Green Diff Lens	DS1

Inductors

135006-004	Inductor,	22.0uH	Ll
		Integrated Circuits	
101051	•	Ntwk 220/330 Ohm	4A(R12)

TOTODT	IC, REBIB NEWR 220/330 Onm	TA(KIZ)
101315	IC, 74S00 Quad 2-Input Pos NAND	6L,8X,9Y
101316	IC, 7406 Quad Buffer/Driver	14J,14K

Table 6-1. CMB PCBA Parts list (continued)

PART NUMBER

DESCRIPTION

REFERENCE DESIGNATION

Integrated Circuits

101612		MC1489L Quad Line Receiver	1C,3C,ID,3D
101613		MC1488L Quad Line Driver	1B,3B
101615	IC,	74S08 Quad 2-Input Pos AND	7T,8Y
101624	IC,	74S20 Dual 4-Input NAND	10N
101626	IC,	SN74S37 Quad 2-Input Pos NAND Buffer	бV
101627		SN74S38 Quad 2-Input Pos NAND Buffer	2G,8J,9K,7N
101629		SN74S74 Dual D-Type F/F	6К
101630		74S112 Dual J-K Edge Trig F/F	5G,5H,5J
101631		74S138 Decoder/DeMUX	8M,8N,12X
101632	-	SN74S151 Data Select/MUX	8K
101633	-	SN74S157 Quad 2-1 Linedata Select/MUX	
101637		SN74S260 Dual 5-Input Pos NOR	11V
101642	-	74LS163 Binary Counter Sync	3G
101655		74S02 Pos NOR Totem-Pole	9N
101656		74LS04 Hex Inverter	
			7R,9R,4V,10V,13W
101657		74LS157 Quad 2-1 Line Data Select/MUX	
101671		74S280 9-Bit Odd/Even Parity Gen	2V, 3V
101672	-	74LS20 Pos NAND	9W
101709		74LS00 Quad 2-Input NAND	4E,13R,9T,4W
101710		74LS02 Quad 2-Input NOR	10T,14W
101711		74LS08 Quad 2-Input AND	9S,7W,13Z
101712		74LS10 Triple Input NAND	85
101714		74LS32 Quad 2-Input OR	12J.9V.4M
101715	IC,	74S51 Dual 2-Wide 2-Input AND/OR Inv	6M.7Y
101718	IC,	74LS109 Dual J-K Pos-Edge Trig F/F	10R,7S,8V
101719	IC,	74LS138 3-8 Line Decoder/DeMUX 4	K,10L,8R,12Y,9Z,11Z
101720	IC,	74LS151 8-1 Line Data Select/MUX	3J,10K,7V
101722	IC,	74LS175 Quad D-Type Edge Trig F/F	11T
101724		74LS195A 4-BitPar Access S/R	13S
101736		NE555 Timer	5B
101737		74S30 8-Input NAND	10X
101740		74LS51 Dual 2-Wide 2-Input AND/OR Inv	
101741		74LS74 Dual D-Type Pos Edge Trig F/F	10J,14V,14X
101783		74LS112 Dual J-K Edge Trig F/F	8T,8Z
101786		74LS21 Dual 4-Input AND	9X
155002-005		Digital Delay Line Term - 100ns	5L(DL2)
161001		74S139 Dual 2-4 Line Decoder	4T
161003		74S161 4-Bit Binary Counter	6J,15T
161009	IC,	74S240 Octal Buffer 3-State TTL	1F,4H,1J,IN,1R,1S,
1 < 1 0 1 0	та		1T,1X,6X,10Y,4F,1Y
161013		74LS373 Octal D-Type Latch 3-State	13L
161015		74LS14 Hex Schmitt Trig Inv	2E
161017		26LS31 Quad Diff Line Driver	4D
161018		26LS32 Quad Diff Line Receiver	4C
161020		74LS161A 4-Bit Binary Counter	9J
161022		74S85 4-Bit Magnitude Comp	5X,5Y,5Z
161023	-	74LS273 Octal D-Type F/F	13J,13K
161024		74S283 4-Bit Binary Full Adder	2X,2Y,2Z
161028	IC,	74LS393 Dual 4-Bit Binary Counter	3H,12K,11N,2T

Table 6-1. CMB PCBA Parts List (continued)

PART NUMBER

DESCRIPTION

REFERENCE DESIGNATION

Integrated Circuits

161039-001	IC, 74LS164 8-Bit Par Output Ser S/R	11W
161053-001	IC, 74LS38 Quad 2-Input Pos NAND Buffer	3F
161055-001	IC, 74LS221 Dual Monostable MVB	14Z
161061-001	IC, 74S299 8-Bit Univ. S/R	7K
161064-001	IC, 74LS240 Octal Buffer/Line Driver,3-State	1K,1L,1M
161065-001	IC, 74LS374 Octal Register D-Type F/F	12L, 3N, 12N, 3R, 3S
161066-001	IC, 74LS245 Octal Bus Receiver	2L,3L,13M
161068-001	IC, 74LS244 Octal Buffer/Line Driver	5A,11L,2M,3M,11M,
101000 001		14M,4N,4R,4S,4B
161069-001	IC, 74LS259 Latch 8-Bit ADD	10M
161074-001	IC, 74S244 Octal Buffer	1E,1H,1Z,IV,1W
161077-001	IC, 74S373 Transparent Latch	3К
161086-001	IC, 74LS139 Decoder/DeMUX	12W
161108-001	IC, RAM Static 2Kx8 CMOS 200ns	12S
161128-001	IC, 74LS260 Dual 5-Input NOR	7J
161129-001	IC, 74S22 Dual 4-Input NAND OC	6Y,6Z
161133-001	IC, 74LS148 8-3 Priority Encoder	3E
161141-001	IC, 74LS153 Dual 4-1 Select/MUX	2H,2J,9L,2W
161152-001	IC, 74LS629 VCO	13Y
161155-001	IC, 74S40 Dual 4-Input NAND TP	б₩
162031-001	IC, Serial Communications Controller	2C
162032-001	IC, Floppy Disk Controller	14R
162041-001	IC, 2210D 64x4 Nonvolatile Static RAM	4L
162042-001	IC, 68010 16-Bit Vrtl Mem MPU 8.0MHz	5S
162052-001	IC, 1691 Floppy Support Logic	15R
163001-001	IC, 4024 MVB Dual Controller	15V
165042-001	IC, 68230L8 Parallel Intfce/Timer	5D
165047-015	IC, PROM 2764-CMB Kernel Firmware 0	6S
165047-016	IC, PROM 2764-CMB Kernel Firmware 1	бN
	Oscillators	
150001-001	Osc, Xtal Clock 16 MHz	Y3(5K)
150001-012	Osc, Xtal Clock 4.915 MHz	Y2(4G)
150001-021	Osc, Xtal Clock 3.6864 MHz	Y1(2K)
	Potentiometers	
118008-003	Poten, Multi-Turn 20K Ohm 0.5W 10%	R36
118008-004	Poten, Multi-Turn 50K Ohm 0.5W 10%	R37,43
	Resistors	
111000-019	Resis, Comp 47 Ohm 5%	R32
	Regis Comp 8 2K Ohm 5%	D20 10

111000-023	Resis,	Comp	8.2K Ohm 5%	R39,40
111000-029	Resis,	Comp	330 Ohm 5%	R19,20,45,48

Table 6-1. CMB PCBA Parts List (continued)

PART NUMBER DESCRIPTION DESIGNATION

Resistors

111000-031	Resis, Comp 1K Ohm 5%	Rll,15,16,18,21,22,
111000-033	Resis, Comp 39K Ohm 5%	R30
111000-052	Resis, Comp 470 Ohm 5%	R46,47
111000-043	Resis, Comp 100 Ohm 5%	R38
111000-044	Resis, Comp 120 Ohm 5%	Rl,2,8,44
111000-048	Resis, Comp 220 Ohm 5%	R50
111000-052	Resis, Comp 220 Ohm 5%	R46,47
111000-065	Resis, Comp 470 Ohm 5%	R52,53,54,57,58
111000-065	Resis, Comp 47K Ohm 5%	R34
111000-069	Resis, Comp 20K Ohm 5%	R29
111000-077	Resis, Comp 1M Ohm 5%	R13,14
111000-077	Resis, Comp 12K Ohm 5%	R35
111000-091	Resis, Comp 13K Ohm 5%	R33,41
111000-109	Resis, Comp 13K Ohm 5%	R55,56
116000-117	Resis, Metal Film 15K Ohm 0.125W 1%	R42
119000-001	Resis Ntwk, DIP 470 Ohm 16-Pin 15 Resis	R9(1G)
		R9(1G) R10(2F),R23(10S) 13N(R24) R26(14L) R17

Sockets

325005-003	Socket,	IC DIP	4-Leaf	Cont	Gold	14-Pos	(1C,3C,ID,3D,IB,3B)
325005-007	Socket,	IC DIP	4-Leaf	Cont	Gold	28-Pos	(6N,6S,12S)
325005-010	Socket,	IC DIP	4-Leaf	Cont	Gold	40-Pos	(2C,14R)
325005-013	Socket,	IC DIP	4-Leaf	Cont	Gold	64-Pos	(5S)
325038-001	Socket,	LSI DI	P Low Pi	rofile	e 48-I	Pos	(5D)

Transistors

101306 Trans	2N2222A NPN Silicon	Q1,Q2
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Miscellaneous

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Figure 6-2. Memory Array 256K PCBA

Table 6-2. Memory Array 256K PCBA (MM531030) Parts List

PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION
903368-001 904693-001	PCBA, Memory Array 256K (MM531030) PCB, Memory Array Diagram, Schematic	
	Capacitors	
104007-001 108016-003	Capac, Ceram Z5U DIP 0.1 MFD 50V 20% Capac, Alum Elect 47 MFD 10V -20+50%	C3-C49 Cl,2
	Connectors	
300092-001	Conn, D Fml 3x32 Press-Fit,64-Pos A&C	Jl
	Integrated Circuits	
101315 101627 101673 161009 161066-001 161074-001 161129-001 162023-001	IC, 74S00 Quad 2-Input Pos NAND IC, SN74S38 Quad 2-Input Pos NAND Buffer IC, 74S86 Quad 2-Input Exclusive NOR IC, 74S240 Octal Buffer 3-State TTL IC, 74LS245 Octal Bus Receiver IC, 74S244 Octal Buffer IC, 74S22 Dual 4-Input NAND CC IC, 4164,64K Dynamic RAM,150ns <u>Resistors</u>	U4M U4N U4P U1L,U3L,U4L U1P,U3P U1N,U3M L1M U1A-U1J,U2A-U2J, U3A-U3J,U4A-U4J
119000-003 313145-001	Re sis Ntwk, DIP 1K Ohm 16-Pin 15 Resis Resis Ntwk, DIP 33 Ohm	R5 Rl(l) ,R2(2K), R3(3K),R4(4K)
221000 000	Switches	01
331008-006	Switch, Rocker DIP 6-Pos Miscellaneous	S1
907420-001	Catch, I/C PCBA	
907420-001 907388-001 214027-001 310019-001 762022-002 907389-001	Ejector, Euro-DIN Conn Stack Fastener, Push-On 0.312 Dia Stud Housing/Guide, Conn DIN 3x32 Label, Tab 0.250x1.700 Yel Latch, Euro-DIN Conn Stack	(Jl)

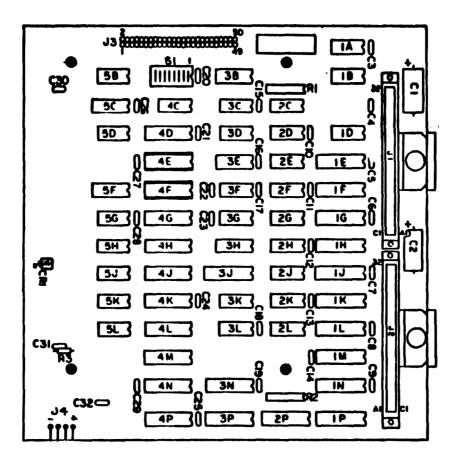


Figure 6-3. WDC Bus Adapter PCBA

Table 6-3. WDC Bus Adapter PCBA (MM531100) Parts List

PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION
903439-001 904854-001	PCBA, WDC Bus Adapter (MM531100) PCB, WDC Bus Adapter Diagram, Schematic	
	Capacitors	
104007-001 108016-004	Capac, Ceram Z5U DIP 0.1 MFD 50V 20% Capac, Alum Elect 100 MFD 6V -20/+75%	C3-32 C1,2
	Connectors	
300092-001 300032-012	Conn, D Fml 3X32 Press-Fit 64-Pos Conn Hdr, 0.025Sq Dbl Row 50-Pos	Jl,2 J3
	Diodes	
152001-001	LED, Green Diff Lens	CR1
	Integrated Circuits	
101051 101315 101514 101615 101623 101625 101627 101628 101630 101631 101633 101637 101655 101656 101709 101710 101710 101710 101741 161009 161015 161023 161064-001 161065-001 161074-001 161076-001	<pre>IC, Pesis Ntwk 220/330 Ohms IC, 74SOO Quad 2-Input Pos NAND IC, 7438 Buffer Quad 2-Input NAND IC, 74S08 Quad 2-Input Pos AND IC, 74S11 3-Input AND IC, 74S32 Quad 2-Input Pos NOR IC, SN74S38 Quad 2-Input Pos NAND Buffer IC, 74S64 4-2-3-2 Dual D-Type F/F IC, 74S112 Dual J-K Edge Trig F/F IC, 74S138 Decoder/DEMUX IC, SN74S157 Quad 2-1 Linedata Select/MUX IC, SN74S157 Quad 2-1 Linedata Select/MUX IC, SN74S260 Dual 5-Input Pos NOR IC, 74LS02 Pos NOR Totem-Pole IC, 74LS04 Hex Inv IC, 74LS00 Quad 2-Input NAND IC, 74LS02 Quad 2-Input NAND IC, 74LS08 Quad 2-Input NOR IC, 74LS18 3-8 Line Decoder/DEMUX IC, 74LS18 3-8 Line Decoder/DEMUX IC, 74LS14 Dual D-Type Pos Edge Trig F/F IC, 74LS14 Hex Schmitt Trig Inv IC, 74LS240 Octal Buffer 3-State TTL IC, 74LS240 Octal Buffer/Line Driver 3-State IC, 74LS244 Octal Buffer/Line Driver IC, 74LS244 Octal Buffer</pre>	SC SL SB 2L 3G 2K 1A, 2F 2C, 2H, 3D, 5D 3E, 5F 2J 3B 2E 2D, 3C 5G 5H, 5J 3K 3L, 5K 3H 4C 1D 1F, 1G 4C 4J 1E, 3J 3N, 3P, 4G, 4H, 4K, 4M, 4N 4L, 4P 1H 2G 1K 1L, 4D
161111-001 161145-001	IC, 74LS640 Octal Bus Receiver IC, 74LS697 Sync U/D Binary Counter	1K,1L,4D 1J,1M,1N,1P,2P

Т	able 6-3. WDC Bus Adapter PCBA Parts List	(continued)
PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION
	Integrated Circuits	
911006-008 911009-004		4E 4F
	Resistors	
111000-029 119001-002	······································	R3 R1,2
	Sockets	
325005-011	Socket, IC DIP 4-Leaf Cont Gold 20-Pos	(4F,4E)
	Switches	
331005-002	Switch, SPST DIP 8-Pos	SW1 (4B)
	Miscellaneous	
907634-001 907420-001 907388-001 214027-001 310019-001 762022-003 907389-001	Cable, Assy DC Pwr-WDC/Bus Adapter-WDC Catch, I/O PCBA Ejector, Euro-DIN Conn Stack Fastener, Push-On 0.312 Dia Stud Housing/Guide, Com DIN 3X32 Label, Tab 0.375 X 1.250 Yel Latch, Euro-DIN Conn Stack	(Jl,2) (Jl,2) (Jl,2) (Jl,2) (Jl,2)
216021-001	Standoff, Ins 0.50L Snap-In	(01,2)

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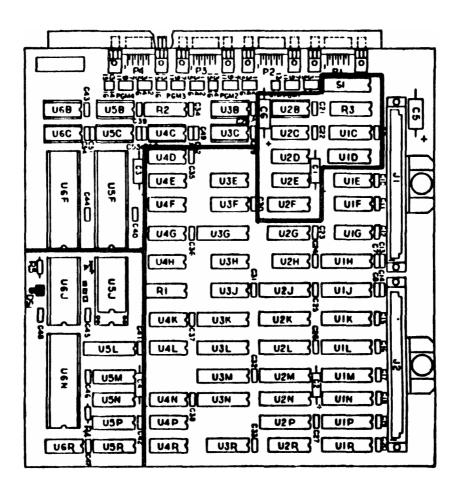


Figure 6-4. 4-Way Controller PCBA

DS1

Table 6-4. 4-Way Controller PCBA (JM531040) Parts List

PART NUMBER DESCRIPTION DESIGNATION

903390-001 PCBA, 4-Way Controller (MM531040) 904741-001 PCB, 4-Way Controller Diagram, Schematic

Capacitors

104007-001	Capac, Ceram 250 DIP 0.	1 MFD 50V 20%	Cl-4
104008-004	Capac, Ceram X/R DIP 22	20 pFD 50V 5%	C9-54
101127	Capac, Tant Sleeved 47	MFD 20V 10%	С5,6
102000-012	Capac, Tant 33 MFD 10V	20%	C(l-4)

Connectors

300091-001	Conn, D Fml Rt/Ang PC Mtg Metal 9-Pos	Pl-4
300092-001	Conn, DIN Fml 3X32 Press-Fit 64-Pos	J1.2
300032-002	Conn Hdr, 0.025Sq Dbl Row 6-Pos	PGM1-4
300032-003	Conn Hdr, 0.025Sq Dbl Row 4-Pos	PGM1-4

Diodes

152003-001 LED

Integrated Circuits

101315	IC, 74S00 Quad 2-Input Pos NAND	4D
101541	IC, 74S04 Hex Inverter	2H,4G,4K
101612	IC, MC1489L Quad Line Receiver	2B,3B,3C,5B,6B
101613	IC, MC1488L Quad Line Driver	4C,5C,6C
101615	IC, 74S08 Quad 2-Input Pos AND	4F,4N,4P
101625	IC, 74S32 Quad 2-Input Pos-OR	4L
101627	IC, SN74S38 Quad 2-Input Pos NAND Buffer	1F, 1G
101628	IC, 74S64 4-2-3-2-Input AND/OR Inv	1E
101629	IC, SN74S74 Dual D-Type F/F	2D,2E
101630	IC, 74S112 Dual J-K Edge Trig F/F	2F,2G
101633	IC, SN74S157 Quad 2-1 LineData Select/MUX	1C
101637	IC, SN74S260 Dual 5-Input Pos NOR	3R
101655	IC, 74S02 Pos NOR Totem-Pole	2C,3E
101713	IC, 74LS30 8-Input NAND	3J
101719	IC, 74LS138 3-8 Line Decoder/DeMUX	2R,3R,5N,5P
101740	IC, 74LS51 Dual 2-Wide 2-Input AND/OR Inv	3F
101741	IC, 74LS74 Dual D-Type Pos Edge Trig F/F	4H,4R,6R
101742	IC, 74LS85 4-Bit Magnitude Comparator	1C
101776	IC, 74LS11 Triple 3-Input Pos AND	4E
161009	IC, 74S240 Octal Buffer 3-State TTL	1H,1J,2J
161013	IC, 74LS373 Octal C-Type Latch 3-State	2K, 3N
161023	IC, 74LS273 Octal C-Type F/F	2M,2N,2P,3G
161049-001	IC, 74279 Quad Shift Reg Latch	5r
161064-001	IC, 74LS240 Octal Buffer Line Driver, 3-State	1L,1M,1N,1P,1R
161065-001	IC, 74LS374 Octal Register D-Type F/F	2L,3K,3L,3M
161066-001	IC, 74LS245 Octal Bus Receiver	5L

PART

Table 6-4. 4-Way Controller PCBA Parts List (continued)

		REFERENCE
NUMBER	DESCRIPTION	DESIGNATION

Integrated Circuits

161086-001	IC,	74LS139 Decoder/DeMUX	5M
161108-001	IC,	RAM Static 2Kx8 CMOS 200ns	5J
162002-002	IC,	Z80A 8-Bit Micro-P	бN
162031-001	IC,	Serial Communications Controller	5F,6F
161111-001	IC,	74LS640 Octal Bus Receiver	lK

Resistors

111000-043	Resis, Comp 100 Ohm 5%	R4,5
119000-003	Resis Ntwk, DIP IK Ohm 16-Pin 15 Resis	R1(4J)
119000-006	Resis Ntwk, DIP 3.9K Ohm 16-Pin 15 Resis	
R2(4B),R3(1B)		

Sockets

325005-003	Socket,	IC DIP	4-Leaf	Cont	Gold	14-Pos	
(2B,3B,3C,4C,5B,5C,							
325005-007	Socket,	IC DIP	4-Leaf	Cont	Gold	28-Pos	(5J , 6J)
325005-010	Socket,	IC DIP	4-Leaf	Cont	Gold	40-Pos	(5F,6F,6N)

Switches

331008-010	Switch,	Rocker I	DIP	10-Pos	S1(1A)	
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Miscellaneous

907388-001	Ejector, Euro-DIN Conn Stack	
214027-001	Fastener, Push-On 0.312 Dia Stud	
310019-001	Housing/Guide, Conn DIN 3X32	(J1,2)
00000-000	Interim Component-Pending Spec	бJ
325033-001	Jumper, 0.025Sq Gold PI	(PGM1-4)
762022-003	Label, Fab	
907389-001	Latch, Euro-DIN Conn Stack	
907420-001	Latch, I/O PCBA	
907402-001	Plate, Conn 4-Way Controller	
208000-001	Rivet, Blind 0.116DxO.188L Alum	(Pl-4)
100114	Screwlock, Fml 4-40 Thd D-Type	(Pl-4)

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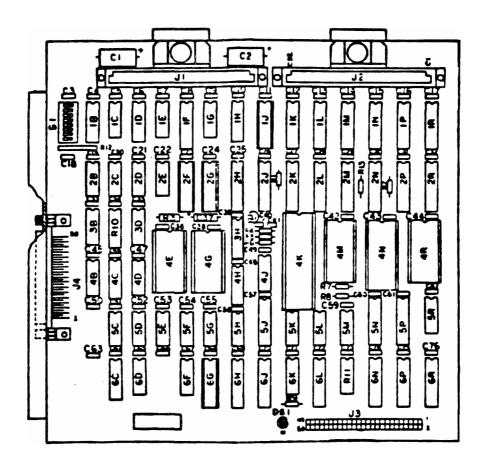


Figure 6-5. MTCS Controller PCBA

Table 6-5. MTCS Controller PCBA (MM531070) Parts List

PART NUMBER DESCRIPTION DESIGNATION

903406-001 PCBA, MTCS Controller(MM531070) 904769-001 PCB, MTCS Controller Diagram, Schematic

Capacitors

108016-004	Capac, Alum Elect 100 MFD 6V,-20/+75%	Cl,2
101144	Capac, Ceram 0.1 MFD 50V 20%	C40
104004-018	Capac, Ceram COG 33 pFD 50V 5%	C41
104007-001	Capac, Ceram Z5U DIP 0.1 MFD 50V 20%	C3-36,38,39,42-57,
		C59-76
102000-007	Capac, Tant 2.2 MFD 35V 10%	C37

-

Connectors

300091-004	Conn,	D Fml Rt/Ang PC Mtg 50-Pos	J4
300092-001	Conn,	DIN Fml 3x32 Press-Fit 64-Pos	J1,2
300032-012	Conn	Hdr, 0.025Sq Dbl Row 50-Pos	J3

Diodes

152001-001	LED, (Green	Diff	Lens	DS1
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Integrated Circuits

101315	IC 74000 and 2 Input Dec NAND	4B
101514	IC, 74S00 Quad 2-Input Pos NAND	
	IC, 7438 Buffer Quad 2-Input NAND	1E,4J
101623	IC, 74S11 3-Input AND	6D
101625	IC, 74S32 Quad 2-Input Pos OR	6K
101627	IC, 74LS38 Quad 2-Input Pos NAND Buffer	1C
101628	IC, 74S64 4-2-3-2-Input AND/OR INV	2C
101629	IC, SN74S74 Dual D-Type F/F	3B,5C
101630	IC, 74S112 Dual J-K Edge Trig F/F	4C,6C,1H
101637	IC, SN74S260 Dual 5-Input Pos NOR	3D
101655	IC, 74S02 Pos NOR Totem-Pole	2B
101709	IC, 74LSOO Quad 2-Input NAND	5H
101710	IC, 74LS02 Quad, 2-Input NOR	5R
101711	IC, 74LS08 Quad 2-Input AND	2E
101712	IC, 74LS10 Triple Input NAND	5L
101714	IC, 74LS32 Quad 2-Input OR	2D,5E,5K,1G,4D
101719	IC, 74LS38 3-8 Line Decoder/DeMUX	3н,4н
101740	IC, 74LS51 Dual 2-Wide W-IN-AND-OR-INV	5D
101741	IC, 74LS74 Dual D-Type Pos Edge-Trig F/F	6F,5H
101776	IC, 74LS11 Triple 3-Input Pos AND	5G
161009	IC, 74S240 Octal Buffer 3-State TTL	2H,1K,2N,1F
161010	IC, 74S241 Octal Non-Inv Buffer 3-State	2К
161023	IC, 74LS73 Octal D-Type F/F	6J
161064-001	IC, 74LS40 Octal Buffer/Line Driver 3-State	5J
161065-001	IC, 74LS74 Octal Register D-Type F/F	1N,6P
161066-001	IC, 74LS45 Octal Bus XCVR	5P
161068-001	IC, 74LS44 Octal Buffer/Line Driver	6Н

Table 6-5. MTCS Controller PCBA Parts List (continued)

PART NUMBER DESCRIPTION

REFERENCE DESIGNATION

	Integrated Circuits		
161076-001	IC, 74S133 13-Input NAND	1D	
161107-002	IC, RAM Static 2Kx8 100ns	4E,4R	
161111-001	IC, 74LS40 Octal Bus XCVR	5N	
161134-001	IC, 74LS34 Octal D-Reg Inv 3-State	1L,2L,1M,2M	
161145-001 162002-002	IC, 74LS97 Sync U/D Binary Counter IC, Z80A 8-Bit Micro-P	2J,1P,2P,1R,2R 4K	
162002-002	IC, 200A 8-BIC MICHO-P IC, 8253-5 Programmable Interval Timer	4K 4M	
162043-001	IC, 8x60 FIFO RAM Controller	4G	
165047-012	IC, PROM 8Kx8 2764 MTCS Control Firmware	4N	
168001-001	IC, 74F157 Quad 2-Input MUX	1B	
168002-001	IC, 74F240 Octal Buffer/Line Driver 3-State	бL	
168002-002	IC, 74F245 Octal Bidir XCVR 3-State	бN	
168002-003	IC, 74F374 Octal D F/F 3-State	6R	
911008-001 911009-001	IC, PAL Tape Sequencer	6G 2F	
911009-001 911009-002	IC, PAL Controller/Host Sequencer IC, PAL Host To Controller Sequencer	2F 2G	
911010-001	IC, PAL MOSt TO CONTROLLED Sequencer IC, PAL MTCS Controller	2G 1J	
911010 001		10	
	Resistors		
111000-031	Resis, Comp IK Ohm 5%	Rl,2,6,7,8,13	
111000-034	Resis, Comp 82K Ohm 5%	R4	
111000-039	Resis, Comp 22 Ohm 5%	R5	
111000-047 112001-013	Resis, Comp 200 Ohm 5% Resis, Comp 56 Ohm 0.5W 5%	R9 R3	
101053	Resis Ntwk, DIP 220/330 Ohm 14-Pin	R3 R11(6M)	
119000-003	Resis Ntwk, DIP 1K Ohm 16-Pin 15 Resis	R10(3C)	
119001-002	Resis Ntwk, DIP 1K Ohm 8-Pin 7 Resis	R12	
Sockets			
325005-001	Socket, IC DIP 4-Leaf Cont Gold 24-Pos	(4E.4M.4R)	
325005-007	Socket, IC DIP 4-Leaf Cont Gold 28-Pos	(4N,4G)	
325005-010	Socket, IC DIP 4-Leaf Cont Gold 40-Pos	(4K)	
325005-011	Socket, IC DIP 4-Leaf Cont Gold 20-Pos	(1J,2F,2G,6G)	
Switches/Transistors			
331005-002	Switch, DIP SPST 8-Pos	S1(1A)	
141018-001	Transistor, 2N2907A PNP Silicon Switch	Ql	
Miscellaneous			
MISCHIMICOUS			
907420-001	Catch, I/O PCBA		
907388-001	Ejector, Euro-DIN Conn Stack		
214027-001	Fastener, Push-On 0.312 Dia Stud	(=1 0)	
310019-001	Housing/Guide, Conn DIN 3x32	(J1,2)	
762022-003 907389-001	Label, Tab 0.375x1.250 Yel Latch, Euro-DIN Conn Stack		
907498-001	Plate, Cover MTC8C		
100114	Screwlock, Rnl 4-40xThd D Type		

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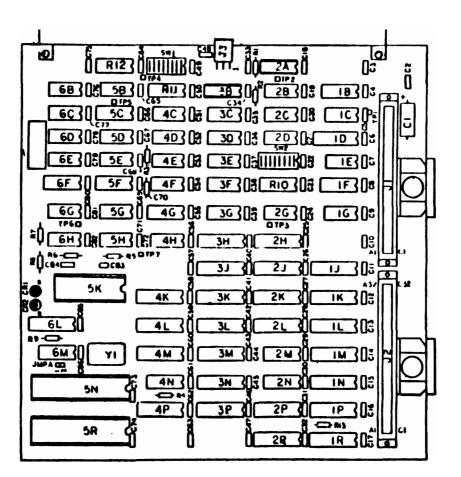


Figure 6-6. LAN Controller PCBA

Table 6-6. IAN Controller PCBA (MM531060) Parts List

PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION
903405-001 904773-001	PCBA, LAN Controller (MM531060) PCB, IAN Controller Diagram, Schematic	
	Capacitors	
104003-008	Capac, Ceram X7R $\overline{220}$ pFD $100V$ 20%	C83
104007-001	Capac, Ceram Z5U DIP 0.1 MFD 50V 20%	C2-69,71-82,84-86
104009-002	Capac, Ceram COG DIP 47 pFD 50V 5%	C70
102000-010	Capac, Tant 100 MFD 6V 20%	Cl
	Connectors	

300092-001	Conn, DIN Fn	l 3x32 Press-Fit 64-Pos	Jl,2
325026-001	Conn Hdr, So	l Row 1-Pos 0.100 Tail	TP1-7
325026-002	Conn Hdr, So	l Row 2-Pos 0.100 Tail	JMPA
325044-001	Conn Hdr, So	1 Row R/A LK 3-Pos	J3

Diodes

152001-001	LED,	Green Diff Lens	CR2
152001-002	LED,	fed Diff Lens	CR1

Integrated Circuits

101315 IC, 74S00 Quad 2-Input Pos NAND 2C	
101541 IC, 74S04 Hex Inverter 3D	
101623 IC, 74S11 3-Input AND 3C	
101625 IC, 74S32 Quad 2-Input Pos OR 5G,6G	
101627 IC, SN74S38 Quad 2-Input Pos NAND Buffer 1E,1G	
101628 IC, 74S64 4-2-3-2-Input AND/OR Inv 2G	
101629 IC, SN74S74 Dual D-Type F/F 1C,3G	
101630 IC, 74S112 Dual J-K Edge Trig F/F 1B	
101633 IC, SN74S157 Quad 2-1 Line Data Select/Mux 1F	
101637 IC, SN74S260 Dual 5-Input Pos NOR 2D	
101655 IC, 74S02 Pos NOR Totem-Pole 2B,3F	
101656 IC, 74S04 Hex Inverter 5B,5E	
101672 IC, 74LS20 Pos NAND 6C	
101709 IC, 74LS00 Quad 2-Input NAND 4D	
101711 IC, 74LS08 Quad 2-Input AND 4F,5H	
101712 IC, 74LS10 Triple Input NAND 4H	
101715 IC, 74S51 Dual 2-Wide 2-Input AND/OR Inv 2E	
101719 IC, 74LS138 3-8 Line Decoder/DeMUX 5F,6F	
101740 IC, 74LS51 Dual 2-Wide 2-Input AND/OR Inv 6B,6E	
101741 IC, 74LS74 Dual D-Type Pos Edge Trig F/F 4C,5D,4E	
101744 IC, 74LS174 Hex D-Type F/F 2M	
101783 IC, 74LS112 Dual J-K Edge Trig F/F 5C,4G,6M	
161009 IC, 74S240 Octal Buffer 3-State TTL 1D,1K,1L,1M	
161023 IC, 74LS273 Octal D-Type F/F 2J	
161064-001 IC, 74LS240 Octal Buffer Line OR 3-State 2K,2L,1N,3N,1P,3	P,1R

Т	able	6-6.	LAN	Controller	PCBA	Parts	List	(continued)

PART NUMBER EESCRIPTION

REFERENCE EESIGNATION

Integrated Circuits

161065-001	IC, 74LS374 Octal Register D-Type F/F	2H,3H,3J,4K,3L,4L, 2P,2R
161068-001	IC, 74LS244 Octal Buffer/Line Driver	1J,3K,6L,4M,4P
161074	IC, 74S244 Octal Buffer	3м
161076-001	IC, 74S133 13-Input NAND	4N
161085-001	IC, 7407 Hex Buffer/Driver	6н
161137-001	IC, 74LS54 4-Wide AND/OR Inv	6D
161138-001	IC, 74LS283 4-Bit Binary Full Adder	2N
161139-001	IC, 75174 Quad DIF Line Receiver	3B,IC75174
161140-001	IC, 75175 Quad DIF Line Driver	2A,IC75175
400548-001	IC Set, Data Link Controller	5K
400548-003	IC Set, Microproceser	5R
400548-002	IC Set, Unbuffered Gate Array	5N

Oscillators

150001-002	Oscillator,	Xtal	Clock	20	MHz	Yl
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Resistors

 111000-029
 Resis, Comp 330 Ohm 5%
 R7,8

 111000-031
 Resis, Comp 1K Ohm 5%
 R3,4,5,6,9,13

 111000-060
 Resis, Comp 4.7K Ohm 5%
 R1,2

 119000-003
 Resis Ntwk, DIP IK Ohm 16-Pin 15 Resis
 R12(5A)

 119000-004
 Resis Ntwk, DIP 4.7K Ohm 16 Pin 15 Resis
 R11(4B),R10(2F)

Sockets

325005-004	Socket,	IC DIP	4-Leaf	Cont	Gold	16-Pos	(2A,3B)
325005-007	Socket,	IC DIP	4-Leaf	Cont	Gold	28-Pos	(5K)
325005-010	Socket,	IC DIP	4-Leaf	Cont	Gold	40-Pos	(5N,5R)

Switches

331005-002 Switch, DIP SPST 8-Pos	SW1(4A) ,SW2(2E)
-----------------------------------	------------------

Miscellaneous

907420-001	Catch, 1/C PCBA	
907388-001	Ejector, Euro-DIN Conn Stack	
214027	Fastener, Push-On 0.312 Dia Stud	
310019-001	Housing/Guide Conn DIN 3x32 ML	(J1.2)
325033-001	Jumper, 0.025Sq Gold PL	(JMPA)
762022-003	Label, Tab 0.375x1.250 Yel	
907389-001	Latch, Euro-DIN Conn Stack	
907531-001	Plate, Conn LAN Controller	
208000-001	Rivet, Blind 0.116Dx0.188L Alum	
213005-003	Washer, Shoulder Insulating #4x0.135	

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	P 2	
		$\begin{array}{c} c_{106} \\ c_{118} \phi \\ BE \\ \phi \\ \hline 7E \\ \phi \\ \hline 6E \\ \phi \\ \hline 5E \\ \phi \\ \hline 4E \\ \phi \\ \hline 4E \\ \phi \\ c_{53} \\ \hline 3E \\ \phi \\ \hline 2E \\ \phi \\ \hline 2E \\ \phi \\ \hline IE \\ \phi \\ \hline e^{12} \\ \downarrow \\ \hline \end{array}$
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		C121 C109 C95 C81 4H 0 C42 C29 1 R 5 0 8H 0 7H 0 6H 0 3H 0 2H 0 1H 0
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A		CIIIQ 7K QC97 6K QCe3 5K Q RI Q 3K Q 2K QC3I IK QC17
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A		$\begin{bmatrix} c_{123} \\ BN \end{bmatrix} \phi^{C100} \\ \hline SN \end{bmatrix} \phi^{C86} \\ \hline SN \end{bmatrix} \phi^{C72} \\ \hline 4N \end{bmatrix} \phi^{C47} \\ \hline 2N \end{bmatrix} \phi^{C34} \\ \hline IN \end{bmatrix} \phi^{C20} \\ \hline C124 \\ \hline C12$
		$\begin{array}{c} \hline \\ \hline $

Figure 6-7. Winchester Drive (Single-Board) Controller PCBA

Table 6-7. WDC Controller PCBA (MM531150) Parts List

ITEM	PART NUM		UM	HREV	PART DESCRIPTION	STAT	REMARKS
0001	904923-001	1.000	ΕA	A	PCB 5 1/4 DISK CONTROLLER	REL	*
	762022-003	1.000	EA	C	LABEL TAB . 375X1. 250 YEL	REL	*
	165007-001	1.000	EA	F	IC PROM 256 BIPOLAR	REL	IN
0006	165007-004	1.000 1.000 2.000 2.000 1.000 3.000	EA	F	IC PROM 256 BIPOLAR	REL	3К
	165007-003	1.000	EA	F	IC PROM 256 BIPOLAR	REL	8B
0009	161008-001	2.000	EA	A	IC 2901 4-BIT PROCESSER SLICE - STANDARD	REL	4F, 4H
	101514	2.000	EA	A	IC 7438 BUFFER QUAD 2 INPUT NAND	RES	IK,8N
0012	101700	1.000	EA	A	IC 74125 QUAD BUS BUF GATE M/3 STATE OUT	RES	8A
0013	161005	3.000	EA	A	IC 74273 OCTAL D-TYPE FLIP-FLOP	RES	IP, 2J, 2M
	161015	1.000	EA	А		REL	2P
0016	101785	8.000	EA	А	IC 74LS193 4-BIT SYNC UP/DOWN COUNTER	RES	2B, 2C, 2D,2K, 2L, 3C,
							3D, 3L
0018	101315	4.000	EA	A	IC 74S00 QUAD 2 INPUT POS NAND GATE IC 74S02 POS-NOR GATE TOTEM-POLE	RES	2N, 6L, 6N, 7N
	101655	2.000			IC 74S02 POS-NOR GATE TOTEM-POLE	RES	3N,7K
	101541	3.000			IC 74S04 INVERTER HEX IC 74S08 QUAD 2 INPUT POS AND GATE IC 74S10 GATE TRIPLE 3-INPUT NAND	REL	3P, 6M,7H
	101615	3.000			IC 74SO8 QUAD 2 INPUT POS AND GATE	RES	4P, 6C, 7L
	101543	2.000			IC 74S10 GATE TRIPLE 3-INPUT NAND	RES	6K, 8J
	101624	1.000			IC 74S20 DUAL 4-INPUT NAND GATE	REL	3E
	101625	4.000			IC 74S20 DUAL 4-INPUT NAND GATE IC 74S32 QUAD 2 INPUT POSITIVE-OR GATE	RES	3M, 4N, 6B,7J
	101715	1.000			IC 74S51 DUAL 2 WIDE 2 IN AND OR INVERT		70
	101629	7.000	EA	C	IC SN74S74 DUAL D-TYPE FLIP/FLOP	REL	3A, 5K, 5M,5N, 6P,7P,€
	101673	1.000			IC 74S86 QUAD 2-INPUT EXCLUSIVE OR GATE		7B
	101631	3.000			IC 74S138 DECODER/DEMULTIPLXR	RES	1A, 2A, 3B
	161001	1.000				RES	7F
	101633	4.000			IC SN74S157 QUAD 2-1 LINEDATA SELECT/MUX		IF,10,6A,7A
	101635	4.000			IC 74S175 QUAD D-TYPE F/F	REL	IE, 4L, 4M, 8H
	101777	1.000			IC 74S175 GOAD D-IIPE F/F IC 74S182 (LOOK AHEAD CARRY GENERATOR)	RES	6H
	161009	11.000			IC 74S182 (LOOK AREAD CARRI GENERATOR)	REL	1C, ID, 1J, 1L, 1M,2E,
0055	101009	11.000	БЛ	л			8M,9C, 9D,9F, 90
0034	161010	1.000	EA	A	IC 74S241 OCTAL NON-INV BUFFER 3 STATE	RES	1H
0035	101726	3.000	ΕA	A	IC 74S251 DATA SELECT/MUX 3 STATE	RES	6D, 7D, 7E
0036	161007	9.000	EA	A	IC 74S253 DUAL-DATA SELECTOR 3 STATE	RES	3F, 3G,3H,3J,6E,6F,
							60, 6J, 7C
0037	161006	11.000	ΕA	A	IC 74S374 OCTAL D-TYPE FLIP-FLOP		20, 2H, 5A,SB,5C,5D,
							5E, 5J, 8C,8D,80
	119000-003				RES NTWK DIP 16 PIN 15 RES 1. OK OHM		Rl(4K », R2(8P)
	101051	3.000			IC RES NTWK 220/330 OHMS	REL	R3< 5P)• R4(9B), R5< 9H
		7.000			CAP SOLID TANTALUM 33UF 20% 10V	REL	C1-7
		117.000			CAP CERAMC Z5U AXIAL . 1UF +80 -20% 50V		C8-124
0046	104011-002				CAP CERAMIC X7R AXIAL 220PF 20% 100V	REL	C125
0048	325003-061	1.000	ΕA	D	CONN HDR .025SQ PCB 50 POS RA W/LG LATCH	RES	₽2
	325003-059	1.000 2.000 5.000	ΕA	D	CONN HDR .025SQ PCB 34 POS RA W/LG LATCH		P3,4
0050	325005-011	5.000	ΕA	F	SOCKET IC DIP FOUR-LEAF CONT GOLD 20 POS	REL	(4A, 4B, 4C,4D,4E)
0001	903460-001	1.000	EA	D	PCBA 5 1/4 DISK CONTROLLER		
0002	165006-128	1.000	EA	AH	IC 4096 BIT (512 X 8) BIPOLAR PROM-R 4A		
0003	165006-129	1.000	EA	AH	IC 4096 BIT (512 X 8) BIPOLAR PROM-R 4B		
0004	165006-130	1.000	EA	AH	IC 4096 BIT (512 X 8) BIPOLAR PROM-R 4C		
0005	165006-131	1.000	EA	AH	IC 4096 BIT (512 X 8) BIPOLAR PROM-R 4D		
0006	165006-132	1.000	ΕA	AH	IC 4096 BIT (512 X 8) BIPOLAR PROM-R 4E		
0002	165006-133	1.000	EA	AH	IC 4096 BIT (512 X 8) BIPOLAR PROM-M 4A		
	165006-134	1.000	EA	AH	IC 4096 BIT (512 X 8) BIPOLAR PROM-M 4B		
					IC 4096 BIT (512 X 8) BIPOLAR PROM-M 4C		
	165006-136	1.000 1.000	EA	AH	IC 4096 BIT (512 X 8) BIPOLAR PROM-M 4D		
	165006-137	1.000	EA	AH	IC 4096 BIT (512 X 8) BIPOLAR PROM-M 4E		

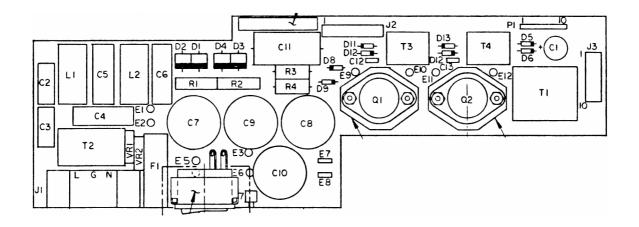


Figure 6-8. Power Supply Input Module PCBA

Table 6-8. Power Supply Input Module (MM533000) Parts List

ITEM	PART NUM	QTY-PER	UM	HREV	PART DESCRIPTION	REMARKS
					PCB INPUT MCOLLE P/S LABEL TAB .375X1.250 YEL THERMISTOR INRUSH PROTECT 15 AMP .03 OHM INTERIM COMPUNENT-PENDING SPEC RES CARBUN COMP ?? 5% 39K UHM CAP METAL FILM .047UF 10% 250 VAC INTERIM COMPONENT-PENDING SPEC	
0001	904761-001	1.000	EA	X1 D	PCB INPUT MCOLLE P/S	*
0002	122022-003	2 000	EA EA	в г	THERMISTOR INDIGU DROTECT 15 AMD 02 OUM	- - 1 - 2
0001	123004-003	2.000	DF	ъ v1	INTERIM COMDUNENT_DENDING SDEC	KI,Z VP1
0004	000000-000	1.000	KF	ΔI	INTERIM COMPONENT-PENDING SPEC	REISD D/N 199019-001
0003	113001-018	2.000	ΕA	D	RES CARBUN COMP ?? 5% 39K UHM	R3.4
0008	107006-002	1.000	EA	В	CAP METAL FILM .047UF 10% 250 VAC	C14
0009	000000-000	2.000	RF	X1	INTERIM COMPONENT-PENDING SPEC	C12,13 CAPACITOR .04
						7 BFIS P/N 104007-00
						3
0010	107006-00i	3.000	ΕA	В	CAP METAL FILM .47UF 10% 250 VAC	C4,5,6
0011	108019-002	1.000	EA	В	CAP FILM POLYFRCP 2.0UF +-10% 200VDC	C11
0012	105000-003	1.000	ΕA	С	CAP ALUM ELECT 390UF +100 - 10% 40V	C1
0013	00000-000	4.000	RF	X1	INTERIM COMPONENT-PENDING SPEC	C7,8,9,10 CAP 470 MF
0016	100005 001	1 000				BFIS P/N 108023-001
0015	130006-001	4.000	EA	A	DIODE SWITCHING IN9148	D10,11,12,13
0017	130016-001	2.000	LA	C	DIODE RECIFIER I AMP-IN4936	D8,9
0018	130000-002	2.000	EA EA	2	DIODE RECT IA 100V IN4002 DIODE DECTIETED LICU CUDDENT	D5,0
0019	152003-001	1 000	EA EA	R	LED	D1,5
0021	141021-001	2 000	EΑ	Δ	TRANSISTOR NON 2N66IS 10A 43118	01 2
0023	180054-001	1.000	EA	A	TRANSFORMER E*I BALDN	T2
0028	180053-001	2.000	EA	A	TRANSFORMER BASE CRWE	T3,4
0029	180055-001	1.000	EA	A	TRANSFORMER PC*£R 36V	T1
0030	135036-001	2.000	EA	А	INDUCTOR 40.2LH	L1,2
0031	137001-001	1.000	EA	С	FUSE GLASS TUBE FST BLUM 6A 250V	Fl
0033	338009-001	1.000	EA	A	FUSEHOLDER 3AG PC MOUNT	(F1)
0034	330006-001	1.000	EA	A	SWITCH ROCKER DPST SNAP-IN PNL PT 10 AMP	S1
0035	907485-001	1.000	ΕA	Х3	BRACKET PCB/SWITCH MOUNTING	*
0036	315062-001	1.000	ΕA	A	KECPT AC PWH PALE CEE 6A 230V PC BKC MT	Jl
0037	325042-001	1.000	EA	A	CONN HOR &GL POfe «i5&CIS .045SU 8 PG^	42
0038	325043-001	1.000	EA	A	CONN FML Sui PUM .100CTS HOK11 PT 10 HJS	J3
0039	000000-000	1.000	KF.	XI	INTERIM COMPONENT-PENOING SPEC	J4 BF1SU P/N J2502lh-OJl
0041	235023-001	4 000	ጉ እ	δ	HEATSINK TOLI SCICEPARIE	TOi»2)
0041 004b	214019-003	2 000	EA	Δ	NUT KEP 6-12	III +21
0047	202015-003	2.000	EA	C	SCREW ??? 4-4CX.31	1,711
0048	214019-001	2.000	EA	A	NUT KEP 4-40	тли
0049	222001-001	2.000	EA	D	AD INS SEMICCNO 10-03	
0050	784007-037	0.700	FT	в	WIRE INS 300V BOG UL1061 18AWG	*
0051	186000-020	0.200	FT	в	WIRE SOLID HOCK-UP	
	904761-001	1.000	EA	X1	PCB INPUT MODULE P/S	
0002	762022-003	1.000	ΕA	В	LABEL TAB .375X1.250 YEL	
0003	125004-003	2.000	EA	Е	THERMISTOR INRUSH PROTECT IS AMP .03 CHM	R1,2
0004	000000-000	2.000	RF	Xl	INTERIM CUMPOfcEfcT-PENOING SPEC	VR1t2
	112001 010	2 000	۳»	D	INTERIM COMPONENT-PENDING SPEC CAP METAL FILM .47UF 10% 250 VAC CAP FILM POLYFRCP 2.0UF +-10% 200VDC CAP ALUM ELECT 390UF +100 - 10% 40V INTERIM COMPONENT-PENDING SPEC DIODE SWITCHING 1N9148 DIODE RECTIFIER 1 AMP-1N4936 DIODE RECTIFIER HIGH CURRENT LED TRANSFORMER E*1 BALbN TRANSFORMER EASE CRWE TRANSFORMER PC*£R 36V INDUCTOR 40.2LH FUSE GLASS TUBE FST BLUM 6A 250V FUSEHOLDER 3AG PC MOUNT SWITCH ROCKER DPST SNAP-IN PNL PT 10 AMP BRACKET PCB/SWITCH MOUNTING KECPT AC PWH PALE CEE 6A 230V PC BKC MT CONN HOR &GL POFE «15&CIS .045SU 8 PG^ CONN HOR &GL POFE «15&CIS .045SU 8 PG^ CONN HCL SUI PUM .100CTS HOK11 PT 10 HJS INTERIM COMPONENT-PENOING SPEC HEATSINK TO-J SCLCERABLE NUT KEP 6-J2 SCREW ??? 4-4CX.31 NUT KEP 4-40 AD INS SEMICCNO 10-03 WIRE INS 300V BOG UL1061 18AWG WIRE SOLID HOCK-UP PCB INPUT MODULE P/S LABEL TAB .375X1.250 YEL THERMISTOR INRUSH PROTECT IS AMP .03 CHM INTERIM CUMPOFENT-PENOING SPEC	BFISD P/N l*9U9-COi
0000	107006-002	2.000	EA E7	л В	RES CARBCN CO^P I* 54 J9K OHM CAP METAL FIL* .04/UF 104 450 VIC INTERIM COMPONENT-PENDING SPEC	C14
0008	107000-002	2 000	DF	ъ v1	INTERIM COMPONENT_DENDING SDEC	114*13 CADACIIIIF+ 04
0009	000000-000	2.000	KF	ΔI	INIERIM COMPONENI-PENDING SPEC	7 BF1S P/N T0404T-0 C
						3
0010	107006-003	3.000	EA	в	CAP METAL FILM .47UF 10% 250 VAC	C495t6
0011	106019-002	1.000	EA	в	CAP FIL* POLVFRCP 2.0UF +-10% 200VAC	Cll
	105000-003	1.000	EA	С	CAP ALU* ELECT 390UF «100 -101 40%	Cl
0013	00000-0000	4.000	RF	X1	CAP METAL FILM .47UF 10% 250 VAC CAP FIL* POLVFRCP 2.0UF +-10% 200VAC CAP ALU* ELECT 390UF «100 -101 40% INTERIM COMPONENT-PENDING SPEC	C7,8,9,10 CAP 470 MF
						BEIS P/N 108023-001
0016	130006-001	4.000	EA	A	DIODE SWITCHING 1N9148	010tlltl2tlJ
0017	130016-001	2.000	ΕA	С	OIOOE RECTIFIER 1 AMP-1N4936	Oit9
0018	130000-002	2.000	EA	С	DIODE RECT 1A 100V 1N4002	D5»6
0019	150002 001	4.000	ĽА	A	DIODE RECTIFIER HIGH CURRENT	01tJt3t4
0021	152003-001	1.000	ĽА	в	ЦЕС	01

Table 6-8. Power Supply Input Module PCBA Parts List (continued)

ITEM	PART NUM	~		HREV	PART DESCRIPTION	REMARKS
0023	141021-001		EA	A	TRANSISTOR NPN 2N6675 10A 450V	
0027	180054-001	1.000	EA	A	TRANSFORMER E?I BALUN	12
0028	180053-001	2.000	EA	A	TRANSFORMER BASE DRIVE	13,4
0029	180055-001	1.000	EA	A	TRANSFORMER PCMEK J6V	II
0030	135036-001	2.000	EA	A	INDUCTOR 40.2UH	1.1
0032	137001-000	1*000	EA	С	FUSE GLASS TUBE FST BLU? 3A 250V	Fl
0033	338009-001	1.000	EA	A	FUSEHOLDER 3A PC MOUNT	
0034	3300C6-001	1.000	EA	A	SWITCH ROCKER DPST SNAP-IN PNL PT 10 AMP	S1
0035	907485-001	1.000	EA	X3	BRACKET PCB/SWITCH MOUNTING	*
0036	315062-001	1.000	EA	A	RECPT AC PWR MALE CEE 6A 250V PC BRO MT	Jl
0037	325042-001	1.000	EA	A	CONN HDR SGL RUW .156CTS .045SM B POS	J2
0038	325043-001	1.000	EA	A	CONN FML SGL ROW .100CTS HU??? PT 10 POS	J3
0039	000000-000		RF	X1	INTERIM COMPONENT-PENDING SPEC	J4
						BFISD P/N 325026-0
0041	235023-001	2.000	EA	А	HEATSINK TO-3 SOLDERABLE	(????)
0046	214019-003			А	NUT KEP 6-32	
0047	202015-003		EA	С	SCREO HWH 4-40X.31	(J1)
0046	214019-001		EA	A	SCREQ HWH 4-40X.31 NUT KEP 4-40	(JT1)
0049	22200i-00i		EA	D	PAD INS SEMICCND TO-03	*
0050	784007-037			В	WIRE INS 300V 80C UL1061 18AWG WHITE	
0051	786000-020		FT	в	WIRE SOLID HOCK-UP	*
0051	/00000-020	0.200	r 1	Б	WIKE SOUTD HOCK-OF	

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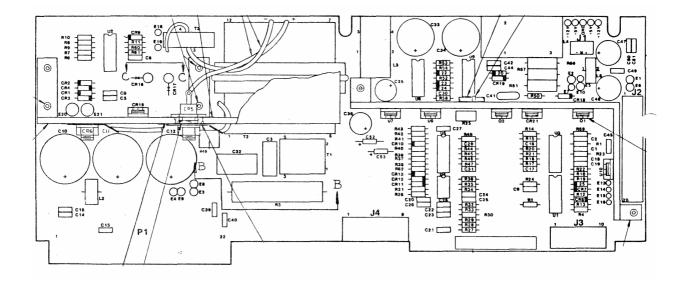


Figure 6-9. Power Supply Output Module PCBA

Table 6-9. Power Supply Output Module PCBA (MM533000) Parts List

ITEM	PART NUM	QTY-PER	UM	HREV	PART DESCRIPTION	STAT	REMARKS
0001	904859-001	1.000	EA				*
0002		1.000	EA		PCB POWER SUPPLY OUTPUT MODULE LABEL TAB . 375X1. 250 YEL RES METAL FILM . 125W IX 11.0 OHM RES METAL FILM . 125W IX 22.6 OHM PES METAL FILM . 125W IX 1 . 18K OHM	REL	*
0003	116000-229	3.000	EA		RES METAL FILM . 125W IX 11.0 OHM	REL	R11,60,61
0004	116000-230	1.000	EA		RES METAL FILM . 125W IX 22. 6 OHM	REL	R8
0005	116000-231	1.000	EA				R7
0006	116000-201	1.000	EA		RES METAL FILM . 125W IX 1. 18K OHM RES METAL FILM . 125W IX 2 80K OHM	REL	R6
0007		1.000	EA		RES METAL FILM . 125W IX 3. 74K OHM	REL	R16
0008	116000-031	12.000	EA		RES METAL FILM . 125W IX 2 80K OHM RES METAL FILM . 125W IX 3. 74K OHM RES METAL FILM . 125W IX 4 99K OHM	REL	R15,17,18,20,22,23 26,32,35,42,29,47
0009	116000-233	1.000	EA	P	PES METAL ETLM 125W 18 6 04K OHM	PFT.	R9
0010	116000-117	1.000	ΕA	P	RES METAL FILM . 125W 1% 15 OK OHM RES METAL FILM . 125W 1% 15 OK OHM RES METAL FILM . 125W 1% 16. 9K OHM RES METAL FILM . 125M 1% 20. OK OHM RES METAL FILM . 125W 1% 23. 2K OHM	REL	R39
0011	116000-228	1.000	ΕA	P	RES METAL FILM . 125W 1% 16. 9K OHM	REL	R14
0012	116000-177	4.000	ΕA	P	RES METAL FILM . 125M 1% 20. OK OHM	REL	R27,37,38,45
0013	116000-108	1.000	EA	P	RES METAL FILM . 125W 1% 23. 2K OHM	REL	R19
0014	101918	1.000	EA	P	RES METAL FILM . 125W 1% 29. 4K OHM	REL REL	R40
0019	116000-215	2.000	EA	P	RES METAL FILM . 125W 1% 40 2K OHM	REL	R34,46
0016	116000-235	1.000	EA		RES METAL FILM . 125M 1% 46. 4K OHM	REL	R21
0017	101915	1.000	EA		RES METAL FILM . 125W 1% 100K OHM	REL	R43
0018	116000-232	1.000	EA		RES METAL FILM . 125W 1% 4. 32K OHM RES METAL FILM . 125W 1% 15. 8K OHM	REL	Rl
0019	116000-234	1.000	EA		RES METAL FILM . 125W 1% 15. 8K OHM	REL	R59
0020	116000-156	1.000	EA		RES METAL FILM . 125W 1% 1 65K OHM	REL	R28
0022	101917	1.000	EA		RES METAL FILM . 125W 1% 10. OK OHM	REL	R30
0024	116000-205	1.000	5	P	RES METAL FILM . 125W 1% 4. 87K OHM	INA	R44
0028	116000-107	1.000	EA	P	RES METAL FILM . 125W 1% 22 6K OHM	REL	R33
0"^	111000-031	3.000	EA	L	RES METAL FILM . 125W 1% 15. 6K OHM RES METAL FILM . 125W 1% 1 65K OHM RES METAL FILM . 125W 1% 10. 0K OHM RES METAL FILM . 125W 1% 4. 87K OHM RES METAL FILM . 125W 1% 22 6K OHM RES CARBON FILM . 25W SX IK OHM	REL	R52, 53. 54
С	111000-032	1.000	EA	L	RES CARBON FILM . 25W 5X 2. OK OHM	REL REL	R50
00	111000-085	1.000	EA	L	RES CARBON FILM . 25W 5X 2. 7K OHM	REL	R24
0032	111000-091	2.000	EA	L	RES CARBON FILM . 25W 5X 3. 9K OHM	REL	R4, 10
0033	111000-060	5.000	EA	L	RES CARBON FILM . 25W 5X 4. 7K OHM	REL REL	R12,31,36,48,62
0034	111000-009	1.000	EA	L	RES CARBON FILM . 25W 5X 1. 5K OHM	REL	R41
0035	111000-065	2.000	EA	L	RES CARBON FILM . 25W 5X 20K OHM	REL	R2,13
0036	111000-095	1.000	EA	L	RES CARBON FILM . 25W 5X 1. 5K OHM RES CARBON FILM . 25W 5X 1. 5K OHM RES CARBON FILM . 25W 5X 20K OHM RES CARBON FILM . 25W 5X 51 OHM RES CARBON COMP 1W SX 10 OHM RES PWR WW 3W 0.04 OHM IX RES PWR WW 10W 100 OHMS 5X DEC CARBON COMP 1W 5K 0.2 CMM	REL	R58
0038	113000-001	1.000	EA	Е	RES CARBON COMP 1W SX 10 OHM	REL	R51
0040	115006-011	2.000	EA	D	RES PWR WW 3W 0.04 OHM IX	REL	R56. 57
0041	115009-006	1.000	EA	В	RES PWR WW 10W 100 OHMS 5X	REL	R3
0042	113000-109	1.000	EA	Е	RES PWR WW 10W 100 OHMS 5A RES CARBON COMP 1W 5X 8.2 OHM RES DWR WW 5W 33 OHM 10X	REL	R5
0043	115003-005	1.000	EA	В	RES PWR WW 5W 33 OHM 10X	REL	R49
0045	118005-011	1.000	EA	В	POT RD CERMET LOW SINGLE TURN 500 OHM	REL	R25
0051	104008-007	2.000	EA	В	POT RD CERMET LOW SINGLE TURN 500 OHM CAP CERAMIC X7R DIP 330PF 5X 50V	REL	C26. 31
0052	104008-008	1.000	EA	В			C27
0053	104008-003	2.000	EA	В	CAP CERAMIC X7R DIP 1000PF 5X 50V CAP CERAMIC X7R DIP . 022UF SX 50V	REL	C1.6
0054	104011-006	1.000	EA	A	CAP CERAMIC X7R AXIAL 8, 200PF 5X 50V	REL	C2
0055	104008-005	1.000	EA	в	CAP CERAMIC X7R AXIAL 8, 200PF 5X 50V CAP CERAMIC X7R DIP 01UF 5X 50V	PEL	C21
0056	104011-011	1.000		A			C22
0057	104008-009	1.000		В	CAP CERAMIC X7R AXIAL . O33UF 5X 50V CAP CERAMIC X7R DIP 3300PF 5X 50V	REL	C23
0059	104009-002	1.000	EA		CAP CERAMIC COG DIP 47PF 5X 50V		C25

Table 6-9. Power Supply Output Module PCBA Parts List (continued)

ITEM	PART NUM	QTY-PER	UM	HREV	PART DESCRIPTION	STAT	REMARKS
0063	104010-002	10.000	ΕA	В	CAP CERAMC Z5U AXIAL .01UF 20% 100V CAP CERAMC Z5U AXIAL .1UF +80 -20% 50V CAP SOLID TANTALUM 1 OUF 20% 35V CAP FILM POLYPROPLENE .01UF 5% 400VDC CAP MICA DIDPED PADDAL 2000DE 5% 500V	REL	C5,14,15,16,17,18, ,42,50,51
0066	104010-001	12.000	EA	В	CAP CERAMC Z5U AXIAL .1UF +80 -20% 50V	REL	C8,9, 13, 20,28,29,3 39, 40, 44, 45, 49
0067	102000-006 107001-003 103000-003 108000-008	2.000	EA	Н	CAP SOLID TANTALUM 1 OUF 20% 35V	REL	C52,53
0070	107001-003	1.000	EA	A	CAP FILM POLYPROPLENE .01UF 5% 400VDC	REL	C32
0071	103000-003	1.000	EA	0	CAP MICA DIPPED RADIAL 3000PF 5% 500V	REL	C3
0072	108000-008	1.000	EA	Е	CAP FILM POLYESTER .022UF 10% 600V	REL	C4
0073	104003-002 108022-005	2.000	EA	Н	CAP MICA DIPPED RADIAL 3000PF 5% 500V CAP FILM POLYESTER .022UF 10% 600V CAP CERAMIC X7R .1UF 10% 50V CAP ALUM ELECT MINI 100UF +-20% 35V	REL	C24,41
0074	108022-005	2.000	EA	D	CAP ALUM ELECT MINI 100UF +-20% 35V	REL	C35, 36
0075	108024-001	2.000	EA	A	CAP ALUM ELECT ESR/LIFE 330UF +100% 16V	REL	C47,48
0076	108024-001 108020-002	2.000	EA	D	CAP ALUM ELECT ESR/LIFE 330UF +100% 16V CAP ALUM ELECT LOW ESR PCB 560UF 40V	REL	C33,34
0077	108020-003	3.000	EA	D	CAP ALUM ELECT LOW ESR PCB 4,700UF 7.5V	REL	C10,11,12
0080	108020-003 130006-001	11.000	EA	A	DIODE SWITCHING 1N914B	REL	CR1,2,3,4,7,8,10,1
							12,24,25
0081	130016-001	4.000	EA	С	DIODE RECTIFIER 1 AMP-1N4936	REL	CR9,19,20,22
0082	130008-001	2.000	EA	A	DIODE PWR SCHOTTKY SD51 120A 45 PIV	REL	CR5,6
0083	130025-002	1.000	EA	В	DIODE DUAL 16A T0220 150V	REL	CR15
0084	130001-001	2.000	EA	D	DIODE FST RECOVERY MR852	REL	CR16,17
0085	130026-001	1.000	EA	A	DIODE SCHOTTKY 10A T0220 45V	REL	CR21
0086	101304	1.000	EA	0	DIODE ZENER 1N5242B	REL	CR23
0087	130016-001 13008-001 130025-002 130001-001 130026-001 101304 131002-033	1.000	EA	C	DIODE ZENER 1N4747A	REL	CR18
0088	131001-007	1.000	EA	0	DIODE ZENER 500MW 1N5233B	REL	CR13
0090	101323	1.000	EA	AX1	TRANS TIP 121	RES	Ql
0091	142003-001	1.000	EA	A	TRANS N-CHANNEL MOSFET 27A 60V	REL	Q2
0094	101799	4.000	EA	В	IC LM339 QUAD COMPARATOR	REL	U1,2,3,5
0095	164009-001	1.000	ΕA	A	IC LM358 DUAL LOW POWER OP AMP	REL	U4
0096	162049-001	1.000	ΕA	A	IC 4011 CMOS QUAD 2-INPUT NAND	REL	U6
0097	141020-001	1.000	ΕA	A	TRANSISTOR QUAD 3725 NPN	REL	U9
0098	101697	1.000	EA	В	IC MC7812CT 3 TERM POS VOLT REG	REL	U10
0099	132006-002	1.000	EA	A	REG NEG VOLTAGE 1.5A -5.2V 7905	REL	U7
0100	132006-006	1.000	EA	A	REG NEG VOLTAGE 1.5A -12.5V 7912	REL	U8
0109	131002-033 131001-007 101323 142003-001 101799 164009-001 162049-001 141020-001 101697 132006-002 132006-000 180056-001 180058-001 135037-002 135040-001 135038-001	1.000	ΕA	Е	CAP ALUM ELECT LOW ESR PCB 560UF 40V CAP ALUM ELECT LOW ESR PCB 4,700UF 7.5V DIODE SWITCHING 1N914B DIODE RECTIFIER 1 AMP-1N4936 DIODE PWR SCHOTTKY SD51 120A 45 PIV DIODE DUAL 16A T0220 150V DIODE FST RECOVERY MR852 DIODE SCHOTTKY 10A T0220 45V DIODE SCHOTTKY 10A T0220 45V DIODE ZENER 1N5242B DIODE ZENER 1N5242B DIODE ZENER 500MW 1N5233B TRANS TIP 121 TRANS N-CHANNEL MOSFET 27A 60V IC LM339 QUAD COMPARATOR IC LM339 QUAD COMPARATOR IC LM358 DUAL LOW POWER OP AMP IC 4011 CMOS QUAD 2-INPUT NAND TRANSISTOR QUAD 3725 NPN IC MC7812CT 3 TERM POS VOLT REG REG NEG VOLTAGE 1.5A -5.2V 7905 REG NEG VOLTAGE 1.5A -12.5V 7912 TRANSFORMER CURRENT SENSE INDUCTOR 19UH 50A INDUCTOR 0.22UH INDUCTOR 180UH COUPLED CONN HDR RT ANG .045SQ .156CTS 3 POS CONN HDR RT ANG .045SQ .156CTS 3 POS	RES	Т2
0110	180057-001	1.000	ΕA	A	TRANSFORMER CURRENT SENSE	REL	Tl
0111	180058-001	1.000	ΕA	В	TRANSFORMER CURRENT SENSE	REL	Т3
0112	135037-002	1.000	ΕA	С	INDUCTOR 19UH 50A	RES	L1
0113	135040-001	2.000	ΕA	В	INDUCTOR 0.22UH	REL	L2. 5
0114	135038-001 135039-001 325014-002 325043-002	1.000	ΕA	В	INDUCTOR 90UH 10A	PRF	L4
0115	135039-001	1.000	ΕA	C	INDUCTOR 180UH COUPLED	REL	L3
0118	325014-002	1.000	ΕA	A	CONN HDR RT ANG .045SQ .156CTS 3 POS	REL	Jl
0119	325043-002	1.000	ΕA	~	COMM FML SOL ROW .IUUCIS HORIZ MI 20 F05	REL	J2
0120	325043-001	1 000	ΕA	A	CONN FML SOL ROW .100CTS HORIZ MT 10 POS	REL	J3
0121	325043-001 300096-001	1.000	EA	A	CONN FML HDR 156 CTS RT/ANG PC MT 8 POS	RES	J4
0123	907594-001 907479-001	1.000	EA	A	HEATSINK 1 OUTPUT MODULE PCBA CABLE ASSY P/S DRIVE 1&2	REL	*
0125	907479-001	1.000	EA	С	CABLE ASSY P/S DRIVE 1&2		
0127	784007-037	9.000	FΤ	С	WIRE INS 300V 80C UL1061 18AWG WHITE	REL	*

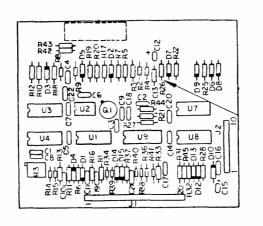


Figure 6-10. Power Supply Control Module PCBA

Table 6-10. Power Supply Control Module PCBA (MM533000) Parts List

ITEM	PART NUM	QTY-PER	UM	HREV	PART DESCRIPTION	REMARKS
0001	004765-001	1 000	ር እ	D	DCD CONTROL MODILE D/C	*
0003	762022-003 325026-037 325026-038 116000-156 116000-166 116000-226 116000-229	1.000	EA	C	LABEL TAB .375X1.250 YEL	*
0004	325026-037	1.000	EA	AX3	CONN HDR SOL ROW .100 10 POS .275 LG	J2
0005	325026-038	1.000	EA	AX3	CONN HDR SOL ROW .100 20 POS .275 LG	
0006	116000-156	1.000	EA	N	RES METAL FILM .125W 1% 1.65K OHM	R4
0007	116000-166	1.000	EA	N	RES METAL FILM .125W 1% 2.49K OHM	R33
0008	116000-226	1.000	EA	N	RES METAL FILM .125W 1% 5.49K OHM	R2
0009	116000-195	5.000	EA	N	RES METAL FILM .125W 1% 5.49K OHM RES METAL FILM .125W 1% 11.0K OHM	R9, 34,36,38*40
0010	116000-228	1.000	EA	N	RES METAL FILM .125W 1% 11.0K OHM RES METAL FILM .125W 1% 16.9K OHM RES METAL FILM .125W 1% 16.9K OHM RES METAL FILM .125W 1% 105K OHM RES METAL FILM .125W 1% 121K OHM RES CARBON FILM .125W 1% 787K OHM RES CARBON FILM .25W 5% 10 OHM RES CARBON FILM .25W 5% 30 OHM RES CARBON FILM .25W 5% 2.0K OHM RES CARBON FILM .25W 5% 15K OHM RES CARBON FILM .25W 5% 15K OHM	R8
0011	116000-127	1.000	ΕA	N	RES METAL FILM .125W 1% 24.3K OHM	R39
0012	116000-227	1.000	ΕA	N	RES METAL FILM .125W 1% 105K OHM	R41
0013	116000-225	1.000	ΕA	N	RES METAL FILM .125W 1% 121K OHM	R15
0014	116000-236	1.000	ΕA	N	RES METAL FILM .125W 1% 787K OHM	R14
0017	111000-001	2.000	EA	J	RES CARBON FILM .25W 5% 10 OHM RES CARBON FILM .25W 5% 30 OHM RES CARBON FILM .25W 5% 680 OHM	R26,32
0018	111000-040	1.000	ΕA	J	RES CARBON FILM .25W 5% 30 OHM	R3
0019	111000-055	4.000	ΕA	J	RES CARBON FILM .25W 5% 680 OHM	R22, 25,28,31
0020	111000-032	3.000	ΕA	J	RES CARBON FILM .25W 5% 2.0K OHM	R21,27,43
0021	111000-006	2.000	ΕA	J	RES CARBON FILM .25W 5% 15K OHM	RIO,37
0022	111000-065	8.000	EA	J	RES CARBON FILM .25W 5% 10K OHM RES CARBON FILM .25W 5% 100K OHM RES CARBON FILM .25W 5% 100K OHM RES CARBON FILM .25W 5% 10M OHM RES CARBON FILM .25W 5% 10M OHM	R7, 11, 12, 17, 18, 19
						20, 42
0023	111000-071	2.000	EA	J	RES CARBON FILM .25W 5% 100K OHM	R6, 13
0024	111000-123	1.000	EA	J	RES CARBON FILM .25W 5% 300K OHM	R5
0025	111000-072	1.000	EA	J	RES CARBON FILM .25W 5% 1M OHM	R16
0026	111000-099	1.000	EA	J	RES CARBON FILM .25W 5% 10M OHM	Rl
0027	111000-047	2.000	EA	J	RES CARBON FILM .25W 5% 10M OHM RES CARBON FILM .25W 5% 200 OHM	R44,45
0030	118008-002	1.000	EA	AX1	POT SQ MULTI TURN . 5W 5K OHM 10% CAP CERAMIC X7R DIP 1500PF 5X 50V	R35
0031	104008-001	3.000	EA	В	CAP CERAMIC X7R DIP 1500PF 5X 50V	C3,4,20
0032	104008-005	1.000	EA	В	CAP CERAMIC X7R DIP .01UF 5% 50V	C17
0033	104010-002	5.000	EA	A	CAP CERAMC Z5U AXIAL .01UF 20% 100V CAP CERAMIC X7R DIP .022UF 5% 50V	Cl, 11, 13, 16,2
0034	104008-003	1.000	EA	В	CAP CERAMIC X7R DIP .022UF 5% 50V	CIO
0035	111000-071 111000-123 111000-072 111000-099 111000-047 118008-002 104008-001 104008-005 104010-002 104008-003 104010-001	9.000	EA	A	CAP CERAMC Z5U AXIAL .1UF +80 -20% 50V	C5,6,7,8,9,14,18,19
						22
0036	102004-001	2.000	EA	В	CAP TANT 1UF 10% 35V	C12, 15
0037	104008-012	1.000	ΕA	В	CAP CERAMIC X7R DIP 820PF 5% 50V	C21
0038	906895-001	1.000	ΕA	В	CUSHION RETAINER .25X.75	*
0040	130006-001	12.000	EA	A	DIODE SWITCHING 1N914B	Dl,3,4,6,7,8,9,10,
						12,13,14, 15
0041	131002-028	2.000	EA	С	DIODE ZENER 1N4733A	D2,5
0042	141018-001	1.000	ΕA	A	CAP TANT 1UF 10% 35V CAP CERAMIC X7R DIP 820PF 5% 50V CUSHION RETAINER .25X.75 DIODE SWITCHING 1N914B DIODE ZENER 1N4733A TRANSISTOR PNP SILICON SWITCH 2N2907A TRANSISTOR OUAD 3725 NPN	Ql
0043	141020-001	2.000	ΕA	A	TRANSISTOR QUAD 3725 NPN	U7,8
0044	101799	3.000	EA	В	IC LM339 QUAD COMPARATOR	Ul,3,4
0045	132003-001	1.000	EA	В	TRANSISTOR QUAD 3725 NPN IC LM339 QUAD COMPARATOR IC 3524 VOLTAGE REG	U9
0046	131002-028 141018-001 141020-001 101799 132003-001 164010-001	1.000	EA	A	IC, VOLTAGE REFERENCE 2.5 VOLTS	U2

SECTION VII

5.25" FLOPPY DISK DRIVE

7.1 INTRODUCTION

This section provides maintenance personnel with information necessary to install, operate and maintain the 5.25" Floppy Disk Drive.

Section VII is arranged in three subsections. The scope of each subsection is described as follows:

- 7.1 INTRODUCTION contains general information, physical and electrical descriptions and equipment specifications.
- 7.2 INSTALLATION AND MAINTENANCE contains information to enable maintenance personnel to install and repair the Floppy Disk Drive. Electrical and mechanical adjustments are included.
- 7.3 REFERENCE INFORMATION Contains description of input and output lines, system timing diagram, schematics and jumper connections.

7.1.1 General Description

The 5.25" Floppy Disk Drive is a removeable-media, magnetic, rotating, data storage device. Its purpose is to allow the Model 4108 Base Unit to store and retrieve blocks of data (records) onto and from a rotating disk, thus providing secondary storage for the MAI® 2000 Series Computer System. The Drive functions as an input/output device in the Base Unit. Access to data is provided by one moving head per disk surface. Data is recorded on the disk surfaces using modified frequency modulation (MFM) techniques.

The Drive incorporates an open-loop, stepper motor positioning system. The major mechanical components of the Drive are illustrated in figure 7-1 through figure 7-3 and are explained in the following paragraphs.

7.1.1.1 Spindle Mechanism

The Spindle Mechanism comprises the Spindle, a Center Cone, a Main Arm and a Clamp Lever (see figure 7-1). Inserting a mini-floppy disk and pressing the button for loading the disk causes the Clamp Lever to lower the Main Arm and the Center Cone to enter the hole of the disk. The Center Cone catches the inside diameter of the disk and sets it to the correct position. To eject the disk, pressing the button (again) causes the Main Arm to be raised (by a spring), the Center Cone to be raised, and the disk to be released from the Spindle and ejected. The DC Motor drives the Spindle at 300 rpm, fixed speed.

7.1.1.2 Positioning Mechanism

The Positioning Mechanism comprises the Stepper Motor, the Carriage Assembly, a Guide Bar, a Pulley, and a Steel Belt (see figure 7-2). The rotation of the

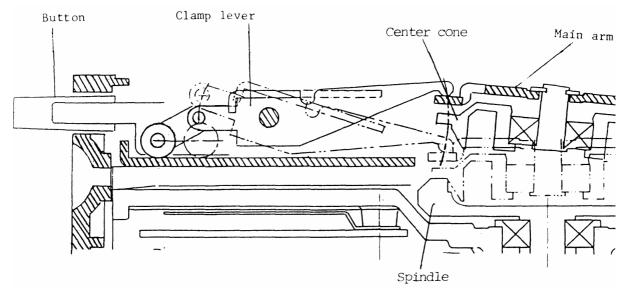


Figure 7-1. Spindle Mechanism

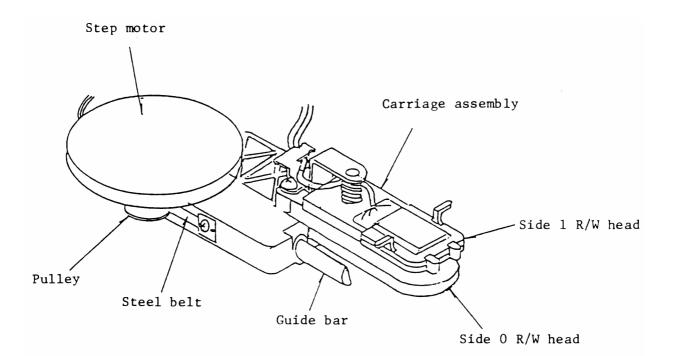
Stepper Motor is converted into rectilinear motion, by the Pulley/Steel Belt assembly (connected directly to the Stepper Motor axle), to drive the Carriage Assembly. The Carriage Assembly consists of the Carriage, the Side 0 R/W Head, and the Side 1 R/W Head. The Stepper Motor rotates 3.6 degrees per step.

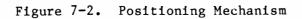
7.1.1.3 Head Load/Interlock Mechanism

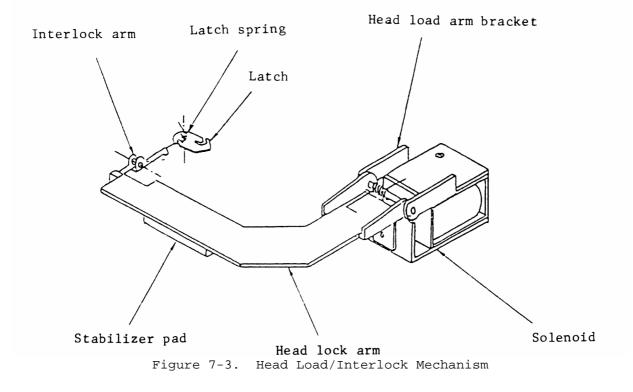
The Head Load/Interlock Mechanism consists of a Solenoid, the Head Load arm, the Stabilizer Pad, the Head Load Arm Bracket, the Interlock Arm, and a Latch and Latch Spring (see figure 7-3). When the Solenoid is actuated by the HEAD LOAD signal, the Head Load Arm is pulled down, and the Stabilizer Pad presses the disk to prevent the disk from vibrating. Also, the Side 1 R/W Head is pressed against the disk. Moreover, since the Interlock Arm presses the Latch Spring, the Latch does not move, and the disk cannot be ejected. When the HEAD LOAD signal is turned off, the Stabilizer Pad and the Side 1 R/W Head move from the disk, thus lowering the Interlock Arm and moving the Latch. In this state, the disk can be ejected.

7.1.2 Functional Concepts

The simplified block diagram in figure 7-4 shows the functional concepts of the Floppy Disk Drive. The Drive uses LSls for the major circuits, thus reducing the number of circuit parts to 25 percent of the amount used in conventional products. This increases the reliability of the Drive and miniaturizes the PCB space, thereby realizing a very thin unit. These LSIs are of custom analog-hybrid and digital-hybrid designs, each of which accommodates the following circuit functions.

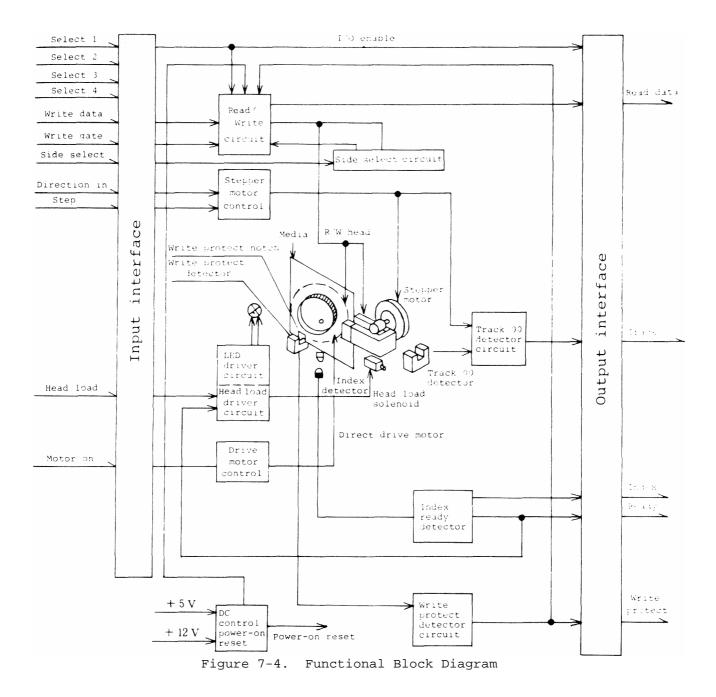






Analog System	DC Control Circuit Erase Amplifier Circuit Read Amplifier Circuit Write Circuit
Digital System	Stepper Motor Control Circuit Index Ready Circuit Write Protect Circuit Head Load Solenoid Control Circuit

Brief explanations of the major circuits are presented in the following paragraphs.

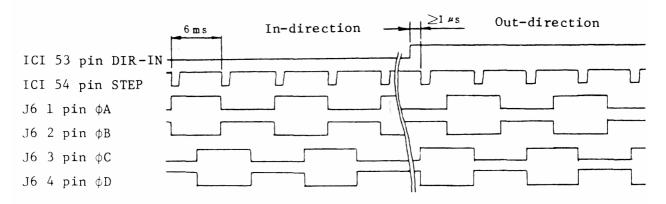


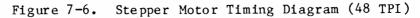
7.1.2.1 Stepper Motor Control

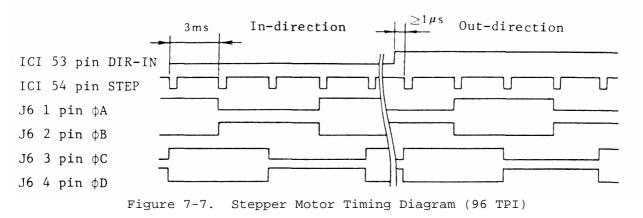
The Stepper Motor is a 4-phase DC motor. The circuit in ICl controls the motor (see figure 7-5 for a block diagram of the Stepper Motor Control Circuit). The STEP signal rotates the motor 3.6 degrees (48 TPI) or 1.8 degrees (96 TPI). The rotation of the Stepper Motor is converted to linear motion of the Read/ Write Heads by the Pulley/Steel Belt assembly. The DIRECTION-IN signal controls the movement of the heads toward the inner tracks with a logic low level and toward the out tracks (toward track 00) with a logic high level. Figure 7-6 and figure 7-7 show the Stepper Motor timing. Figure 7-8 is a Stepper Motor phase transfer chart.

	ICl			Driver			Stepper motor
Step 54		38	4	IC3	7	φA	<u> </u>
Select 50		37	6		3	фВ	
Direc-		36	4	IC4	7	φC	
tion in 53		35	6		3	φD	
			L				Ĺi









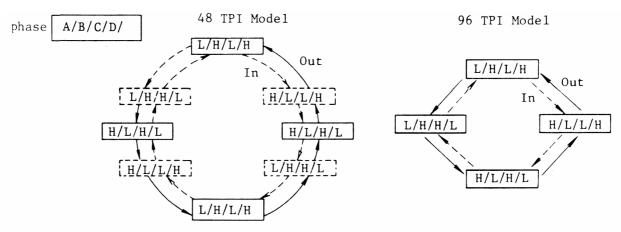


Figure 7-8. Stepper Motor Phase Transfer Chart

7.1.2.2 Drive Motor Control

The Drive Motor is a brushless DC motor and is controlled by the PCBA of the Drive Motor itself. The Drive Motor is started and stopped by the MOTOR-ON signal (Jl, pin 16). The Drive Motor reaches the optimum speed in 800 ms after the Motor has started. The speed is adjusted to 300 rpm (disk rotation speed) by the potentiometer located on the Drive Motor PCBA.

7.1.2.3 Head Load Circuit

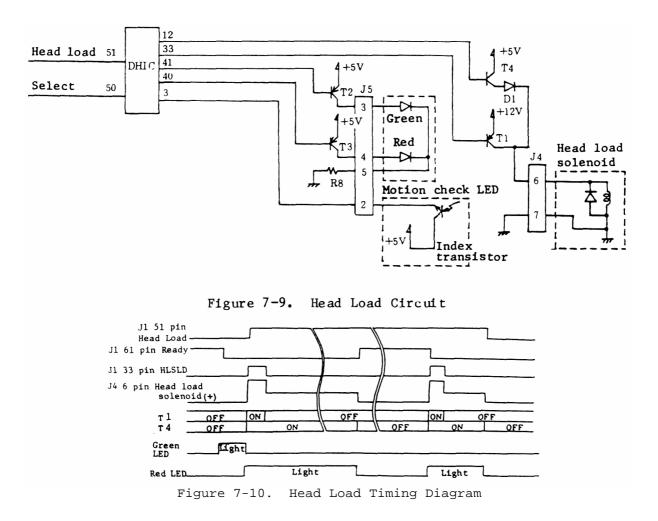
The Head Load mechanism is operated by the Solenoid. When transister Tl is turned on by a 36 ms one shot MV in 1C1, current is supplied to the Solenoid to actuate it. There are two methods to load the heads. One method, named SH (Select Head Load), is that the Head Load Solenoid is drawn when the Drive has been selected and the Head Load signal goes to logic low. Another method, named AH (Automatic Head Load), is that the Head Load Solenoid is drawn when the Drive is selected, irrespective of the Head Load signal condition. Figure 7-9 is a simplified schematic of the Head Load Circuit, and figure 7-10 is the Head Load timing diagram.

7.1.2.4 Motion Check LED

The motion of the Drive is indicated with green and red LEDs (light emitting diodes). The green LED lit indicates that a disk is inserted in the Drive and the control is in the ready condition. In this state, the disk can be ejected from the Drive. The red LED lit indicates that a disk is inserted in the Drive and the Read/Write Heads have been loaded. In this state the disk cannot be ejected.

7.1.2.5 Track 00 Detection

The TRACK 00 signal is provided for correcting the track position of the heads when their position is unknown. Moving the heads to Track 00 causes the TRACK 00 signal to go to logic level low. The Track 00 detector consists of a photo switch comparator and peripheral circuit. The Track 00 Switch is closed by the



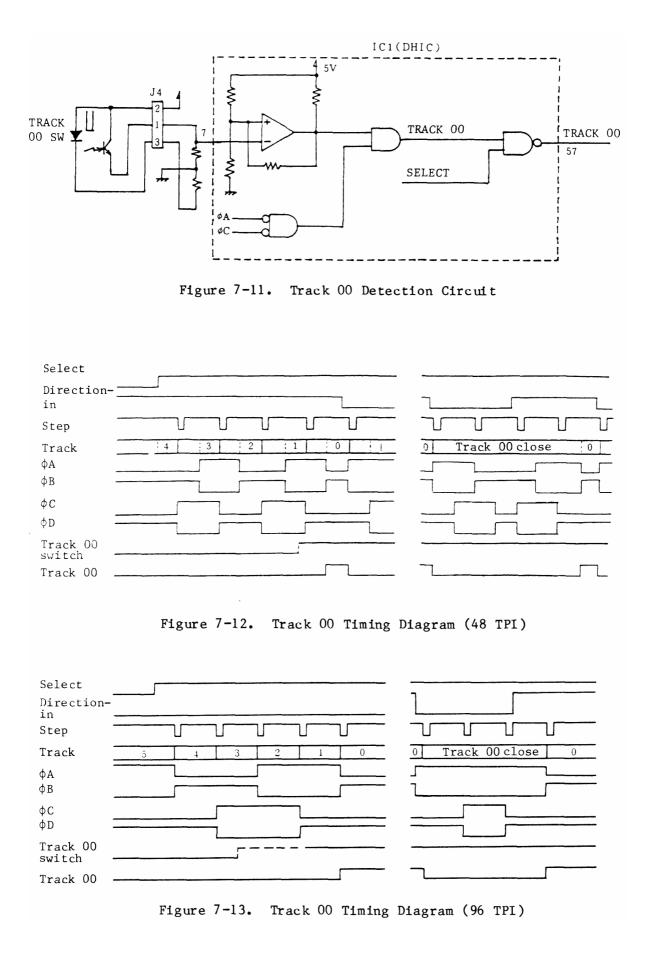
Head Carriage cutting off the light to the photo switch. The TRACK 00 signal is output when the output level of the Track 00 photo switch is the same as the output level of phase A and phase C of the Stepper Motor. Figure 7-11 is a simplified schematic of the Track 00 detection circuit, and figure 7-12 and figure 7-13 are Track 00 timing diagrams.

7.1.2.6 Write Protect Detector

The Write Protect Detector consists of an LED and a photo transistor. For write protect, the disk write protection notch is covered by an opaque cover. Inserting a disk with the covered notch causes the photo transistor output to go to logic level low, because the light from the LED does not reach the photo transistor. In this case, if the Select signal goes to logic level high, the WRITE PROTECT signal goes to logic level low. Thus, the Central Microprocessor Board is notified of the write protect status. Figure 7-14 is a simplified schematic of the Write Protect Detector circuit.

7.1.2.7 Index Detector

The Index Detector consists of an LED, a photo transistor, and a comparator, similar to the Write Protect Detector. When the index hole is positioned between the LED and the photo transistor, the LED light reaches the photo transis-



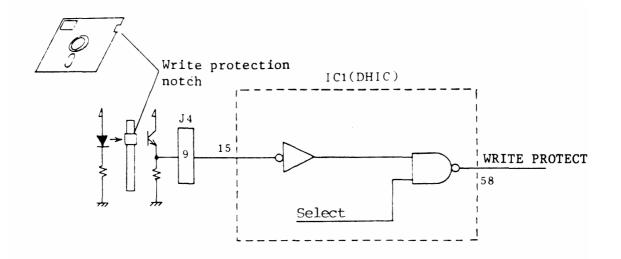
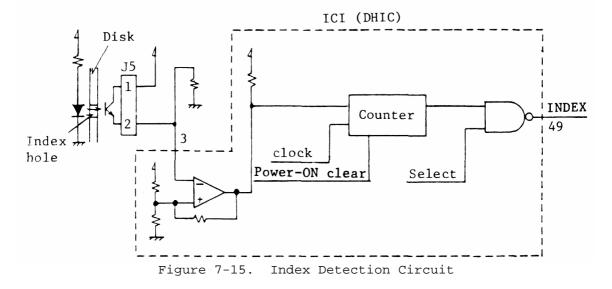


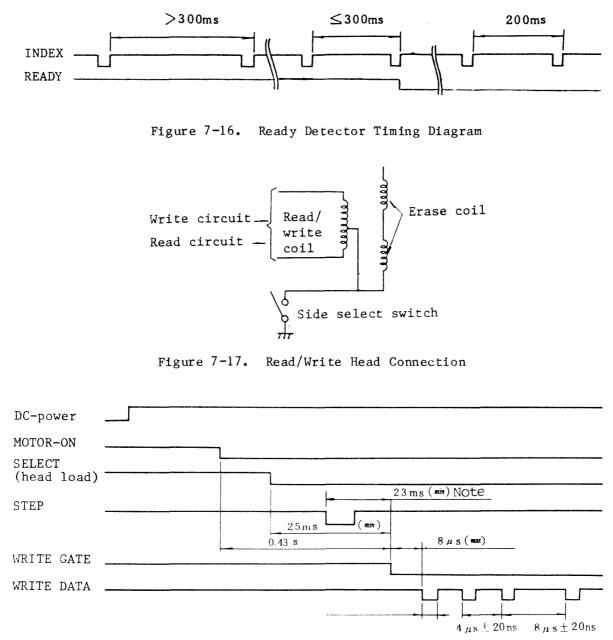
Figure 7-14. Write Protect Detector Circuit

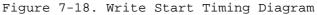


tor, and a negative pulse of 2.5 ms to 5 ms is generated in the comparator output. This pulse enters the counter and, as a 4 ms pulse, is conveyed to the Central Microprocessor Board as a negative pulse when the SELECT signal is active. Figure 7-15 is a simplified schematic of the Index Detection circuit.

7.1.2.8 Ready Detector

The Ready Detector is provided for monitoring the disk speed by the index pulse and is built into IC1. When the index pulse time interval is over 300 ms, the IC1 READY output (pin 61) is at logic level high (inactive). When it is below 300 ms, the READY output goes to logic level low (inactive). Figure 7-16 shows the Ready Detector timing.





7.1.2.9 Read/Write Heads

The Read/Write Head is a tunnel erase ceramic head. The head consists of the read/write coils and the erase coil. The erase coil is excited in the write mode, and a noise prevention area is formed at both sides of a track recorded by the read/write coil. The read/write coils are rolled on the core chip and center tapped. At the write operation time, each bit of write data is alternately distributed to each coil by the D flip-flop. Writing data over the old data causes the old data to be replaced by the new data. At the read time the output voltage is induced when the Read/Write Head gap passes over the magnetized track. Figure 7-17 is a Read/Write Head connection diagram.

7.1.2.10 Write Circuit

The Write Circuit converts the serial data passed from the Central Microprocessor Board into the magnetic pattern on the disk. Figure 7-18 shows the write start timing (96 TPI). Loading the heads and making the WRITE GATE signal logic level low causes the Drive to enter the writable status. Sending data from the Central Microprocessor Board in this state causes the write flip-flop to alternately turn on. Hence, the write current is supplied to the two halves of the read/write coils alternately.

The alternating magnetic field corresponding to the data from the Central Microprocessor Board is stored on the disk. When the erase enable signal is at logic level low, the erase amplifier turns on, and current is supplied to the erase coil. The erase enable signal goes to logic level low after the WRITE GATE signal has gone to logic level low and a fixed delay time has elapsed. Figure 7-19 is a simplified write circuit block diagram, figure 7-20 is the

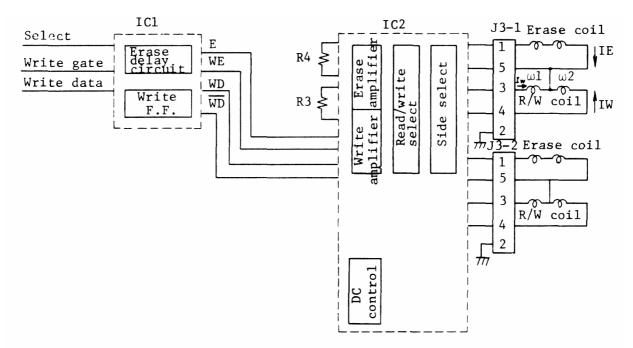
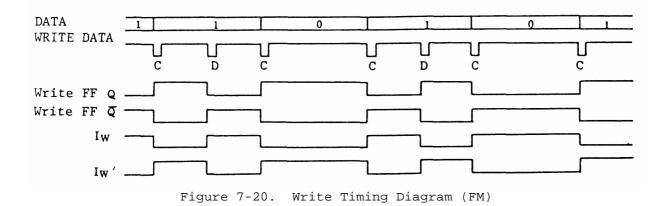


Figure 7-19. Write Circuit Block Diagram



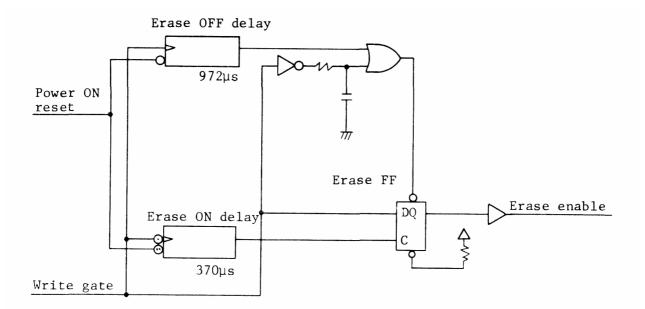


Figure 7-21. Simplified Erase Delay Circuit

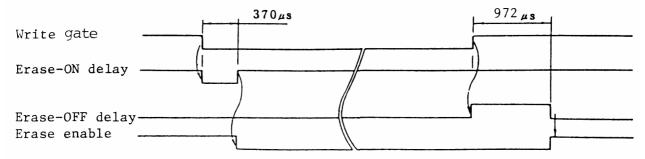


Figure 7-22. Erase Delay Timing Diagram

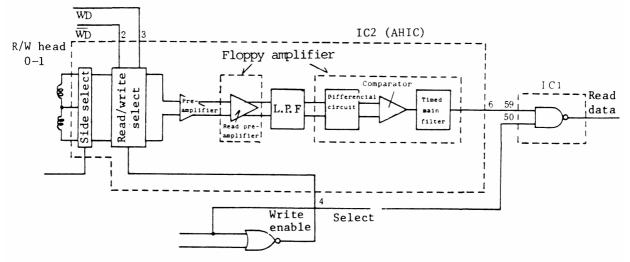
write timing diagram, figure 7-21 shows the erase delay circuit (simplified), and figure 7-22 is the erase delay timing diagram.

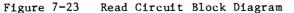
7.1.2.11 Read Circuit

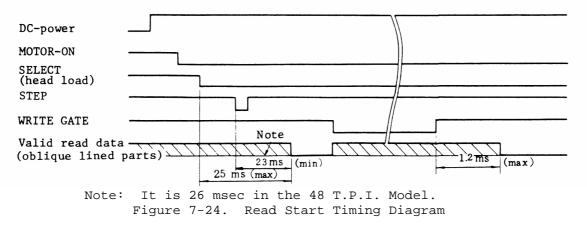
Data stored on the floppy disk are recovered by the Read Circuit. Loading the heads and making the WRITE GATE signal a logic level high causes the Drive to enter the readable status. The Read Circuit consists of an IC floppy amplifier and associated circuitry. Figure 7-23 a simplified block diagram of the Read Circuit, and figure 7-24 is the Read Timing Diagram.

7.1.2.12 Read/Write Select Circuit

The Read/Write Select Circuit consists of a diode switch. The input side of the switch is connected to the coil of the Read/Write Head, and the output side







of the switch is connected to the Read Amplifier Circuit. When the Drive is in the write mode, the WRITE ENABLE signal is at logic level low, and the diodes are turned off. When the Drive is in the read mode, the WRITE ENABLE signal is at logic level high, diodes D9 and D10 are turned on, and the Read/Write Head is connected to the Read Amplifier. Figure 7-25 is a simplifed block diagram of the Read/Write Select Circuit.

7.1.2.13 Read Amplifier Circuit and Filter Network

The read data signal is amplified by the preamplifier and the Floppy Amplifier. The amplified read data signal is delivered through the Filter Network (low pass) to the Active Differential Circuit. Figure 3-26 is a simplified schematic of the Read Amplifier Circuit and Filter Network.

7.1.2.14 Active Differential Circuit and Comparator

The Active Differential Circuit and Comparator are part of the Floppy Amplifier. The Active Differential Circuit is a differential amplifier whose emit-

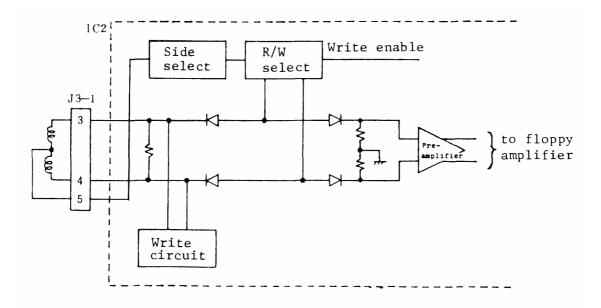


Figure 7-25. Read/Write Select Circuit

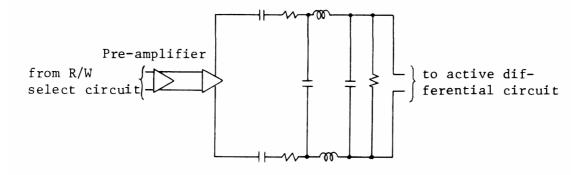


Figure 7-26. Read Amplifier Circuit and Filter Network

ters are coupled through an RLC network. The RLC network differentiates the input signal voltage so that the amplifier output is a differentiated version of the input signal. The output of the differential amplifier is input to the Comparator. The Comparator detects the zero-crossover point of the signal, thereby detecting the peak of the Active Differential Circuit input signal voltage. Figure 7-27 is a simplified schematic.

7.1.2.15 Timed Main Filter and Crossover Detector

The Timed Main Filter and Crossover Detector are part of the IC Floppy Amplifier. The Timed Main Filter removes any erroneous crossovers from the Comparator caused by shouldering of the differentiated read data signal. When a high resolution head is used, shouldering sometimes occurs in the outer circumference of the Drive. The Timed Main Filter consists of a pulse generator, a timed one-shot MV, and a timed main flip-flop. The pulse generator outputs a short pulse to trigger the timed main one-shot at every input transfer. The timed main one-shot pulse width is determined by the external resistance and

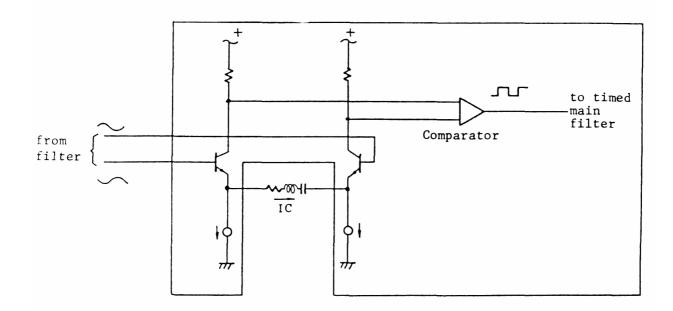


Figure 7-27. Active Differential Circuit and Comparator

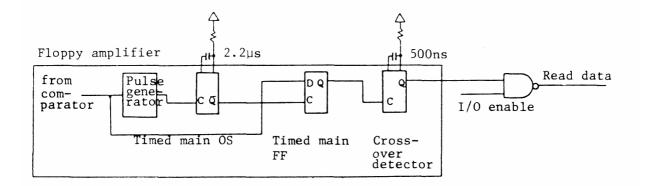
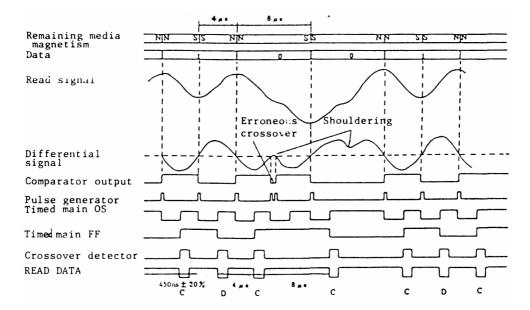
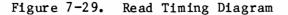


Figure 7-28. Timed Main Filter and Crossover Detector

capacitor value. The data passed from the Comparator is delayed by 2.2 microseconds by the timed main one-shot and loaded on the timed main flop-flop. Even if the timed one-shot is clocked by an erroneous crossover, the timed main flip-flop output does not change, because the erroneous crossover time is shorter than 2.2 microseconds. The Crossover Detector is triggered with every timed main flip-flop transfer. The pulse width of the Crossover Detector is set at 450 nanoseconds.





5V DC < 4.0V 12V DC < 8.3V

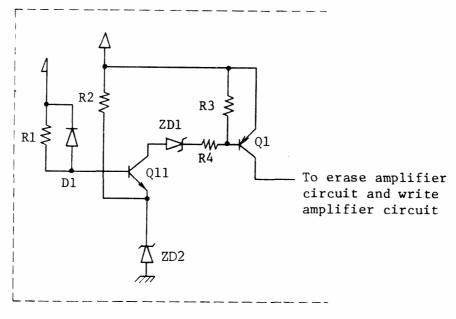


Figure 7-30. DC Control Circuit

Figure 7-28 is a block diagram of the Timed Main Filter and Crossover Detector; figure 7-29 is the read timing diagram.

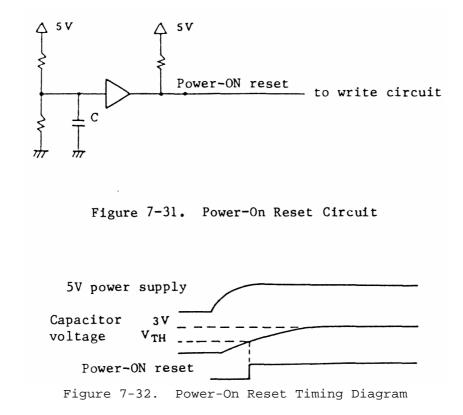
7.1.2.16 DC Control Circuit

The DC Control Circuit is used to monitor the 5VDC and 12VCD Power Supplies. When either supply voltage deviates from the limits listed below, the write current and erase current are turned off. Figure 7-30 is a simplified schematic of the DC Control Circuit.

5 volts +4.0 volts 12 volts +8.3 volts

7.1.2.17 Power-On Reset Circuit

When the power is turned on to the Base Unit, capacitor C (figure7-31) begins charging to 3 volts. When the capacitor voltage is lower than the buffer threshold voltage, the Power-On Reset signal goes to logic level low, and the initial reset pulse is generated. Figure 7-31 is a simplified block diagram of the Power-On Reset Circuit, and figure 7-32 is the Power-On reset timing diagram.



7.1.3 Equipment Specifications

Performance characteristics for the Floppy Disk Drive are listed in table 7-1, on the following page.

	Table 7-1.	Specifications
PARAMETERS		CHARACTERISTICS
Storage Capacity		
Per Diskette		1 MB
Per Track		6.25 KB
Data Transfer Rate (bits per second)		250 к
Average Latency Time		100 ms
Track-to-Track Positioning Time		3 ms
Average Access Time		100 ms
Head Loading Time		25 ms
Head Settling Time		20 ms
Motor Start Time		800 ms
Innermost Circumference Recording Density		5922 BPI
Number of Tracks		160 (both sides)
Track Density		96 TPI
Track Radius		
Outer Circumference		57.15 mm
Inner Circumference		34.13 mm
Modulation System		BM or MFM
Ambient Operating Temperature		5°C to 45°C
Ambient Temperature in Transportation		-40°C to 62°C
Non-Operating Temperature		-22°C to 55°C
Relative Humidity		20% to 80% RH
Maximum Wet Bulb		29°C

Table 7-1.	Specifications (continued)
PARAMETERS	CHARACTERISTICS
Error Rates	
The following error rates are valid only when the drive is being used accord- ing to specifications. Media defects or equipment failures are excluded. Written data should be veri- fied as being correctly written. All media defects should be flagged.	
Seek errors	1 in 1,000,000 seeks
Recoverable read errors	1 in 1,000,000,000 bits
Nonrecoverable read errors	1 in 1,000,000,000,000 bits
Resistance Against Vibration in Operation	
Acceleration	1G
Vibration Sweep	5 to 100 Hz
Vibration Direction	X,Y,Z directions
Resistance Against Vibration in Transportation	
Acceleration	3G
Vibration Sweep	5 to 100 Hz
Vibration Direction	X,Y,Z directions
Resistance Against Impulse in Transportation	Will satisfy all specifica- tions after being dropped from height of 100 cm in packed condition
Dimensions	
Width	150.0 mm
Height	33.5 mm
Depth	221.5 mm
Weight	1.2 kg

7.2 INSTALLATION AND MAINTENANCE

This subsection contains unpacking, installation and maintenance information for the Floppy Disk Drive.

7. 2.1 Unpacking

Prior to unpacking the Drive, inspect the packaged Drive to determine Aether any damage was incurred during shipment.

- 1. Using shipping documents, verify that all items have been received.
- 2. Open the protective shipping carton at the top.
- 3. Remove the Drive from the shipping carton.
- 4. Remove the plastic cover.
- 5. Inspect each package article to determine whether any damage was incurred during shipment.
- 6. Verify that connectors, indicators and protruding parts have not been damaged.
- 7. Check the ID nameplate against the shipping papers to verify that the drive part number and serial number are correct.
- 8. When practical, store shipping containers for reuse.
- 9. Record any damage, and report damage to the applicable carrier.

7.2.2 Equipment Placement

Equipment placement consists of mounting the Drive in the Base Unit and routing the input/output cables.

7.2.3 Electrical Installation

Electrical installation of the Floppy Disk Drive system consists of routing the Drive interface (ribbon) cable to the Central Microprocessor Board (CMB), in the Base Unit, and connecting it, and routing the 4-wire power cable to the Base Unit Power Supply and connecting it. Detailed installation procedures are included in Section II of this manual.

7.2.4 Adjustment Procedures

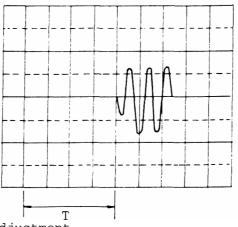
Alignment and adjustment instructions for the Floppy Disk Drive are presented in the following paragraphs and are listed below.

- 1. Index burst position adjustment
- 2. Track position adjustment

- 3. Track 00 position adjustment
- 4. Rotation adjustment
- 5. 0-1 head gap adjustment
- 7.2.4.1 Index Burst Position Adjustment
 - a. Load the alignment diskette, and step it to track 34.
 - b. Set an an oscilloscope as follows:

Channel 1	200 mV AC
Channel 2	200 mV AC (inverted)
Mode	ADD
Time Base	50 microseconds
Trigger	EXTERNAL, NORMAL, NEGATIVE

- c. Connect the Channel 1 test probe to the Drive test point labeled CHK1; connect the Channel 2 test probe to the Drive test point labeled CHK2; connect the Trigger input to pin 49 of IC1, on the Main PCBA.
- d. Check that the start of the index burst is observed 200 microseconds from the beginning of the sweep, as shown below. Adjust side 0 first, then side 1. If necessary, adjust the phototransistor holder assembly. For both sides, time T should be 200+80 microseconds.

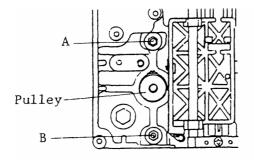


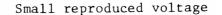
- 7.2.4.2 Track Position Adjustment
 - a. Loosen the Stepper Motor mounting nuts (A, B in illustration below).
 - b. Insert the alignment diskette, and step it to track 16.
 - c. Set an an oscilloscope as follows:

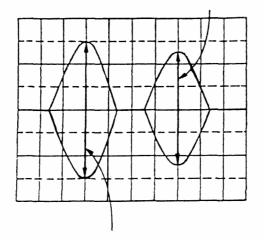
Channel	1	200	mV	AC	
Channel	2	200	mV	AC	(inverted)

Mode	ADD
Time Base	20 milliseconds
Trigger	EXTERNAL, NORMAL, NEGATIVE

- d. Connect the Channel 1 test probe to the Drive test point labeled CHK1; connect the Channel 2 test probe to the Drive test point labeled CHK2; connect the Trigger input to pin 49 of IC1, on the Main PCBA.
- e. Select sides 0 and 1 alternately and monitor the waveforms on both sides while moving the Stepper Motor to put the amplitude ratios (small waveform divided by large waveform) within the range prescribed by the label on the alignment diskette.
- f. Step the heads from track 15 to 16 and from track 17 to 16 to check that the amplitudes remain within the range prescribed by the label on the alignment diskette.







Large reproduced voltage

- 7.2.4.3 Track 00 Position Adjustment
 - a. Load a normal diskette into the Drive.
 - b. Set an an oscilloscope as follows:

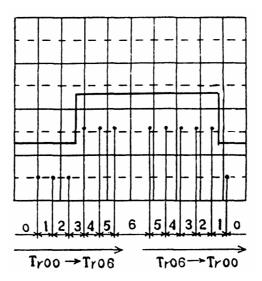
Channel 1	5V DC				
Channel 2	2V DC (inverted)				
Mode	ADD				
Time Base	5 milliseconds				
Trigger	INTERNAL (CH. 2), NORMAL, NEGATIVE				

- c. Connect the Channel 1 test probe to pin 54 of IC1, on the Main PCBA; connect the Channel 2 test probe to the Drive test point labeled CHK3.
- d. Step the head between track 00 and 06 alternately.
- e. Check the switching as follows (see the waveform below):

Track 01 in the direction from track 00 to track 06

Track 00 in the direction from track 06 to track 00

If necessary, loosen the screw mounting the track OO switch $\ensuremath{\mathsf{PCBA}}$ and adjust.



7.2.4.4 Rotation Adjustment

- a. After running the heads for 10 minutes, load a normal diskette.
- b. Connect a frequency counter to the INDEX terminal of the exerciser.
- c. Adjust VRl of the Drive Motor PCBA so that the period of the index is 200+1 ms in tracks 00 and 39.

7.2.4.5 0-1 Head Gap Adjustment

- Adjust the position of the Head Load Arm so that the gap between side 0 and side 1 becomes 0.6+0.2 mm when the Arm is clamped without the diskette in the Drive.
- b. Mount the Head Load Arm so that it is parallel to the Arm portion of the Main Arm.

7.3 REFERENCE INFORMATION

This subsection provides schematics and other reference data for the Floppy Disk Drive.

7.3.1 Interface

The Floppy Disk Drive interface consists of two sections:

- 1. Signal
- 2. Power Supply

Each line is detailed below.

7.3.1.1 Signal Interface

SIGNAL CONNECTOR

The daisy chain or radial chain is used for the signal interface of the Select line, allowing connection to a maximum of four Drives. In the case of the daisy chain, only the last Drive is terminated. A resistance array close to connector J2 is provided for this termination. (The resistance array is removable.)

The alignment of the interface connector and of the power connector is shown below.

Ground Return	Signal Pin	Signal Name	Ground Return	Signal Pin	Signal Name
1	2		19	20	Step
3	4	Head Load	21	22	Write Data
5	6	Select 4	23	24	Write Gate
7	8	Index	25	26	Track 00
9	10	Select 1	27	28	Write Protect
11	12	Select 2	29	30	Read Data
13	14	Select 3	31	32	Side Select
15	16	Motor-On	33	34	Ready
17	18	Direction-In			

POWER SUPPLY CONNECTOR

Pin No.	Power Name
1	+12VDC
2	+12V GND
3	+5V GND
4	+5VDC

The signal interface lines are illustrated in figure 7-33, on the next page.

7.3.1.2 Input Lines

<u>SELECT 1-4</u> - A maximum of four Drives can be connected in the daisy chain mode. A jumper is used to switch each Drive. (All Drives are set to select 1 at the factory.) Select lines 1-4 are used to select the ranked Drive. Only the selected Drive can send and receive signals.

 $\underline{\text{MOTOR-ON}}$ - This signal is a Spindle Motor ON/OFF signal; the motor is turned ON at logic level 0.

<u>DIRECTION-IN</u> - The function of this signal is to determine the direction of the read/write heads and must be set at least 1 microsecond earlier than the STEP pulse leading edge. The direction of the head carriage by the DIRECTION-IN signal is handled as follows:

```
Logic level 1 Away from the center of the disk
```

```
Logic level 0 Toward the center of the disk
```

 $\underline{\text{STEP}}$ - Sending the logic level 0 pulse to this line causes the read/write heads to move in the direction determined by the DIRECTION-IN signal. In usual cases, this step speed is 3 ms/track. When the WRITE GATE signal is at logic level 0, the STEP signal is inhibited. See the timing chart in figure 7-xx.

<u>WRITE GATE</u> - This is a signal to control the write data and read data. The write data are valid at logic level 0, and the read data are valid at logic level 1. In the case of a write-protected disk, the write function is inhibited within the Drive. Another function of the WRITE GATE is to internally operate the tunnel erase, which keeps operating for 972 microseconds after the WRITE GATE has been closed.

 $\frac{\text{WRITE DATA}}{\text{Power is line is used to write data onto the disk. Power is supplied to the read/write heads when logic level 1 changes to logic level 0, which causes a magnetic flux. This line is valid when the WRITE GATE is at logic level 0. A WRITE DATA timing chart is shown in figure 7-34.}$

<u>HEAD LOAD</u> - When this line becomes logic level 0,the heads are loaded and are released at logic level 1. Depending on the jumper selection, both the HEAD LOAD and SELECT are available, or the heads can be loaded by SELECT only. In every case, the heads are loaded only when the READY sig-

HOST SYSTEM		MINI	DISK	DRIVE	2
	RESERVED	2	1		
	HEAD LOAD	4	3		
	SELECT 4	6	5		
	INDEX	8	7		
	SELECT 1	10	9		
	SELECT 2	12	11		
	SELECT 3	14	13		
	MOTOR ON	16	15		
	DIRECTION IN	18	17		J
	STEP	20	19		Ū
	WRITE DATA	22	21		
	WRITE GATE	24	23		
	TRACK 00	26	25		
	WRITE PROTECT	28	27		
	READ DATA	30	29		
	SIDE SELECT	32	31		
	READY	34	33		
			J 2		
	+ 5 V DC	4 5 V	GND	3	
	+ 1 2 V DC	1 12 V	GND	2	
		100 K		=0.1 # F	

1

Figure 7-33. Signal Interface Lines

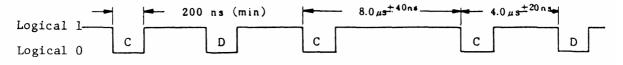


Figure 7-34. WRITE DATA Timing (FM)

nal is at logic level 0. The function of this signal is to control the operation confirmation LED.

<u>SIDE SELECT</u> - The function of this signal is to select the two read/write heads. Logic level 0 selects the 1 side and logic level 1 selects the 0 side. When the heads are switched, a 200-microsecond wait period is required at read time, and a 1200-microsecond wait period is required at write time.

7.3.1.3 Output Lines

 $\underline{\text{READY}}$ - This signal is issued when the disk is inserted into the Drive and is at logic level 0 during the normal select time. Otherwise it is at logic level 1.

<u>TRACK 00</u> - This signal goes to logic level 0 when the read/write heads are positioned at track 00 and is used to detect the Head Carriage position after POWER-ON.

 $\underline{\text{INDEX}}$ - The Drive carries the index detection mechanism and issues the detection signal when the index hole is detected. Normally this line is at logic level 1 and becomes logic level 0 when the index hole is detected (4 ms). On the soft sector disk, a signal at one hole indicates the start of the track. When the disk is not inserted, the index signal remains at logic level 0. Figure 7-35 shows the index timing.

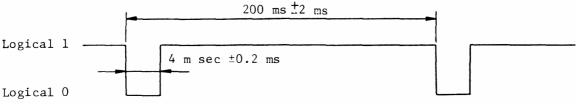
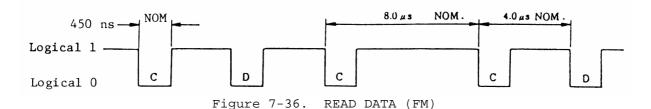


Figure 7-35. Index Timing

BFISD 8079

<u>READ DATA</u> - The function of this signal is to output the raw data that was read by the read circuit of the Drive. Usually this line is at logic level 1 and becomes logic level 0 when the magnetic inversion exists on the track.



<u>WRITE PROTECT</u> - The function of the signal is to notify the Central Microprocessor Board that a write-protected disk has been inserted. When the protected disk is inserted, the line becomes logic level 0, and the write onto the disk is inhibited in the Drive. For write protect, the disk write prevention notch can be covered by an opaque label.

7.3.2 Jumper Pin

Selecting a jumper pin located on the Main PCBA permits a desired function to be used. Head load, the operation confirmation LED and the door lock solenoid can be controlled by jumper pins. A jumper pin selection tabel is presented below. The factory jumper arrangement is shown on the following page.

Function	Content	JJ1					
		<u>S1</u>	<u>s2</u>	<u>S3</u>	<u>S4</u>	SH	AH
	Jumper mode at factory before shipment	0	Х	Х	X	0	Х
Drive Select	Drive Select 1 " 2 " 3 " 4	0 X X X	X O X X	X X O X			
Head Load	Head loading takes place under head loading signal					0	х
Selection	Head loading takes place by ready mode automatically					Х	0

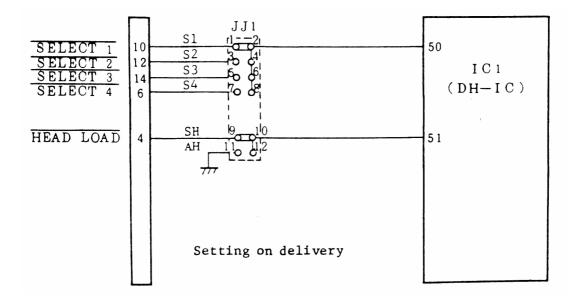
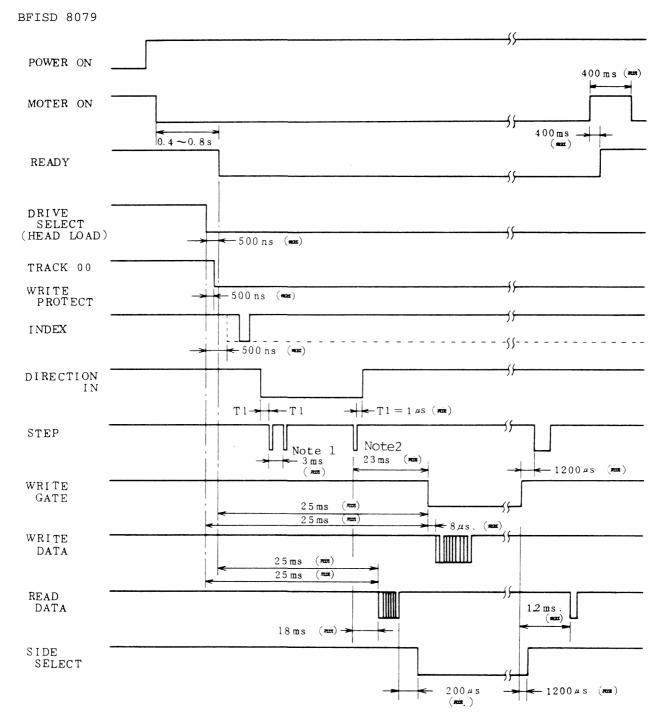
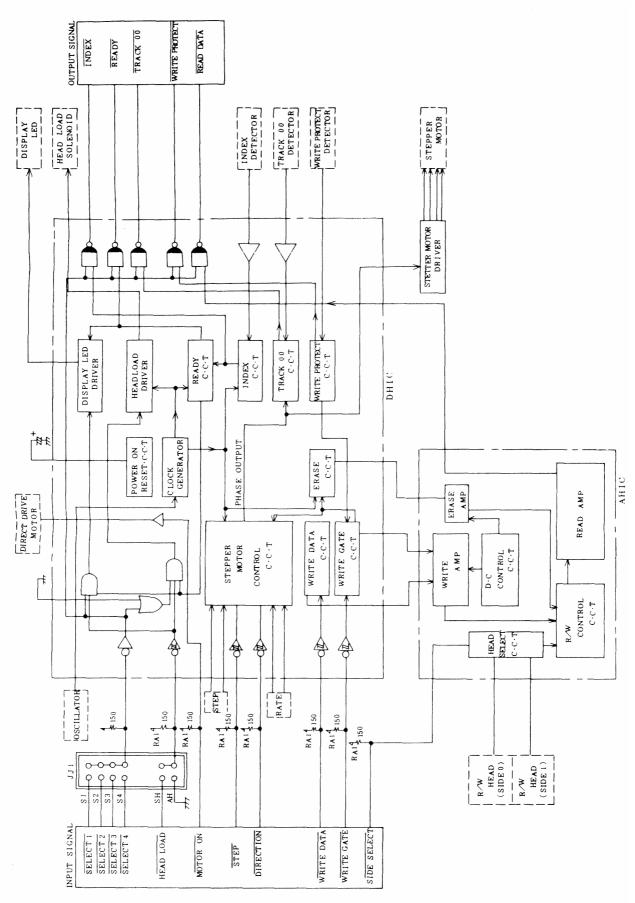


Figure 7-37. Factory Arrangement of Jumper

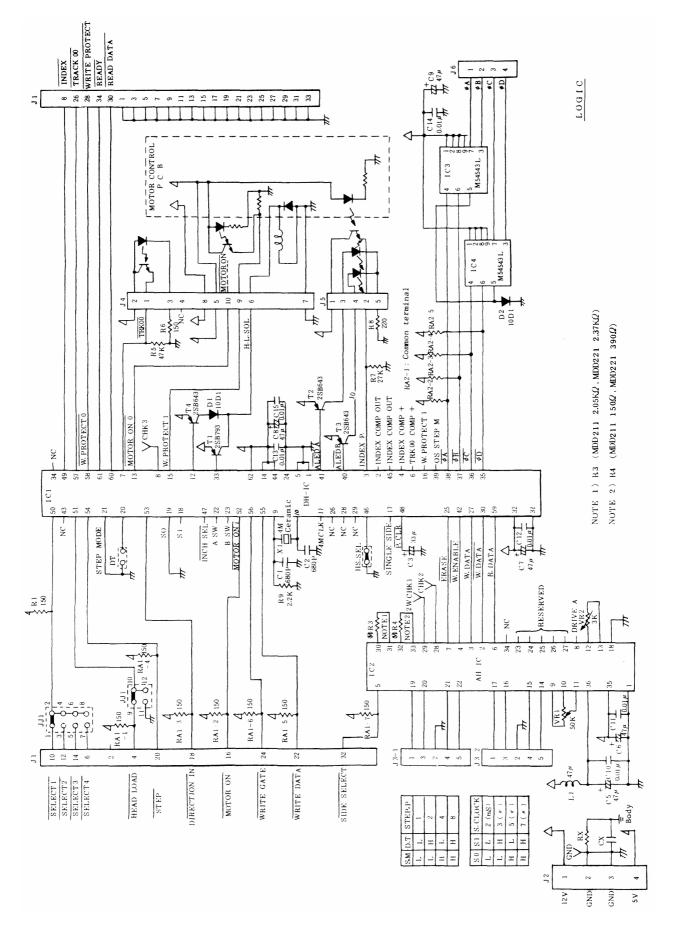


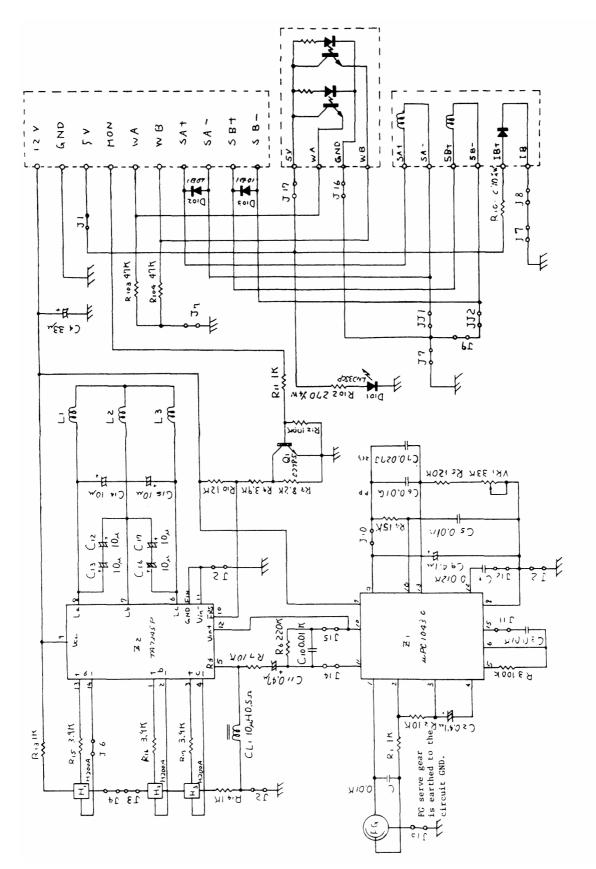
Note 1: In 48 T.P.I Model, the period is 6 ms. Note 2: In 48 T.P.I Model, the period is 26 ms.

Figure 7-38. Drive Timing Diagram



7-31







BFISD 8079

SECTION VIII

20 MEGABYTE WINCHESTER DRIVE SYSTEM

8.1 INTRODUCTION

This section provides maintenance personnel with information necessary to install, operate and maintain the 20 MB Winchester Drive system. Section VIII is arranged in six subsections. The scope of each subsection is as follows:

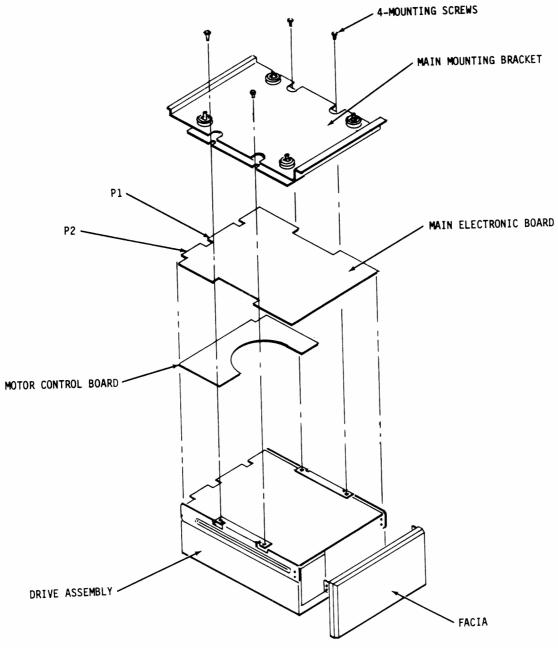
- 8.1 INTRODUCTION contains general information, physical and electrical descriptions and equipment specifications.
- 8.2 INSTALLATION AND OPERATION contains information to enable maintenance personnel to inspect and install the 20 MB Winchester Drive and includes information on the Winchester Drive Controller (WDC).
- 8.3 FUNCTIONAL DESCRIPTION explains Drive and Controller operation and gives a detailed description of each function. Simplified logic and block diagrams, timing diagrams and waveforms are included.
- 8.4 MAINTENANCE contains corrective maintenance procedures.
- 8.5 REMOVAL AND REPLACEMENT PROCEDURES presents step-by-step procedures for removing and replacing major subassemblies.
- 8.6 PARTS LIST

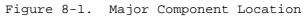
8.1.1 General Description

The 20 MB, 5 1/4-inch, Winchester Drive is a fixed-media, magnetic, rotating, data storage device. Its purpose is to allow the Model 4108 Base Unit to store and retrieve blocks of data (records) onto and from rotating disks, thus providing storage for the MAI® 2000 Series Computer System. The Drive functions as an input/output device in the Base Unit. The Drive contains four magnetic disks and has a total data storage capability of 20.97 megabytes, formatted.

Access to data is provided by one moving head per disk surface. The heads are an integral part of the Head Disk Assembly (HDA) and never require alignment in the field. Data is recorded on the disk surfaces using modified frequency modulation (MFM) techniques. The Drive incorporates an open-loop, stepper motor positioning system. The major components of the Drive are illustrated in figure 8-1 and are explained in the following paragraphs.

<u>Head Disk Assembly</u> - The Head Disk Assembly, shown in figure 8-2, is a completely sealed module that houses the read/write heads, disks, positioner assembly, stepper motor and filters. The spindle-mounted disks are rotated by the dc motor as the read/write heads "fly" over the surface of the disk. The stepper motor positions the heads over the disk, using positioning information from a single-chip microcomputer. Within the sealed module, air movement generated by disk rotation causes air to flow from the disk chamber (upper chamber), through an aperture, into the drive chamber (lower chamber) and return via a recirculating filter.





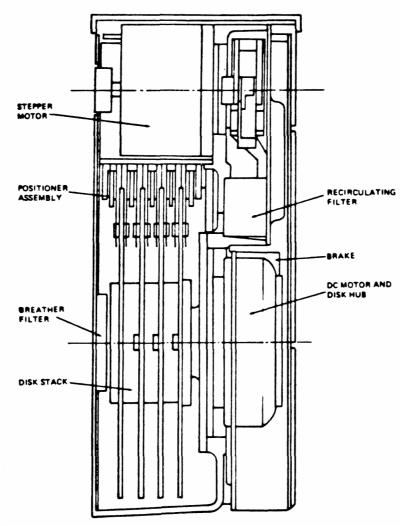


Figure 8-2. Head Disk Assembly

DC Motor and Brake - The dc motor is a brushless, two-phase external rotor motor with integral hub. Commutation is effected by a Hall sensor. The rotational speed of the motor is 3600 revolutions per minute (rpm). The disk hub is grounded to the Master Electronics PCBA via the motor shaft and a button contact. The brake is a plunger-solenoid designed to stop the motor in five seconds and to provide a restraining torque during handling.

Disk Electronics - The disk electronics consists of three standard printed circuit board assemblies (PCBAs): the Master Electronics PCBA; the Preamplifier PCBA; and the Motor Control PCBA.

Power Supply - The dc supply voltages (+12 and +5 volts) to the Winchester Drive are supplied by the Base Unit Power Supply and are input to the Drive on connector J3.

8.1.2 Functional Concepts

The simplified block diagram in figure 8-3 shows the functional concepts of the Winchester Drive. Additional detailed explanations of the logic areas are discussed in paragraph 8.3.

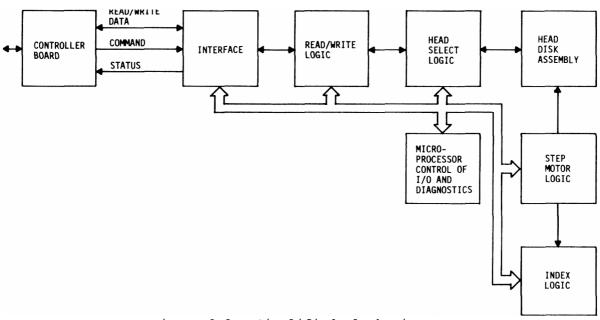


Figure 8-3. Simplified Block Diagram

<u>Interface logic</u> - The interface logic translates the input/output signals of the Winchester Drive to ensure drive-to-controller signal compatibility. Winchester Drive logic signal levels are transistor-totransistor logic (TTL) compatible. The transmission line signals are differential signals.

<u>Read/Write Logic</u> - To execute read or write commands, the Drive must be free of faults, and the selected head must be at the correct location on the disk (i.e., on cylinder). During a read command, the read/write logic recovers data from the disk, processes the data, and transfers the data to the Winchester Drive Controller (WDC) board, in the Base Unit. During a write command, the read/write logic receives data from the WDC, processes the data and writes it onto a disk.

 $\underline{\text{Head Select Logic}}$ - The head select logic receives and decodes the addresses of a specific head.

<u>Stepper Motor Logic</u> - A four-phase stepper motor is used to control the read/write heads in the proper sequence at a rate and direction determined by a single-chip microcomputer.

<u>Index Logic</u> - The square wave output of the Hall sensor in the dc motor is processed to produce a pulse every disk revolution. This pulse is used as an interface signal to mark a fixed reference point relative to the disk.

<u>Winchester Drive Controller</u> - The Winchester Drive Controller PCBA uses the Shugart Associates System Interface (SASI). It communicates with the Central Microprocessor Board (CMB) global bus via the WDC Bus Adapter PCBA. Together, these two boards interface the Winchester Drive to the CMB. The Winchester Drive Controller PCBA is mounted above the component side of the WDC Bus Adapter PCBA.

8.1.3 Equipment Specifications

Performance characteristics for the 20 MB Winchester Drive are listed in table 8-1.

Table 8-1. Specifications

PARAMETERS

CHARACTERISTICS

Storage Capacity Unformatted	
Disks per drive	4
Cylinders	320
Tracks per cylinder	8
Data bytes per track	10,417
Tracks per drive	2,560
Capacity (megabytes)	26.67

Table 8-1. Specifications (continued) PARAMETERS CHARACTERISTICS Storage Capacity Formatted 256 Data bytes per sector 32 Data sectors per track 8,192 Data bytes per track 20.97 Capacity (megabytes) Recording Parameters Bit density 8,900 bpi (inner track, nominal) Coding Modified-frequency-modulation (MFM) 360 tracks per inch (average) Track density Rotational Parameters Disk rotational speed 3,600 (+1%) rpm Data transfer rate 5 megabits per second Cylinder Access Time Ramp mode Single cylinder 18 milliseconds (average) 320 cylinders 215 milliseconds (maximum) Cylinder access 90 milliseconds (average) 3 ms step mode Single cylinder 18 milliseconds (average) 320 cylinders 1,035 milliseconds (maximum) 360 milliseconds (average) Cylinder access Slow pulse mode Single cylinder 23 milliseconds (average) 320 cylinders Step rate=pulse rate Step rate=pulse rate (average) Cylinder access Data Access Time Average latency 8.3 milliseconds Average data access time/ramp mode 98.3 milliseconds time/3 ms step mode 368.3 milliseconds Head switching time 8 microseconds (maximum) Error Rates The following error rates are valid only when the drive is being used according to specifications. Media defects or equipment failures are excluded. Written data should be verified as being correctly written. Seek errors 1 in 1,000,000 seeks Recoverable read errors 1 in 10,000,000,000 bits 1 in 1,000,000,000,000 bits Nonrecoverable read errors

Table 8-1. Specifications (continued)

PARAMETERS	CHARACTER	ISTICS
STORAGE	TRANSIT	OPERATING
Temperature:		
-40°F to 158°F -40°C to 70°C	-40°F to 158°F -40°C to 70°C	50°F to 122°F 10°C to 50°C
Temperature Gradient:		
27°F per hour 15°C per hour	20°F per hour 15°C per hour	18°F per hour 10°C per hour
Humidity:		
5-90% RH no condensation	5-90% RH no condensation	10-85% RH no condensation
Humidity Gradient:		
20% per hour	20% per hour	20% per hour
<u>Altitude</u> :		
-1,000 to 40,000 feet	0 to 40,000 feet	-1,000 to 10,000 feet
Vibration:		
0.2 inches peak-peak displacement (5 Hz to 20 Hz)	0.2 inches peak- peak displacement (5 Hz to 20 Hz)	0.006 inches peak- peak displacement (5 Hz to 60 Hz)
Shock:		
Will withstand a drop of 36 inches	Will withstand a drop of 36 inches	3.0 g, peak; 10 milli- seconds duration; 2 shocks/second, maximum
<u>RF Interference</u> :		1 volt/meter rms (1.5 HZ to 10GHz)
Magnetic field:		0.0003 tesla, max.
Emitted Acoustic Noise:		54 db, max. (cont.)

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8.2 INSTALLATION AND OPERATION

This subsection contains unpacking, installation and checkout information for the 20 MB Winchester Drive System.

8.2.1 Unpacking

Prior to unpacking the Drive, inspect the packaged Drive to determine whether any damage was incurred during shipment.

- Using the shipping documents, verify that all items have been received.
- 2. Open the protective shipping carton at the top.
- 3. Remove the Drive from the shipping carton.
- 4. Remove the plastic cover.
- 5. Inspect each package article to determine whether any damage was incurred during shipment.
- 6. Verify that connectors, indicators and protruding parts are undamaged.
- 7. Check the ID nameplate against the shipping papers to verify that the drive part number and serial number are correct.
- 8. When practical, store shipping containers for reuse.
- 9. Record any damage, and report damage to the applicable carrier.

8.2.2 Equipment Placement

Equipment placement consists of mounting the Drive in the Base Unit, installing the Winchester Drive Controller, and routing the input/output and power cables.

8.2.3 Shipping Lock (Read/Write Heads)

The stepper motor lock is fixed in place automatically through a relay. The lock prevents movement of the read/write heads across the disk surface during shipment or other movement.

8.2.4 Step Rate Selection

The Winchester Drive has a step rate operational range of 10 microseconds to 8 milliseconds. This operational range has three bands; two ranges are automatically selected by the single-chip microcomputer, and one is selected by removing Link A on the Master Electronics PCBA.

Link A in: step rate is 10 microseconds to 200 microseconds Link B in: step rate is 700 microseconds to 3.1 milliseconds Link A out: step rate is 3.1 milliseconds to 8.0 milliseconds

8.2.5 System Installation

Installation of the Winchester Drive system consists of plugging the WDC PCBA/ WDC Bus Adapter PCBA combination into the Central Microprocessor Board, in the Base Unit, and then routing the Winchester Drive cables to the WDC and the power supply and connecting them. All components required to interface the 20 MB Winchester Drive to the Central Microprocessor Board are included. Detailed installation procedures are provided in Section II of this manual.

8.2.6 Operation

Operating instructions consist of indicator functions, power-on/off procedures and voltage checks.

Indicators - When lit, the two red LEDs fixed to the Master Electronics PCBA are visible through the facia. The Power On LED is located closest to the center of the facia and is used to indicate fault conditions (refer to table 8-3).

The Power On LED will not come on, indicating an error, if the +5 volt supply does not come up and stabilize within one second.

The Select On LED comes on (provided the Power On LED is on) when the Drive is ready and selected by the Base Unit.

Power-On Procedures - The Drive requires +12 volts and +5 volts dc source power, and these voltages are measured at Drive connector J3. At poweron, the Drive motor takes 4 amperes at +12 volts, dropping to 2.4 amperes (maximum) after 10 seconds. For power-up or power-down sequences, the +12 and +5 volt supplies may be applied or removed in any order. However, if the +5 volt power is applied first, the +12 volts should follow within 5 seconds, or the fault detection circuitry will issue an error indication.

On power-up the Drive performs an automatic recalibration sequence, which includes a disk speed check, accurate to $\pm 1\%$ of nominal; a seek to track 00; and an index pulse selection. The Central Microprocessor Board uses status READY to sense the completion of this sequence. The time until READY turns true is 18 seconds, maximum.

Power Supply Checks - The following loads are used to check the power supplies. For the 12 volt supply, the power-up current is measured using a standard load of 3 ohms in parallel with 1 millihenry, and the operating current is measured using 5 ohms in parallel with 1 millihenry. With a 7 ohm resistive load on the 5 volt supply, and the aforementioned loads on the 12 volt supply, noise and ripple should be no more than 100 millivolts peak-to-peak, up to 500 Hz; and 50 millivolts peak-to-peak, from 500 Hz to 5MHz. The power requirements of the Drive are listed in table 8-2.

Table 8-2. Power Requirements

VOLTAGE (VDC)	TOLERANCE	NOMINAL CURRENT	MAXIMUM CURRENT
+5	<u>+</u> 5%	0.65A	0.75A
+12	<u>+</u> 10%	2.0A	2.4A

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	Table 8-3. Diagnosti	c and Failure Code Indicators
ACTION	ABNORMAL RESULT (DOT-DASH CODE)	RESULT
Power-Up		LED flashes at 0.5 second intervals
Drive		After 25 seconds maximum, the LED stops flashing and remains on. Heads are at track 000
Code 1	LED displays*	No index track data burst at track 2 or track 3
Code 2	LED displays	No flag 0 from track 000 detector
Code 3	LED displays	Motor speed exceeds +_!% tolerance during normal operation
Code 4	LED displays	Motor speed exceeds +10%, -5% toler- ance during normal operation
Code 5	LED displays	Flag 0 always true
Code 6	LED displays	Step pulse while Write Gate true
Code 7	LED displays	Static write fault condition**
Code 8	LED displays N/A	
Code 9	LED displays	Microcomputer self-test failed
Code 10	LED displays	No index
Code 11	LED displays LED remains off LED remains on LED flashes (erratic)	Motor not up to speed Firmware/microcomputer fault Firmware/microcomputer fault Firmware/microcomputer fault
Code 12	LED displays	Found index track data burst, but cannot set index

*For the fault codes, a four-bit binary code is used. Long flash (-) = logic 1; a short flash (.) = logic 0, with the most significant bit (MSB) occuring first.

**Write Fault conditions:

- 1. Write current and no Write Gate
- 2. No write current and Write Gate
- 3. More than one read/write head selected
- 4. 12 volt supply drops below 10.3 volts
- 5. 5 volt supply drops below 4.5 volts

8.3 FUNCTIONAL DESCRIPTION

The following paragraphs describe the theory of the various electronic subsystems that comprise the 20 megabyte 5.25" Winchester Drive. This information provides maintenance personnel with a comprehensive understanding of the functions of the Drive. A brief discussion of disk recording principles is followed by a functional description of the Winchester Drive unit, explaining how the Drive interfaces with the Winchester Drive Controller.

The interconnection of the logics is shown in the detailed diagram, figure 8-4.

8.3.1 Basic Disk Principles

The recording medium for the Drive is a stack of four 5 1/4-inch disks with eight recording surfaces (see figure 8-5).

Each disk is coated with a layer of magnetic oxide. The coating is burnished to a flatness that allows the read/write heads to "fly" in proximity to the surface without actual physical contact.

Data is recorded in serial fashion on concentric rings on each disk surface by holding the head in a fixed position over the rotating disk. (These rings are referred to as "tracks." The disk drive unit positions the heads precisely over the tracks. Corresponding track positions, both upper and lower on each disk, are referred to as one "cylinder" of data.)

A center-tapped coil is mounted on the core of the read/write head to perform the read/write function. The recording flux direction is controlled by energizing the center tap connection, causing current to flow through the bifiler winding from the center tap to either one end or the other. When reading, the ends of the coil are switched to the input of the read amplifier. Data is erased by writing new data on the track. The read/write coil is mounted onto the core of the ferrite slider.

As the disk rotates, it creates an "air bearing" around its surface. This air bearing moves under the slider and exerts an upward force on the shoe. A downward pressure is placed on the slider by the spring flexure of the head. Supported by carefully balanced aerodynamic forces, the head shoe then flies at a point where the downward force of the load spring is equal in force to the air pressure under the head. The slider's flying height is influenced, in part, by the air-bleed channel in the middle of the slider. This channel allows some air to bleed from under the slider, decreasing the air pressure.

This, in turn, allows the head to fly closer to the disk surface. The average flying height of the head is 19 microinches. (The head is closer on an inner track because the inner track portion of the disk is moving at a slower speed than the outer track portion of the disk, resulting in less air pressure on the inner track than on the outer track.)

The slider is mounted to the head arm assembly via a spring gimbal-mount. This allows the flying attitude of the slider to vary slightly so that it can follow minor surface variations without contacting the disk surface. As the disk starts, or stops, the head takes off from, or lands in, a silicone-lubricated landing area. When the disk is not spinning, the head rests on, and actually contacts, the landing zone on the disk.

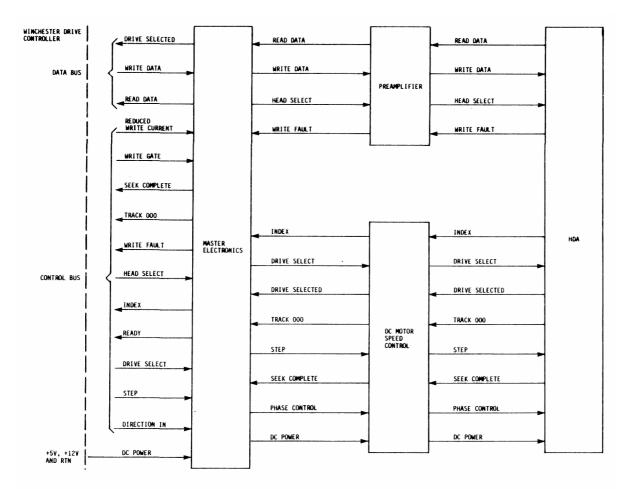


Figure 8-4. Winchester Drive Block Diagram

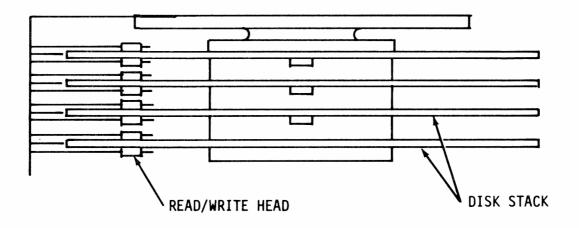


Figure 8-5. Surface and Head Geometry

All heads are mounted on a carriage such that the heads and carriage move as one unit. The carriage moves the heads radially over the disks' surfaces. All the heads are positioned at the same cylinder at any given time.

8.3.2 Control Lines

The control data is exchanged between the Winchester Drive and the Winchester Drive Controller board (WDC), in the Base Unit, via a control cable. The following paragraphs define the control interface signals.

<u>Reduced Write Current</u> - The Reduced Write Current signal from the WDC enables a current sink during a write , diverting current from the head and effectively reducing the write current.

 $\underline{\text{Write Gate}}$ - When true, the Write Gate signal from the WDC enables the current source and Write drive signals. When false, this signal enables Read Data to be transferred from the drive to the WDC.

<u>Seek Complete</u> - The Seek Complete status signal is generated by the single-chip microcomputer in the Master Electronics PCBA when the value of an internal 8-bit counter equals the desired stepper motor phase changes (determined by the Step and Direction In input signals).

 $\underline{\mathrm{Track}\ 00}$ - The Track 00 status line is set true when the read/write heads are positioned over track 00.

<u>Write Fault</u> - The Write Fault signal is true under the following fault conditions:

- a. Write current in a head when Write Gate is false.
- b. No write current in any head when both Write Gate and Drive Selected are true.
- c. More than one head is selected.
- d. The 12 volt supply is below 10.3 volts.
- e. The 5 volt supply is below 4.5 volts.
- f. Motor speed exceeds ± 1 % tolerance after the power-up sequence is completed.
- g. Motor speed exceeds +10% tolerance.
- h. No index signal.
- i. Motor not up to speed.
- j. Step signal received while Write Gate is true.

<u>Head Select</u> - Up to eight read/write heads may be selected using a 3-bit code on the Head Select 0, Head Select 1 and Head Select 2 lines. Table 8-4 is a head select matrix showing the logic level required on each Head Select line to select the desired read/write head.

Table 8-4. Head Select Decode Matix

	LINE	HDO	HD1	HD2	HD3	HD4	HD5	HD6	HD7
Head	Select 0	False	True	False	True	False	True	False	True
Head	Select 1	False	False	True	True	False	False	True	True
Head	Select 2	False	False	False	False	True	True	True	True

 \underline{Index} - The Index signal is a 200-microsecond output pulse used to mark a fixed reference point relative to the disk.

<u>Ready</u> - The Ready signal is true when the Drive is ready to read or write (with or without an implied seek) and the other lines are valid. Ready remains true until power-off or until there is a Write Fault. The Ready signal is false under the following conditions:

- a. The Drive is undergoing power-up.
- b. Motor speed is out of tolerance (+10%, -5% of nominal).
- c. Write Fault is true.

<u>Drive Select</u> - The Drive Select signal from the WDC corresponds with the Drive Select switch setting of the Drive. If the Drive Select signal does not correspond, and the Ready signal is true, a Drive Select true signal is returned to the WDC, via the data lines.

<u>Step</u> - The Step signal pulse from the WDC is used in conjunction with the Direction In signal to move the stepper motor. This pulse input to the microcomputer is used to clock an internal 8-bit counter, which is reset prior to each seek.

Once the first step pulse is received, the microcomputer issues stepper motor phase changes until the number of changes equals the value in the counter .

<u>Direction In</u> - The Direction In signal from the WDC determines the direction of motion of the stepper motor. The microcomputer receives the first step pulse of each seek, samples the input and internally stores the result.

8.3.3 Winchester Drive Controller

The Winchester Drive Controller (WDC) operates in conjunction with an. adapter board that permits the WDC SASI interface to communicate with the Central Microprocessor Board global bus. The two boards are "piggybacked," with the WDC PCBA mounted above the component side of the WDC Bus Adapter PCBA.

They are electrically interconnected by a 50-pin flat ribbon connector at J4 and by a 4-pin AMP connector at J3 (power).

The simplified block diagram in figure 8-6 shows the functional organization of the WDC. Only the major areas are shown, and they are defined as follows:

- Host Interface The host interface connects the internal data bus to the WDC Bus Adapter PCBA. The state machine controls the movement of data and commands through the host interface.
- Processor The eight-bit microprocessor is the intelligence of the WDC. It monitors and controls the operation of the WDC.
- State Machine The state machine controls and synchronizes the operation of the host interface, serializer/deserializer (SERDES) and sector buffer.
- SERDES The serializer/deserializer (SERDES) converts parallel data from the internal data bus to serial data for transfer to a selected Drive. It converts serial data from the selected Drive to parallel data, which it places on the internal data bus.

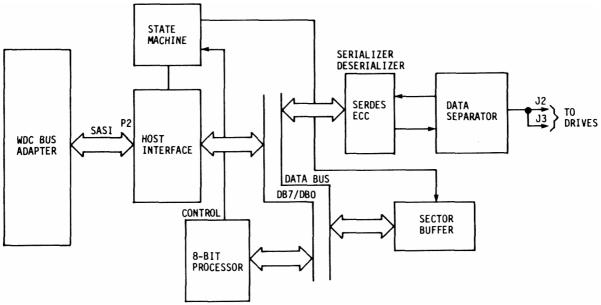


Figure 8-6. Controller, Functional Organization

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- Data Separator The data separator converts serial TTL data to MFM for transfer to the selected Drive. It converts MFM data coming from the selected Drive to serial TTL data for the SERDES.
- Sector Buffer The sector buffer stages data transfers between the disk and the host to prevent data overuns. The sector buffer (FIFO) comprises 1K bytes of dual port RAM, for rapid data transfers. No sector interleaving is required.

8.3.3.1 Signal Definitions

Tables 8-5 through 8-9 list and define the signals that appear on the SASI bus lines between the WDC Bus Adapter and the Winchester Drive Controller.

The dash(-), or the lack of one, indicates the active state of a signal (the active state of a signal is that state that is required for a given operation):

When a dash is appended to the end of a signal name, the signal is active when it is low, and

when no dash appears at the end of a signal name, the signal is active when it is high.

Some signal lines have two so-called active (or significant) states:

When the level on the line is high, a particular operation takes place, and

when the level on the line is low, a different operation occurs.

The following examples show the use of these conventions.

- BUSY- The signal BUSY- is active when it is at low level because it has the dash appended.
- BUSY The signal BUSY is active at a high level because it does not have the dash appended.
- C-/D The line C-/D (command-/data) has a dual purpose: the slash (/) indicates quality; that is, the dash after the C indicates that when this line has a low level, the command mode is indicated, and when the line has a high level, data mode is indicated.

Other designations used to define signal lines are listed below.

- Drv Driver
- Rcvr Receiver
- OC Open collector
- Tri-State Line has three states: high, low and high impedance
- 220/330 Line termination: 220 ohms to source voltage and 330 ohms to ground

Table 8-5. SASI Bus Status Signals

NAME DRV/RCVR DEFINITION

- I-/0 Drv OC Input-/Output: The controller drives this line. A low level on this line indicates that the controller is driving the data in on the SASI bus. A high level on this line indicates that the WDC Bus Adapter is driving the data out on the SASI bus. The WDC Bus Adapter monitors this line and uses it to enable and disable its data bus drivers. This signal is qualified by signal REQ-.
- C-/D Drv OC Control-/Data: This signal line indicates whether the information on the data bus consists of control or data bytes. A low means command bytes; a high means data bytes. This signal is qualified by signal REQ-.
- BUSY- Drv OC Busy: The controller generates this active low signal in response to the SEL- signal and the address bit (DBO- to DB7-) from the WDC Bus Adapter. The busy signal informs the WDC Bus Adapter that the controller is ready to conduct transactions on the SASI bus.

Table 8-6. Summary of SASI Bus Status Signals

- I-/0 C-/D MSG- DEFINITION
- High Low High The controller receives commands from the WDC Bus Adapter.
- High High The controller receives data from the WDC Bus Adapter.
- Low High High The controller sends data to the WDC Bus Adapter.
- Low Low High The controller sends an error status byte to the WDC Bus Adapter.
- Low Low Low The controller informs the WDC Adapter that it has completed the current command.

Table 8-7. Controller - Host Handshaking

NAME	DRV/RCVR	DEFINITION
NAME	DRV/RCVR	DEFINITIO

REQ- Drv OC Request: The controller sends this active low signal to the WDC Bus Adapter for each byte transferred across the interface. This signal qualifies signals I-/0, C-/D and MSG-.

ACK- Rcvr, Acknowledge: The WDC Bus Adapter generates this active low 220/330 signal in response to the REQ- signal from the controller when the host is ready to receive or transmit a byte of data. To complete the handshake, the WDC Bus Adapter must send an acknowledge in response to each request (REQ-). Table 8-8. Host Bus Control Signals

NAME DRV/RCVR DEFINITION

RST- Rcvr, Reset: The WDC Bus Adapter sends this active low signal to 220/330 the WDC to force the controller WDC to the idle state. After RST- has become active, any controller status is cleared. RST- also causes the deactivation of all signals to the drives. The time requirement for the RST- signal is as follows :

Minimum Maximum

100 nsec None

SEL- Rcvr, Select: The WDC Bus Adapter sends this active low signal to 220/330 the WDC to begin a command transaction. Along with SEL-, the WDC Bus Adapter also sends an address bit to select the controller (DBO- for controller). The controller must not be busy. The WDC Bus Adapter must deactivate SEL- before the end of the current command.

Table 8-9. Host Bus Data Signals

NAME DRV/RCVR DEFINITION

DBO- Tri-State These are the eight data bits (lines) of the host SASI bus to 220/330 (DBO = LSB). DB7-

The eight lines also are used as address bits to select a controller, in systems using multiple controllers. There is a one-to-one correspondence between the data lines and the controller select lines. The normal connection (hard-wired on the board) is to DBO-, which is the address of controller 0. Any other connection requires cutting the existing trace on the PCBA and adding a jumper.

The following list shows the bit assignments.

DB0-	Controller	0
DBl-	Controller	1
DB2-	Controller	2
DB3-	Controller	3
DB4-	Controller	4
DB5-	Controller	5
DB6-	Controller	6
DB7-	Controller	7

8.3.3.2 Detailed Description (Handshaking and Timing)

The following paragraphs describe the interaction between the Winchester Drive Controller (WDC) and the WDC Bus Adapter.

<u>Controller Selection</u> - Before the WDC Bus Adapter can begin a transaction, it must select the controller. The WDC Bus Adapter selects the controller by activating the SEL- control signal and the address bit of the controller. Any bit, DBO- through DB7-, can be the address bit in a system with multiple controllers (all controllers leave the factory with DBO- connected to the controllers' address logic). For this discussion, the controller's address is 0.

The timing diagram in figure 8-7 shows the basic timing requirements. Upon receiving both the SEL- signal and DBO-, the WDC activates the BUSYsignal. As shown in the timing diagram, both SEL- and DBO- mut be active (low) before the controller can activate the BUSY- signal. During the selection process, the host (the Central Microprocessor Board) has control of the data bus as signified by the deactivation of the I-/0 line. Selection is complete when BUSY- becomes active. The SEL- signal must be deactivated by the WDC Bus Adapter before the current controller operation has completed. It is recommended that the SEL- line be deactivated at or before the time the first control byte is sent to the controller (WDC). The controller then enters the command mode.

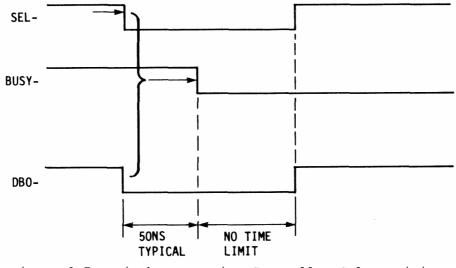


Figure 8-7. Winchester Drive Controller Select Timing

Command Mode - The Winchester Drive Controller (WDC) receives commands from the WDC Bus Adapter using a handshaking sequence. The controller places a low level on the C-/D (Control-/Data) line to indicate that it wants a command from the WDC Bus Adapter and places a high level on the I-/O line to indicate that the movement of information is from the Adapter to the controller. The MSG- line is high.

The controller activates the REQ- line within 10 microseconds after signals I-/0, C-/D and MSG- have been placed at high, low and high levels. The WDC Bus Adapter responds by activating the ACK- signal when a control byte is ready for the controller. The control byte placed on the data bus by the WDC Bus Adapter must be stable within 250 nanoseconds after the ACK- is activated. The control byte must be held stable until REQ- is deactivated. The WDC Bus Adapter deactivates ACK- after REQ- goes high. This completes the handshake for the first control byte. Each succeeding control byte from the WDC Bus Adapter requires the same complete handshake sequence. See figure 8-9 for data bus, REQ- and ACK- timing. See table 8-5 for I-/0, C-/D and MSG- definitions.

Data Transfer - The timing diagrams in figures 8-8 and 8-9 illustrate the required timing for data transfer. See table 8-5 for I-/0, C-/D and MSG-definitions.

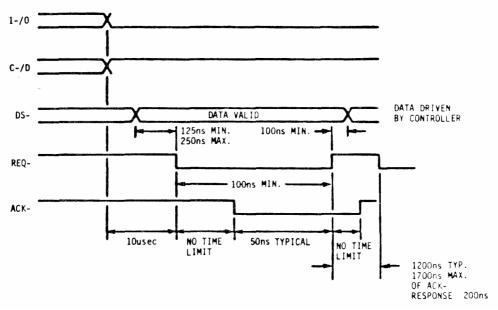


Figure 8-8. Data Transfer to Host, Timing

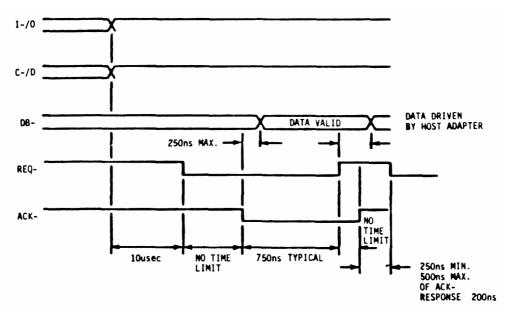


Figure 8-9. Data Transfer from Host, Timing

Status Bytes - Two bytes of status are passed to the host at the end of all commands. The first byte informs the host (Central Microprocessor Board via the WDC Bus Adapter PCBA) whether any errors occurred during the execution of the command. The second is a zero byte. It signals to the host that the command is complete. Figure 8-8 shows the data bus, REQ-, and ACK- timing. See table 8-5 for I-/0, C-/D and MSG- definitions. Figure 8-11 shows the format of these two bytes.

8.3.3.3 Programming Information

The following subsection discusses communication between the Winchester Drive Controller (WDC) and the host (Central Microprocessor Board) from the point of view of the codes that are passed. The host sends commands to the controller through the WDC Bus Adapter. The controller then implements the commands and reports back to the host.

8.3.3.4 Commands

The host sends a six-byte block to the controller to specify the operation. This block is the Device Control Block (DCB). Figure 8-10 shows the composition of the DCB. The list that follows figure 8-10 defines the bytes that make up the DCB.

At the end of a command, the controller returns two completion status bytes to the host. The format of these bytes is shown in figure 8-11.

Control Byte - The control field, byte 5, of the DCB allows the user to select options for several different types and makes of disk drives. The following list defines the bits of the control byte.

- Bit 0 Half-step option: Seagate Technology and Texas Instruments.
- Bit 1 Half-step option: Tandon
- Bit 2 Buffer-step option: Computer Memories, Inc. and Rotating Memories, Inc. (200 microsecond pulse per step)
- Bit 3-5 Spare. Set to zero for future use.
- Bit 6 If one during a read sector command, the failing sector is not re-read on the next revolution before attempting correction. This bit should be set to zero for normal operation.
- Bit 7 Disable the retries by the controller on all disk-access commands. Set this bit only during the evaluation of the performance of a disk drive. Otherwise, the bit should be set to zero.

NOTE

The step option bits (0-2) are mutually exclusive, and only one option should be selected in any given configuration.

BIT		7	б	5	4	3	2	1	0
Byte	0	Cla	iss Coo	de			Opcode	9	
Byte	1		LUN		Logi	cal	Block	Addre	SS
Byte	2		Lo	ogical	Bloc}	c Ac	ldress		
Byte	3		Logi	cal Blo	ock Ad	ddre	ess (L	SB)	
Byte	4	Number of Blocks							
Byte	5		Coi	ntrol 1	Byte	(res	served)	
Fig	ure	8-10.	Devic	e Cont	rol B	loc	k (DCE	3) Forr	nat

Byte 0 Bits 7, 6 and 5 identify the class of the command. Bits 4 through 0 contain the opcode of the command.										
Byte 1						al unit n block addr	umber (LUN ess 2.	1).		
Byte 2	Bits 7	throug	h 0 con	tain 1	ogical b	lock addr	ess 1.			
Byte 3	Bits 7 through 0 contain logical block address 0 (LSB).									
Byte 4	Bits 7	throug	h 0 spe	cify t	he block	count.				
Byte 5	Bits 7	throug	h 0 con	tain t	the contr	ol byte.				
Next to Last Status Byte										
BIT	7	6	5	4	3	2	1	0		
	0	0	0	d	BUSY	EQUAL	CHECK	0		
Bits 0, 5 6 7										
5, 6, 7 Bit 1 Check condition. Sense is available. Bit 2 Equal. Set when any SEARCH is satisfied. Bit 3 Busy. Device is busy or reserved.										
Last Status Byte										
BIT	7	6	5	4	3	2	1	0		
	0	0	0	0	0	0	0	0		
Bits Set to zero. 0-7										
Figure 8-11. Completion Status Bytes										
Logical Address (High, Middle, Low) - The logical address of the drive is computed by using the following equation.										
Logical Address = (CYADR * HDCYL + HDADR) * BKTRK + BKADR										
Where: CYADR = Cylinder Address HDADR = Head Address BKADR = Block (Sector) Address HDCYL = Number of Heads per Cylinder BKTRK = Number of Blocks (Sectors) per Track										

The commands fall into eight classes, 0 through 7; only classes 0 and 1 are used. Class 0 commands are data, non-data transfer, and status commands. Classes 1 through 6 are reserved. Class 7 are diagnostic commands.

Each command is described below. The description includes its class, opcode and format.

<u>Test Drive Ready (Class 0, Opcode 00)</u> - This command selects a particular drive and verifies that the drive is ready. The following diagram shows the format of the device control block for this command.

d = drive, 0 or 1

BIT	7	б	5	4	3	2	1	0
Byte O	0	0	0	0	0	0	0	0
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	0	0	0	0	0	0	0	0
Byte 4	0	0	0	0	0	0	0	0
Byte 5	0	0	0	0	0	0	0	0

Rezero Unit (Class 0, Opcode 01) - This command positions the read/write $(\mbox{R/W})$ arm to track 00.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	0	0	0	0	1
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	0	0	0	0	0	0	0	0
Byte 4	0	0	0	0	0	0	0	0
Byte 5	0	0	0	0	0	0	0	0
Reserved (Class 0,	Opcod	de 02	<u>) – r</u>	This	opcode	e is :	not u	sed.

<u>Request Sense Status (Class 0, Opcode 03)</u> - The host must send this command immediately after it detects an error. The command causes the controller to return four bytes of drive and controller status. The formats of these four bytes are shown after the DCB. When an error occurs on a multiple sector data transfer (read or write), the Request Sense Status command returns the logical address of the failing sector in bytes 1, 2 and 3. If the Request Sense Status command is issued after any of the format commands or the Check Track Format command, then the logical address returned by the controller points to one sector beyond the last track formatted, or checked, if there was no error.

If there was an error, then the logical address returned points to the track in error. Tables 8-10 through 8-13, which follow the formats, list the error codes.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	0	0	0	1	1
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	0	0	0	0	0	0	0	0
Byte 4	0	0	0	0	0	0	0	0
Byte 5	0	0	0	0	0	0	0	0

SENSE BYTES

0

BIT	7	6	5	4	3	2	1	
Byte O			S	EE BE	LOW			
Bits 0-3 Bits 4-6 Bit 7	Erro	or '	Code Type valid	, whe	n set			

The address valid bit in the error code byte (bit 7) is relevant only when the previous command required a logical block address, in which case it is always returned as a one; otherwise, it is set to zero. For instance, if a Recalibrate command is followed immediately by a Request Sense Status command, the address valid bit would be returned as zero, since this command does not require a logical block address to be passed in its DCB.

 BIT
 7
 6
 5
 4
 3
 2
 1
 0

 Byte 1
 000
 Logical Block Address
 Image: Comparison of the state of

Table 8-10. Type 0 Error Codes, Disk Drive

HEX	
CODE	DEFINITION
00	The controller detected no error during execution of the previous oper- ation.
01	The controller did not detect an index signal from the drive.
02	The controller did not get a seek complete signal from the drive after seek operation.
03	The controller detected a write fault from drive during last operation.
04	After the controller selected the drive, the drive did not respond with ready signal.
06	After stepping the maximum number of cylinders, the controller did not receive the track 00 signal from the drive.
	Table 8-11. Type 1 Error Codes, Controller
HEX CODE	DEFINITION
10	ID Read Error: the controller detected a CRC error in the target ID field on the disk.
11	Data Error: the controller detected an uncorrectable data error in the target sector during a read operation.
12	Address Mark: the controller did not detect the ID address mark.
13	Address Mark: the controller did not detect the data address mark.
14	Record Not Found: the controller found the correct cylinder and head, but not the target record.
15	Seek Error: the controller detected an incorrect cylinder or track, or both.
18	Data Check in No Retry Mode
19	ECC Error During Verify
1A	Interleave Error
1C	Unformatted or Bad Format on Drive
1D	Self Test Failed
1E	Defective Track: the controller detected the bad track flag.

Table 8-12. Type 2 Error Codes, Command and Miscellaneous

HEX CODE	DEFINITION
20	Invalid Command: the controller has received an invalid command from the disk.
21	Illegal Block Address: the controller detected an address that is be- yond the maximum range.
23	Volume Overflow
24	Bad Argument
25	Invalid Logical Unit Number

The following is a summary of the error codes returned as the result of the Request Sense Status command.

NOTE: The address valid bit (bit 7) may or may not be set and is not included here, for clarity.

Table 8-13. Request Sense Status Error Codes

ERROR CODE (HEX)

DEFINITION

00	No error detected (command completed okay)
01	No index detected from drive
02	No seek complete from drive
03	Write fault from drive
04	Drive not ready after it was selected
06	Track 00 not found
10	ID field read error
11	Uncorrectable data error
12	ID address mark not found
13	Data address mark not found
14	Record not found
15	Seek error
18	Data Check in No Retry mode
19	ECC error during verify
1A	Interleave error
1C	Unformatted or bad format on drive
1D	Self test failed
1E	Defective track
20	Invalid command
21	Illegal block address
23	Volume overflow
24	Bad Argument
25	Invalid logical unit number

NOTE: 05, 07-OF, 16/17, 1B, 1F, 22 and 26-2F are not assigned.

Format Unit (Class 0, Opcode 04) - This command formats all sectors with ID and data fields, according to the selected interleave factor. The controller will write from index to index all ID and data fields with a block size as specified by an Immediately previous Mode Select command. If no Mode Select command has been executed, the previous data block size wil be used. On unformatted disks, or on those whose format is determined bad (sense byte error code 1C [hex] returned following a Read command), a Mode Select command is required prior to the Format Unit command. Data fields are completely written with 6C (hex) unless otherwise specified in the Format Unit command.

The ID fields will be interleaved as specified in bytes 3 and 4 of the Command Description Block (CDB). Under normal conditions, the Winchester Drive Controller does not require interleaving, because of its high speed buffer control.

An interleave number of 1 results in sequential ID fields being written on the disk. Any interleave number greater than 1, but less than the total number of sectors per track, results in interleaved formatting. A 00 in this field will cause the default interleave factor of 2 to be used. The interleave number is equivalent to the number of disk revolutions required to sequentially read one track.

When the data bit is set (bit 4, byte 1), the controller expects a list of known bad areas in the data portion of the command (defect skipping).

Bit 3 (byte 1) is the complete list bit. It specifies that all the known defects on the drive are contained in the list.

Bit 2 (byte 1), if set, indicates that the next two bits (1 and 0) will be used to define the format. A zero indicates default. Bit 1, if set, indicates that the data pattern in byte 2 is to be used to format the disk. A zero indicates default. A zero in bit 0 indicates that a "Cylinder/ Head/Byte Count" format is used in the data list.

```
d = drive, 0 \text{ or } 1
```

- b = data bit
- c = complete list bit
- f = list format bit

BIT	7	б	5	4	3	2	1	0		
Byte O	0	0	0	0	0	1	0	0		
Byte 1	0	0	d	b	С	f	f	f		
Byte 2	Data Pattern									
Byte 3	0	0	0	0	0	0	0	0		
Byte 4	Interleave Number									
Byte 5	0	0	0	0	0	0	0	0		

Reserved (Class 0, Opcode 05) - This opcode is not used.

Reserved (Class 0, Opcode 06) - This opcode is not used.

Reserved (Class 0, Opcode 07) - This opcode is not used.

<u>Read (Class 0, Opcode 08)</u> - This command transfers to the host the specified number of blocks starting at the specified logical starting block address. The controller will verify a valid seek address and proceed to seek to the specified starting logical block address. When the seek is complete, the controller then reads the starting address data field into the buffer, checks the ECC and begins DMA data transfer.

Subsequent blocks of data are transferred into the buffer in a similar manner until the block count is decremented to zero. Cylinder switching is transparent to the user.

On a data ECC error, the block is re-read up to five times to establish a "solid error syndrome." Only then is correction attempted. Correction is done directly into the data buffer, transparent to the user.

d = drive, 0 or 1

BIT	7	б	5	4	3	2	1	0			
Byte O	0	0	0	0	1	0	0	0			
Byte 1	0	0	d	Log	ical	Block	Addr	ess			
Byte 2	Logical Block Address										
Byte 3		Log	ical	Block	Addr	ess (I	SB)				
Byte 4	Block Count										
Byte 5	0	0	0	0	0	0	0	0			

Reserved (Class 0, Opcode 09) - This opcode is not used.

<u>Write (Class 0, Opcode OA)</u> - This command transfers to the target device the specified number of blocks, starting at the specified logical starting block address. The controller seeks to the specified logical starting block. When the seek is complete, the controller transfers the first block into its buffer and writes its buffered data and its associated ECC into the first logical sector.

Subsequent blocks of data are transferred as they become available from the FIFO buffer, until the block count is decremented to zero. Cylinder switching and defect skipping are transparent to the user.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0		
Byte O	0	0	0	0	1	0	1	0		
Byte 1	0	0	d	Log	ical 1	Block	Add	ress		
Byte 2	Logical Block Address									
Byte 3		Logi	cal B	lock .	Addres	ss (I	SB)			
Byte 4	Block Count									
Byte 5	0	0	0	0	0	0	0	0		

<u>Seek (Class 0, Opcode OB)</u> - This command causes the selected drive to seek to the specified starting address. The controller returns completion status immediately after the seek pulses are issued and head motion starts. This allows the controller to free the bus and accept further commands prior to actual seek completion.

NOTE

Any command received for a unit with a seek in progress will immediately complete with the busy command completion status (bit 3 set). This is done to allow the host to use the SASI bus to do other processing while waiting for seek to complete.

The drive is stepped to the addressed track position, but no ID field verification is attempted. When the seek is complete, the controller reconnects to the host and responds with the completion status.

The Winchester Drive Controller uses an implied seek on READ, WRITE and SEARCH commands, obviating the need for issuance of SEEK commands with each operation.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0	
Byte O	0	0	0	0	1	0	1	1	
Byte 1	0	0	d	Logi	cal B	lock	Addr	ess	
Byte 2	Logical Block Address								
Byte 3		Logi	cal B	lock	Addre	ss (L	SB)		
Byte 4	0	0	0	0	0	0	0	0	
Byte 5	0	0	0	0	0	0	0	0	

Reserved (Class 0, Opcode OC) - This opcode is not used.

Reserved (Class 0, Opcode OD) - This opcode is not used.

Reserved (Class 0, Opcode OE) - This opcode is not used.

<u>Translate (Class 0, Opcode OF)</u> - This command performs a logical address to physical address translation and returns the physical location of the requested block address in a cylinder/head/bytes-from-index format. This data can be used to build a defect list for the FORMAT command.

Eight bytes are returned in the format of defect descriptors, required by FORMAT.

A data error in the ID field will cause an error status to be returned. It is then necessary to TRANSLATE the blocks before and after the targeted block to determine the location of the target block. The use of interleaved sectors and formatted (skipped) defects may complicate the determination of the error location.

d = drive, 0 or 1

BIT	7	б	5	4	3	2	1	0		
Byte O	0	0	0	0	1	1	1	1		
Byte 1	0	0	d	Log	ical	Block	Addr	ess		
Byte 2	2 Logical Block Address									
Byte 3		Log	gical	Bloc	k Add	ress	(LSB)			
Byte 4	0	0	0	0	0	0	0	0		
Byte 5	0	0	0	0	0	0	0	0		

Reserved	(Class	Ο,	Opcode	10)	-	This	opcode	is	not	used.
Reserved	(Class	Ο,	Opcode	11)	-	This	opcode	is	not	used.
Reserved	(Class	Ο,	Opcode	12)	-	This	opcode	is	not	used.

<u>Write Data Buffer (Class 0, Opcode 13)</u> - This command serves buffer RAM diagnostic purposes. The controller will fill the buffer with IK bytes of data from the host. There is no guarantee that this data will not be overwritten by other operations initiated by other initiators.

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```
d = drive, 0 \text{ or } 1
```

<u>Read Buffer RAM (Class 0. Opcode 14)</u> - Read Buffer RAM will pass the host IK bytes of data from the buffer. It is intended for RAM diagnostic purposes. There is no guarantee that this data will not be overwritten by other operations initiated by other initiators. In addition, although data remains in the buffer after normal data operations, the ordering of the data found there is undefined.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	1	0	1	0	0
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	0	0	0	0	0	0	0	0
Byte 4	0	0	0	0	0	0	0	0
Byte 5	0	0	0	0	0	0	0	0

Mode Select (Class 0, Opcode 15) - This command is used to specify FORMAT parameters and should always precede the FORMAT command.

A blown format error (code 1C) is detected when the controller is unable to read the drive information from a drive already formatted. The user should use this command to inform the controller about the drive information. Then the drive should be backed up and reformatted.

Byte 4 of the command specifies the number of information bytes to be passed with the command. A minimum of twelve bytes (OC [hex]) must be specified. If drive parameters are being specified, the count should be 22 bytes (16 [hex]). The Parameter List is four bytes long, with the first three bytes reserved (zero filled). The fourth byte contains the length, in bytes, of the Extent Descriptor List; this is always eight. (Only a single extent is supported.)

MODE SELECT PARAMETER LIST

BIT	7	б	5	4	3	2	1	0
Byte O	0	0	0	0	0	0	0	0
Byte 1	0	0	0	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	0	0	0	0	1	0	0	0
			EXTENT	DES	SCRIPTOR	S LI	IST	
BIT	7	6	extent 5	DES 4	SCRIPTOR 3	а LI 2	IST 1	0
BIT Byte O		6 0						0
	0		5	4	3	2	1	
Byte O	0 0	0	5 0	4 0	3 0	2 0	1 0	0

BIT	7	б	5	4	3	2	1	0
Byte O	0	0	0	0	0	0	0	0
Byte 1	0	0	0	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	0	0	0	0	0	0	0	0
Byte 4	0	0	0	0	0	0	0	0
Byte 5			Blo	ck Si	ze (M	SB)		
Byte 6				Block	Size			
Byte 7			Blo	ck Si	ze (L	SB)		

Byte 0 of the Extent Descriptor List specifies the data density of the drive. The Winchester Drive Controller supports only MFM, and a value of 00 is required in this byte. Bytes 1, 2 and 3 are reserved and must be zero, specifying that the entire drive is to be formatted. Bytes 5 through 7 are used to specify the data block size. The block size must not be less than 256 or exceed the RAM buffer capacity, which is IK bytes, or 1,024 characters.

In this controller the block size must be set up with a value 256, 512 or 1024 bytes. Violation of this constraint results in Check Status with an Error Code of 24 [hex], indicating an invalid argument in parameter data.

The Extent Descriptor List and the Drive Parameter List (described next) are a single large block of data that follows the command.

The Drive Parameter List includes all the data necessary to specify a drive. It is optional, but if present, it must be complete, and the items must be within the limits stated. If these parameters are not supplied, the format operation will use previously supplied values, if available, or the default values given on the following page.

The List Format Code must be 01.

DRIVE PARAMETER LIST

BIT	7 6	5 5	4	3	2	1	0
Byte O		List Fo	ormat	Code	== 01		
Byte 1		Cylind	der Co	unt	(MSB)		
Byte 2		Cylind	der Co	unt	(LSB)		
Byte 3		Data	a Head	Cou	nt		
Byte 4	Reduo	ced Write	e Curr	ent (Cylind	er	(MSB)
Byte 5	Reduc	ced Write	e Curr	ent	Cylind	er	(LSB)
Byte 6	Write	e Precom <u>r</u>	pensat	ion	Cylind	er	(MSB)
Byte 7	Write	e Precom <u>r</u>	pensat	ion	Cylind	er	(LSB)
Byte 8		Landing	g Zone	Pos	ition		
Byte 9	St	ep Pulse	e Outp	ut R	ate Co	de	

The Cylinder Count is the number of data cylinders on the drive. Because of the inline defect skipping formatting, cylinders normally set aside as spares may be included in this total. The minimum is one. The maximum supported is 2,048. The default value is 306.

The Data Head Count is the number of usable data surfaces. The heads will be selected from 0 to head count minus 1. The minimum is 1; the maximum is 16. A drive with nine or more heads will use the Reduced Write Current line as the high order head select. The default value is two.

The Reduced Write Current Cylinder is the cylinder number beyond which the controller will assert the Reduced Write Current line. The minimum value is 0; the maximum is 2,047. The default value is cylinder 150.

The Write Precompensation Cylinder is the cylinder beyond which the controller will compensate for inner track bit shift. The specifications for this function agree with those of most disk manufacturers. Minimum value is 0; maximum is 2,047.

The Landing Zone Position is used with the Start/Stop command to indicate the direction and number of cylinders from the last data cylinder to the shipping position. The most significant bit indicates the direction, with a zero meaning that the landing zone is beyond the highest track, and a one indicates the landing zone is outside track 00. Thelow seven bits gives the number of cylinders. The default value is zero (land on innermost track).

The Step Pulse Output Rate Code specifies the timing of seek steps. Three options are available:

00 = non-buffered, 3 ms; 01 = buffered, 0.028 ms; 02 = buffered, 0.012 ms.

Reserved (Class 0, Opcode 16) - This opcode is not used.

Reserved (Class 0, Opcode 17) - This opcode is not used.

Reserved (Class 0, Opcode 18) - This opcode is not used.

Reserved (Class 0, Opcode 19) - This opcode is not used.

<u>Mode Sense (Class 0, Opcode 1A)</u> - This command is used to interrogate the Winchester Drive Controller parameter table to determine the specific characteristics of any disk drive currently attached.

The attached drive must have been formatted by this controller for this to be a legal command.

Byte 4 of the command specifies the number of data bytes to be returned from the command. A minimum of 12 bytes (OC [hex]) must be specified. If the drive parameter list is required, the count should be 22 bytes (16 [hex]).

The returned information will be the four-byte parameter list, the Extent Descriptor List and the Drive Parameter List (if requested). These lists take the exact format of those in the MODE SELECT command. Please reference that command for details.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	1	1	0	1	0
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	0	0	0	0	0	0	0	0
Byte 4		Numbe	er of	Byte	s Ret	urned		
Byte 5	0	0	0	0	0	0	0	0

<u>Start/Stop Unit (Class 0, Opcode 1B)</u> - Byte 4, bit 0 of this command should be set if this is a START command; otherwise, it is a STOP command.

This command is designed for use on drives with a designated shipping or landing zone.

A STOP command will move the head to the landing zone position.

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d = drive, 0 or 1

s = Start/Stop, 0 or 1

BIT	7	б	5	4	3	2	1	0
Byte O	0	0	0	1	1	0	1	1
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	0	0	0	0	0	0	0	0
Byte 4	0	0	0	0	0	0	0	S
Byte 5	0	0	0	0	0	0	0	0

<u>Receive Diagnostic Result (Class 0, Opcode 1C)</u> - This command sends analysis data to the host (Central Microprocessor Board) after completion of a SEND DIAGNOSTIC command. Bytes 3 and 4 designate the size of the available buffer (in bytes).

READ DIAGNOSTIC is used to transfer data to the host and must immediately follow a SEND DIAGNOSTIC command, which initiates the dump action. Otherwise, the command will be rejected.

The data length specified should be 104 (hex) or more; however, if a smaller buffer is provided, only that much data will be transferred, and the command will terminate normally.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	1	1	1	0	0
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3			Data	Leng	th (MSB)		
Byte 4			Data	Leng	th (LSB)		
Byte 5	0	0	0	0	0	0	0	0

The data received as a result of a dump will be formatted as follows (next page):

BIT	7 6 5 4 3 2 1 0
Byte O	Data Block Length (MSB)
Byte 1	Data Block Length (LSB)
Byte 2	Starting Address of Dump (MSB)
Byte 3	Starting Address of Dump (LSB)
Byte 4	Dumped Data (xx00)
•	
• Byte 103	Dumped Data (xxFF)

<u>Send Diagnostic (Class 0, Opcode 1D)</u> - This command sends data to the controller to specify diagnostic tests for controller and peripheral vmits.

Bytes 3 and 4 specify the length of the data to be sent.

The data length specified in the command must be at least 4 bytes long and should be equal to the length of the data block to be passed over to the controller. If the length specified is longer than needed, the excess is ignored and not read.

The first byte of the data block specifies the particular function being requested. The options available, along with their associated codes are:

HEX CODE	DEFINITION
60	Reinitialize Drive
61	Dump Hardware Area (4000-40FF)
62	Dump RAM (8000-80FF)
63	Patch Hardware Area
64	Patch RAM
65	Set Read Error Handling Options

Of these options, only the patch options require a data block longer than four bytes.

The second byte specifies a subtest or qualifiers specific to the test selected by the first byte. (Because of the potential danger in patching controller programs, this byte provides a safety mechanism to prevent obsolete patches.) The second byte is not checked if the 65 (hex) option code is specified.

The third byte specifies the starting address (in RAM or the memory-mapped registers) to be patched. The high byte of the address is implicit in the

diagnostic specified. Therefore, a Patch RAM operation with a third byte of Al (hex) will overwrite an area of RAM starting with 80A1 (hex).

The fourth byte gives the number of bytes to be overwritten. This can range from 1 to 256, with a zero yielding 256. the data block for the Send Diagnostic Command is as follows.

BIT	7	б	5	4	3	2	1	0
Byte O			Diagn	ostic	Spec	ifier		
Byte 1	Diag	gnost	ic Op	tion/(Coded	Rele	ase L	evel
Byte 2	Pate	ch St	artin	g Addı	ress	LSB/Q	ualif	ier
Byte 3		Patc	h Dat	a Leng	gth o	r Res	erved	
Byte 4 •			Opti	onal I	Patch	Data		
•								
• Byte N+3			Opti	onal I	Patch	Data		

Byte 2 of the data block specifies the actions to take place upon encountering an ECC check, if option 65 (hex) is selected. The default state is established by a controller reset.

These options, once set, stay in effect until the next reset. They apply only to the Logical Unit Number addressed by the command.

The Set Read Error Handling Options are:

HEX CODE

DEFINITION

00 Selects default operation where a correctable error will be corrected without comment and all data transferred without check status.

If the error is not correctable, the controller will transfer the uncorrected data and set check status with an error code 91 (hex). The valid address will be that of the bad block.

01 Report all corrections and stop. A correctable error will be corrected and the data transferred, but the operation will stop with a check status and an error code (hex).

An uncorrectable error will be handled as in OO (hex), above.

02 Do not correct. All ECC errors will be treated as uncorrectable , except that the error code is set to 98 (hex). Reserved (Class 0, Opcode 1E) - This opcode is not used.

Reserved (Class O, Opcode 1F) - This opcode is not used.

Reserved (Class 1, Opcode 20) - This opcode is not used.

Reserved (Class 1, Opcode 21) - This opcode is not used.

Reserved (Class 1, Opcode 22) - This opcode is not used.

Reserved (Class 1, Opcode 23) - This opcode is not used.

Reserved (Class 1, Opcode 24) - This opcode is not used.

<u>Read Capacity (Class 1, Opcode 25)</u> - If byte 8 of the Device Control Block (DCB) is 00, this command will return the address of the last block on the unit. It is not necessary to specify a starting block address in this command mode.

If byte 8 is 01 (hex), this command will return the address of the block (after the specified starting address) at which a substantial delay in data transfer will be encountered (e.g., a cylinder boundary). Any value other than 00 or 01 (hex) in byte 8 will cause Check Status with an Error code of 24 (hex), for an invalid argument.

In both cases, the format block size is defined by the last four bytes of the eight-byte data field returned as a result:

4 bytes, Block Address 4 bytes, Block Size

d = drive, 0 or 1

r = relative address, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	1	0	0	1	0	1
Byte 1	0	0	d	0	0	0	0	r
Byte 2		Log	ical	Block	Addr	ess	(MSB)	
Byte 3			Logic	al Blo	ock A	ddres	5S	
Byte 4			Logic	al Blo	ock A	ddres	SS	
Byte 5		Log	ical	Block	Addr	ess	(LSB)	
Byte 6	0	0	0	0	0	0	0	0
Byte 7	0	0	0	0	0	0	0	0
Byte 8		Full	or Pa	rtial	Medi	.a Inc	dicato	r
Byte 9	0	0	0	0	0	0	0	0

Reserved (Class 1, Opcode 26) - This opcode is not used. Reserved (Class 1, Opcode 27) - This opcode is not used. Reserved (Class 1, Opcode 28) - This opcode is not used. Reserved (Class 1, Opcode 29) - This opcode is not used. Reserved (Class 1, Opcode 2A) - This opcode is not used. Reserved (Class 1, Opcode 2A) - This opcode is not used. Reserved (Class 1, Opcode 2B) - This opcode is not used. Reserved (Class 1, Opcode 2C) - This opcode is not used. Reserved (Class 1, Opcode 2C) - This opcode is not used.

<u>Write and Verify (Class 1, Opcode 2E)</u> - This command is similar to the traditional "read after write" function. It is an extended address command that operates like a WRITE command over the specified number of blocks and then verifies the data written on a block by block basis. The verify function transfers no data to the host.

Since no data is transferred to the host during verify, correctable data checks will be treated in the same manner as uncorrectable data checks.

d = drive, 0 or 1

BIT	7	б	5	4	3	2	1	0
Byte O	0	0	1	0	1	1	1	0
Byte 1	0	0	d	0	0	0	0	0
Byte 2,		Log	ical 1	Block	Addr	ess ()	MSB)	
Byte 3		L	ogica	l Blo	ock A	ddres	S	
Byte 4		L	ogica	l Blo	ock A	ddres	S	
Byte 5		Log	ical 1	Block	Addr	ess (LSB)	
Byte 6	0	0	0	0	0	0	0	0
Byte 7			Nur	mber (of Bl	ocks		
Byte 8			Nur	mber (of Bl	ocks		
Byte 9	0	0	0	0	0	0	0	0

 $\frac{\text{Verify}(\text{Class 1, Opcode 2F})}{\text{WRITE AND VERIFY}}$ - This command is similar to the previous WRITE AND VERIFY except that it verifies the ECC of an already existing set of data blocks.

It is the responsibility of the host to provide data for rewriting and correcting when an error is detected.

BIT	7	6	5	4	3	2	1	0		
Byte O	0	0	1	0	1	1	1	1		
Byte 1	0	0	d	0	0	0	0	0		
Byte 2		Log	ical	Bloc	k Add	ress	(MSB)		
Byte 3			Logic	al B	lock	Addre	SS			
Byte 4		Logical Block Address								
Byte 5		Log	ical	Bloc	k Add	ress	(LSB)		
Byte 6	0	0	0	0	0	0	0	0		
Byte 7			Nu	mber	of Bl	ocks				
Byte 8			Nu	mber	of Bl	ocks				
Byte 9	0	0	0	0	0	0	0	0		

d = drive, 0 or 1

Reserved (Class 1, Opcode 30) - This opcode is not used.

<u>Search Data Equal (Class 1, Opcode 31)</u> - This powerful extended address command provides for a "search-and-compare-on-equal" of any data on the disk. The starting block address and number of blocks to search are specified, and a search argument, which includes a byte displacement and the data to compare, is passed from the host.

The Invert bit (byte 1, bit 4) inverts the sense of the search comparison operation. With invert on, a SEARCH DATA EQUAL command would succeed on data not equal; SEARCH DATA LOW would succeed on data greater or equal. The invert bit allows SEARCH EQUAL inverted, which succeeds on the first block not equal to the pattern.

When a search is satisfied, it will terminate with a Condition Met Status. A Request Sense Command can then be issued to determine the block address of the matching record. A Request Sense following a successful Search Data command will:

- Report a Sense Key of Equal, if the search was satisfied by an exact match. If the search was satisfied by an inequality, a Sense Key of No Sense is reported.
- 2. Set the Valid bit to one.
- 3. Report the address of the block containing the first matching record in the Information Bytes.

The Request Sense command following an unsuccessful Search Data Command will: 1) Report a Sense Key of No Sense, provided no errors occurred; and 2) Set the Valid bit to zero.

```
d = drive, 0 \text{ or } 1
i = invert, 0 or 1
        BIT
                    7
                         б
                              5
                                   4
                                        3
                                            2
                                                 1
                                                      0
        Byte 0
                     0
                         0
                              1
                                   1
                                        0
                                            0
                                                 0
                                                      1
        Byte 1
                     0
                         0
                            d
                                 i
                                        0
                                            0
                                                      0
                                                 0
        Byte 2
                        Logical Block Address (MSB)
        Byte 3
                           Logical Block Address
        Byte 4
                           Logical Block Address
                        Logical Block Address (LSB)
        Byte 5
                     0 0
                              0 0 0
                                          0
                                                     0
        Byte 6
                                                 0
        Byte 7
                              Number of Blocks
        Byte 8
                              Number of Blocks
        Byte 9
                              0 0
                                     0
                     0
                         0
                                          0
                                                 0
                                                      0
```

The argument following a SEARCH command is presented on the following page.

SEARCH COMMAND ARGUMENT

BIT	7 6	5	4	3	2	1	0
Byte O		Record	Size	(MS	B)		
Byte 1		Reco	ord Si	ize			
Byte 2		Reco	ord Si	ize			
Byte 3		Record	Size	(LS	B)		
Byte 4	Firs	t Recor	d Of	fset	(MSB)	
Byte 5	F	irst Re	ecord	Off	set		
Byte 6	F	irst Re	ecord	Off	set		
Byte 7	Firs	t Recor	d Ofi	fset	(LSB)	
Byte 8	Num	ber of	Reco	rds (MSB)		
Byte 9		Number	of Re	ecord	S		
Byte 10		Number	of Re	ecord	S		
Byte 11	Num	ber of	Reco	rds (LSB)		
Byte 12	Searc	h Argum	nent l	Lengt	h (M	SB)	
Byte 13	Se	arch Ar	rgumer	nt Le	ngth		
Byte 14	Searc	h Field	l Disp	place	ment	(MSB)
Byte 15	Sea	rch Fie	eld D:	ispla	cemen	t	
Byte 16	Sea	rch Fie	eld D:	ispla	cemen	t	
Byte 17	Searc	h Field	l Disp	place	ment	(LSB)
Byte 18	P	attern	Lengt	th (M	SB)		
Byte 19		Patte	ern Le	ength			
Byte 20 •		Data	a Patt	tern			
•							
Byte M+19		Data	a Patt	tern			

A definition of the required data in the SEARCH argument is presented on the following page.

SEARCH COMMAND ARGUMENT REQUIRED DATA

BYTES PARAMETER

- 0 to 3 Record Size (bytes) This must equal the blocksize or zero. Zero will be taken to mean the format blocksize.
- 4 to 7 First Record Offset (bytes) This must be zero.
- 8 to 11 Number of Records This must be less than or equal to the number of blocks specified in the command and greater than zero. The search will terminate upon a match or when the smaller of these values is encountered.
- 12 to 13 Search Argument Length (bytes) The number of bytes in the following search argument. Must equal the pattern length plus six.
- 14 to 17 Search Field Displacement The displacement from the beginning of the record to the first byte to be compared. Must be zero.
- 18 to 19 Pattern Length (M bytes) The number of bytes in the following data pattern to be compared with a like size field in each record. Pattern length must equal blocksize.
- 20 to M+19 Data Pattern A variable length field of M bytes up to blocksize minus displacement bytes. The pattern must be one block long.

8.4 MAINTENANCE

The following paragraphs provide information necessary for maintenance of the 5.25" Winchester Drive. Included are removal and replacement procedures for major subassemblies and a description of the built-in diagnostics. The Winchester Drive requires no preventive maintenance and has no adjustments.

8.4.1 Diagnostics

All diagnostics are divided into three sections: (1) Power-Up Diagnostics; (2) Operational Error; (3) Fault Diagnostics.

8.4.1.1 Power-Up Diagnostics

During the power-up sequence in the Drive, a number of automatic diagnostic routine sequences are performed before the Drive becomes ready for system usage. When a fault occurs, an appropriate error code is displayed in the fault indicators. Table 8-14 lists the description of these tests and the applicable error code.

The Power On LED is used to flash error messages when fault conditions occur in the Drive. A 4-bit binary code is used (long flash = logic 1; short flash = logic 0) with the most significant bit occuring first (e.g., short, short, long, long = 0011 = 3).

		Table 8-14. Power-Up Sequence Error Codes
ERR	OR CODE	ERROR DESCRIPTION
1	(0001)	No index track data burst at track 2 or track 3
2	(0010)	No flag 0 from track 00 detector
3	(0011)	Motor speed exceeds <u>+</u> 1% tolerance
5	(0101)	Flag 0 always true
9	(1001)	Single-chip microcomputer self-test failed
10	(1010)	No Index
11	(1011)	Motor not up to speed

The power-up sequence error codes are detailed in the following paragraphs.

<u>Codes 9, 10 and 11</u> - The first check is a self-test of the single-chip microcomputer. A checksum is performed on all the code bytes, and failure results in the display of fault code 9. Following the self-test, the microcomputer checks for an Index pulse (Hall sensor output) from the dc motor. If this does not occur during a period of 8 seconds, then fault code 10 is displayed. Since this condition is likely to be the result of the dc motor not starting, the microcomputer attempts to reduce head/disk static friction (during a period of 8 seconds) by moving the positioner four times (one track in alternate directions).

The dc motor speed then is checked to determine whether it is within + 1% of 3,600 rpm. Each check takes one motor revolution, and during this time the Power On LED is flashed at intervals of approximately 0.5 seconds. If the microcomputer does not see four consecutive speed samples correct to +1%, within 25 seconds, it will display fault code 11.

<u>Codes 5 and 2</u> - When the speed check is successfully completed, Write Fault interrupts are enabled. The microcomputer then begins the recalibration of the actuator to track 00. Two possible halt codes may occur. If Flag 00 does not go false within 25 steps toward the center of the disk, fault code 5 will be displayed. After going false, if Flag 0 cannot then be set true within 512 steps in the out direction, fault code 2 is displayed.

<u>Codes 1 and 3</u> - After calibrating the actuator to track 00, the microcomputer initiates a routine to select the correct index pulse. The actuator is moved to track 2 to find the index data burst on head 0 and to select the corresponding Hall sensor phase, thus establishing Index. This task involves checking for the data burst on track 3, if it cannot be located in track 2. If link B is present, failure to complete this operation results in fault code 1 (but not when link B is cut). The actuator then is positioned on track 00, and a final check is made on the motor speed. If it is not within +1% tolerance, fault code 3 is displayed.

At the successful completion of the power-up routine, both Ready and Track 00 are set true, and the head selects are enabled.

8.4.1.2 Operational Error Check

During normal system usage and diagnostic self-testing, a number of built-in self-tests are performed. If any error conditions are detected by the microcomputer, an error code (as described in paragraph 8.4.1.1, above) is displayed by the Power On LED indicator. Table 8-15 lists the error codes and the tests.

Table 8-15. Operational Error Codes

```
ERROR CODE ERROR DESCRIPTION
```

- 4(0100) Motor speed exceeds +10%, -5% tolerance
- 6(0110) Step pulse while Write Gate is true
- 7(0111) Static Write Fault condition:
 - 1. Write current and no Write Gate, or
 - 2. No write current, no Write Gate, or
 - 3. More than one read/write head selected, or
 - 4. 12 volt supply below 10.3 volts, or
 - 5. 5 volt supply below 4.5 volts

The operational error codes are detailed in the following paragraphs.

<u>Codes 4 and 6</u> - While waiting for a step pulse from the interface, the microcomputer is continually monitoring the dc motor speed. Should the speed vary from nominal by more than +10% or -5%, fault code 4 will be displayed. The microcomputer will not allow a step pulse to be received while Write Gate is true. This a considered a catastrophic controller fault. The Drive returns to Write Gate status, displaying fault code 6.

<u>Code 7</u> - On receipt of a Write Fault interrupt from the Drive's hardware detection circuitry, the microcomputer latches the interrupt and delays for 2 seconds. It then samples the hardware input to check whether the Write Fault condition still exists. If it does, fault code 7 is displayed; if it does not, the microcomputer enters the power-up routine, thus setting the actuator to track 00.

8.4.1.3 Fault Diagnostics

Table 8-16 shows the likely causes and corrective action for power-up sequence and operational faults. The simplest action is to remove and replace either the Master Electronics PCBA or the Motor Speed Control PCBA and then recheck the fault code display.

Table 8-16. Fault Diagnostics

FAULT CODE	PROBABLE CAUSE	CORRECTIVE ACTION
1	Fault in data burst detection circuitry	Replace Master Electronics PCBA
	Fault in head 0 or preamp PCBA	Replace the preamp PCBA (not recommended)
2,5	Transit lock label not removed	Remove
	Connector fault between Motor Speed Control PCBA and step- per motor/flag 0 assembly	Check connector or replace PCBA
	Short circuit between Motor Speed Control PCBA and casting	Reinstall PCBA
	Fault in stepper motor control circuitry	Replace the Master Electronics PCBA or the Motor Speed Control PCBA
3,4	Brake failure	Replace
10,11	No 12 volt supply	Check supply and connector
	Faulty Motor Speed Control PCBA	Replace
6	Controller (WDC) interface fault	Check WDC and connectors
	Faulty Master Electronics PCBA	Replace
7	Faulty Master Electronics PCBA	Replace
	Faulty preamp PCBA	Replace (not recommended)
	5 volt or 12 volt supply too low	Check supply
9	Faulty single-chip micro- computer	Replace Master Electronics PCBA

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In practice, however, the most likely sources of trouble are (a) power supplies out of tolerance and (b) step rates out of the Drive constraints. In any case, the following should be verified:

- 1. The connectors are clean and properly attached.
- 2. Link A is removed for the 3.1-millisecond to 8.0-millisecond range.
- 3. The Drive chassis is free of any system metalwork.
- 4. The dc power lines are short twisted pairs.
- 5. Data and control cables are properly shielded and do not run close to high current switching circuits.

8.5 REMOVAL AND REPLACEMENT PROCEDURES

The following paragraphs detail the removal and replacement procedures for the major subassemblies. Be sure to read each procedure before attempting removal or replacement.

There is no preventive maintenance on the Drive, and there are no adjustments.

Field repair is restricted to replacement of the Master Electronics PCBA, the Motor Speed Control PCBA, the Brake Assembly and the Head Disk Assembly.

NOTE

Repair of the Head Disk Assembly can be effected only by the use of Ampex special tooling and under Class 100 cleanroom conditions.

The tools required for field repair consist of the following:

- a. Pozidrive screwdriver, No. 2
- b. Phillips head screwdriver, medium
- c. Hex driver, Allen, 5/64 inch
- d. Slot screwdriver, medium

8.5.1 Master Electronics PCBA Removal and Replacement

- Remove the three (3) cable connections at the bottom rear of the Winchester Drive (PI [Drive Control], P2 [Drive Data], P3 [Power]. See figure 8-12.
- Remove the four (4) shock mount plate screws, located on the bottom of the Drive. See figure 8-13.

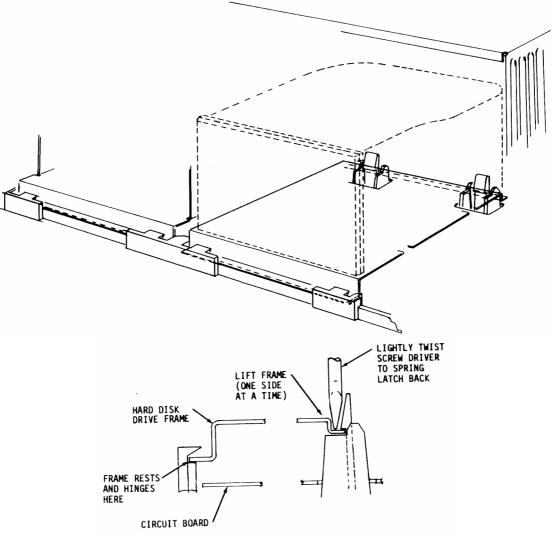


Figure 8-12. Winchester Drive Assembly

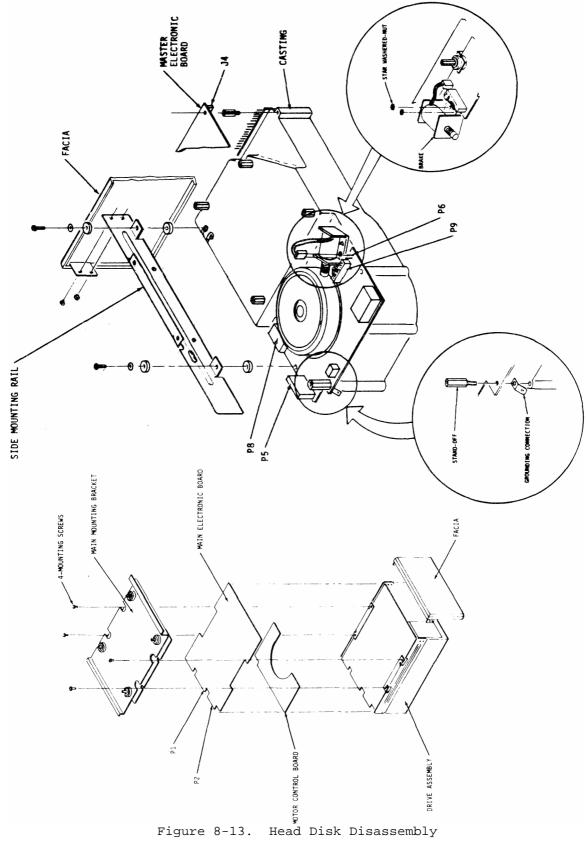


Figure 8-13.

- Remove the front facia by removing two (2) top and two (2) bottom mounting screws (Phillips head). See figure 8-13.
- 4. Using the Allen hex drive, remove the six (6) screws securing the Master Electronics PCBA to the Drive. Carefully loosen connector J4 from the Preamplifier PCBA, and remove the Master Electronics PCBA.
- 5. Disconnect flat cable connector J5 from the Motor Speed Control PCBA.
- 6. To replace the Master Electronics PCBA, connect flat cable connector J5 to the Motor Speed Control PCBA, ensuring that the connector is properly polarized.
- 7. Ensure that connector J4 mates properly with the Preamplifier PCBA.
- 8. Secure the Master Electronics PCBA to the Drive with six (6) screws.
- 8.5.2 Brake Removal and Replacement
 - 1. Remove the Master Electronics PCBA as described in paragraph 8.5.1.
 - 2. Disconnect brake connector J6 from the Motor Speed Control PCBA.
 - 3. Using the box spanner, remove the two nuts securing the brake to the casting, and remove the brake.
 - 4. To replace the brake, position the replacement brake, and refit the nuts loosely.
 - 5. Place the feeler gauge between the motor rotor and the brake pad, and push the brake body so that the plunger is fully depressed against its spring.
 - 6. Ensure that the center line of the brake lines up with the motor center, and lock the nuts.
 - 7. Reconnect the Power connector, ensuring correct polarization.

WARNING

Before powering up the Drive, make sure the motor is free of obstructions. Do not touch the spinning motor.

- 8. Power up the Drive with the Master Electronics PCBA lying alongside, and verify that the brake does not contact the motor rotor. Ensure that the Master Electronics PCBA is isolated from metallic parts.
- 9. Turn the power off, and verify that stopping time is within 5 to 8 seconds.
- 10. Refit the Master Electronics PCBA, as described in paragraph 8.5.1.

8.5.3 Motor Control PCBA Removal and Replacement

- 1. Remove the Master Electronics PCBA, as described in paragraph 8.5.1.
- 2. Disconnect brake connector J6, dc motor connector J9 and stepper motor connector J8 from the Motor Speed Control PCBA.
- 3. Unscrew both the rear standoff with ground tab and left standoff; remove the Motor Speed Control PCBA.
- 4. If the spare Hall element is to be connected, remove the link on the Motor Speed Control PCBA, and reconnect it as shown on the Motor Speed Control PWBA Assembly Drawing.
- 5. To replace the Motor Speed Control PCBA, install the replacement Motor Speed Control PCBA, insert the ground tab, and tighten the rear stand-off. Insert and tighten the left standoff.
- 6. Reconnect stepper motor connector J8, dc motor connector J9 and brake connector J6, ensuring correct polarization of the connectors.
- 7. Refit the Master Electronics PCBA, as described in paragraph 8.5.1.

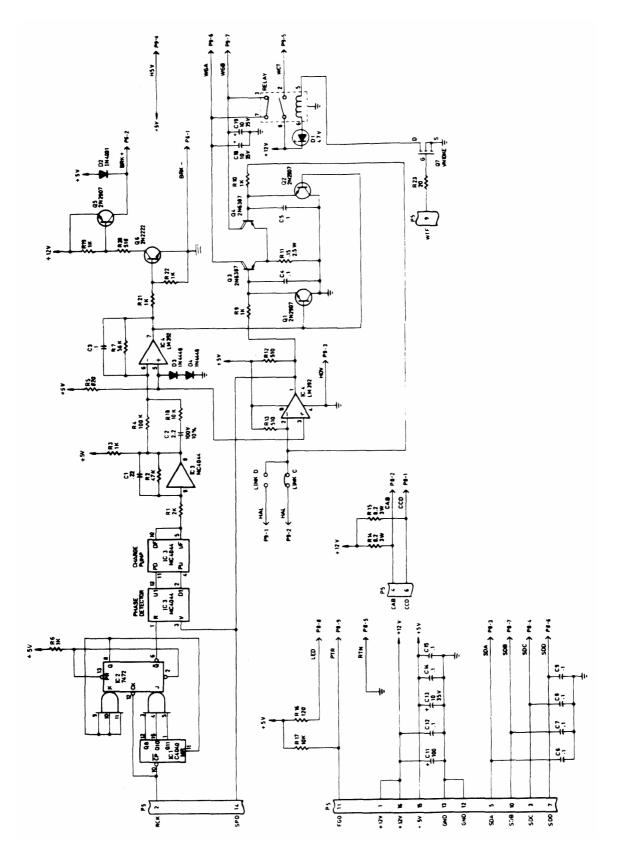
8.5.4 Preamplifier PCBA Removal and Replacement

(Not recommended as field replaceable)

8.6 PARTS LIST

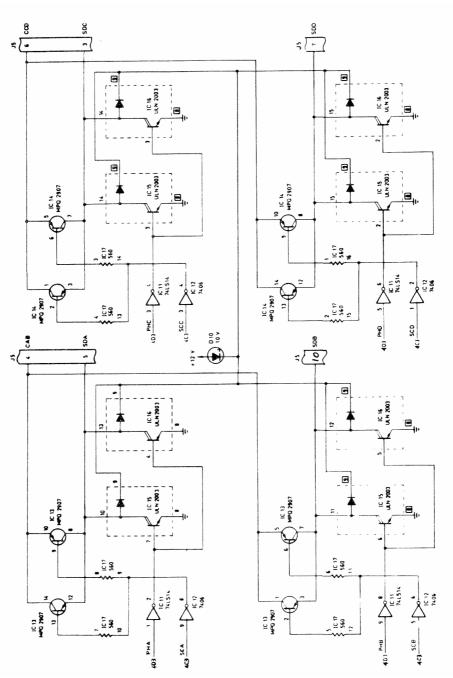
Table 8-17 is a listing of field replaceable parts for replacing failed subassemblies.

ICN	VENDOR PART NUMBER	DESCRIPTION
TT524100	400413-002	5-1/4" WINCHESTER DISK DR., 20MB
TT520100	ASY5023	PCBA, MASTER ELECTRONICS
TT520110	ASY5024	PCBA, MOTOR SPEED CONTROL
		PCBA, WINCHESTER DRIVE CONTROLLER
		PCBA, WDC BUS ADAPTOR
TT528160	TAB1004	GROUND TAB

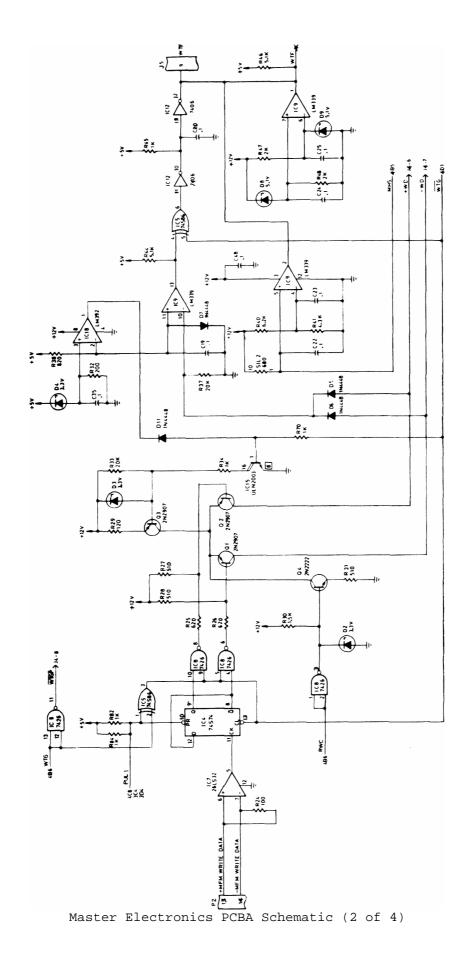


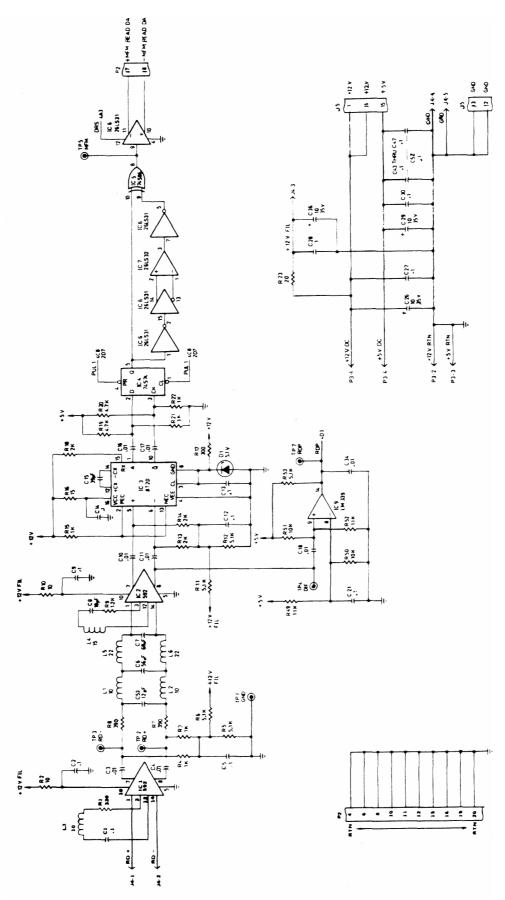
Motor Speed Control PCBA Schematic

3-53

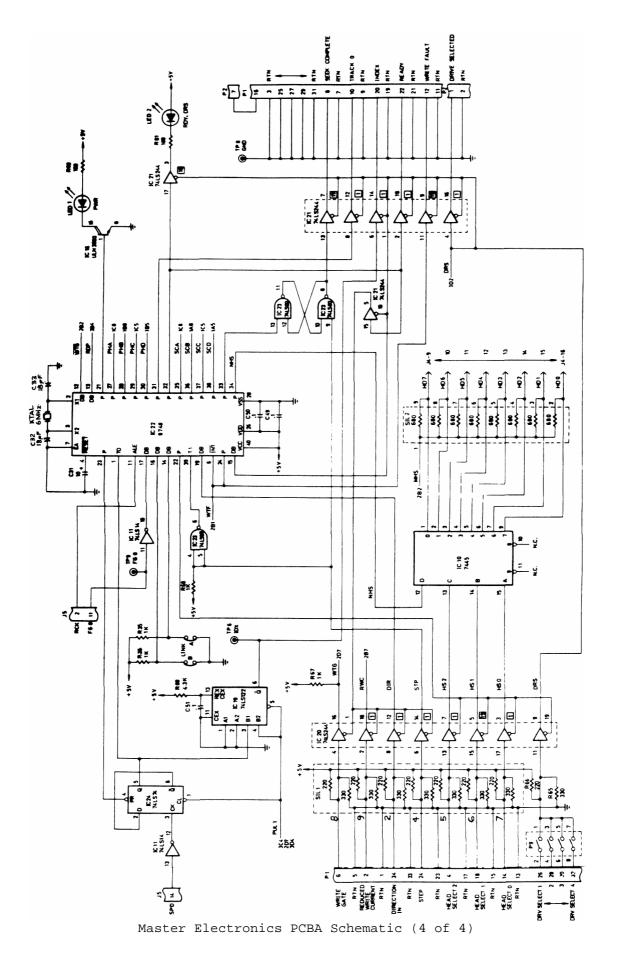


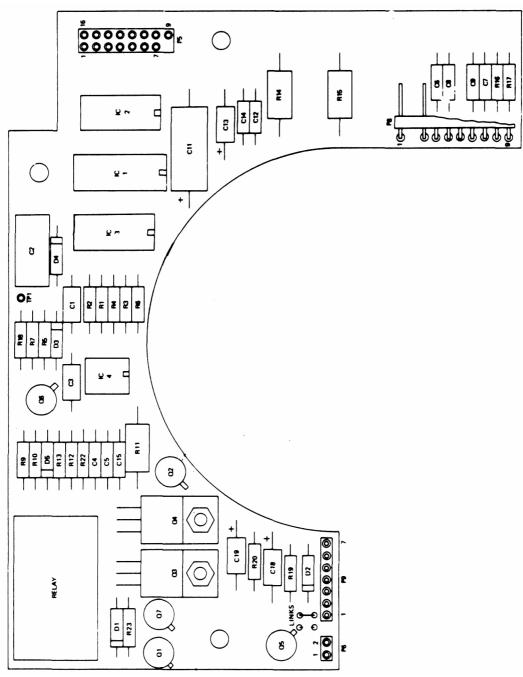
Master Electronics PCBA Schematic (1 of 4)



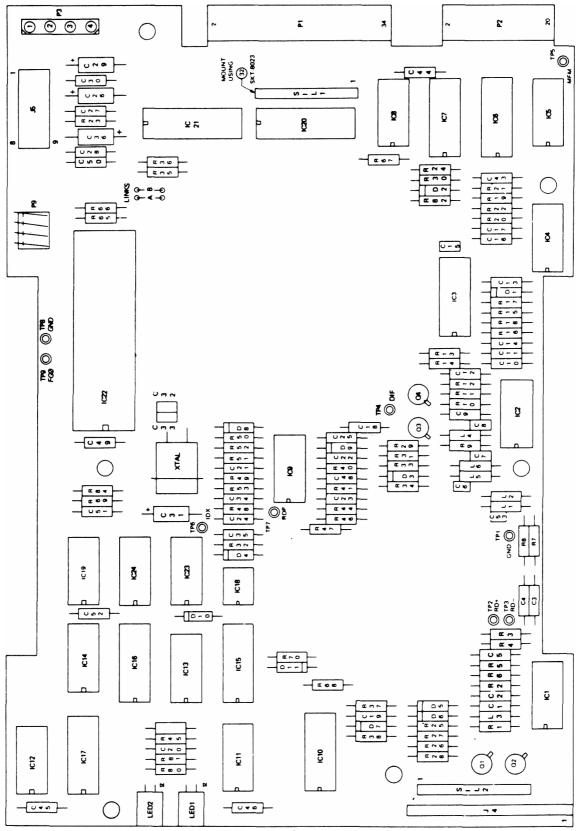


Master Electronics PCBA Schematic (3 of 4)





Motor Speed Control PCBA Layout



Master Electronics PCBA Layout

SECTION IX

50 MEGABYTE WINCHESTER DRIVE SYSTEM

9.1 INTRODUCTION

This section provides maintenance personnel with information necessary to install, operate and maintain the 50 MB, 5 1/4-inch, Winchester Drive system.

Section IX is arranged in three subsections. The scope of each subsection is escribed as follows:

- 9.1 INTRODUCTION contains general information, physical and electrical descriptions and equipment specifications.
- 9.2 INSTALLATION AND OPERATION contains information to enable maintenance personnel to inspect and install the Winchester Drive system, and includes information on the Winchester Drive Controller (WDC) and WDC Bus Adapter PCBAs. Instructions for the installation of jumpers and the setting of switches are also included.
- 9.3 FUNCTIONAL DESCRIPTION explains drive and Controller operation and gives a detailed description of each function.

9.1.1 General Description

The 50 MB Winchester Drive is a fixed-media, magnetic, rotating, data storage evice. Its purpose is to allow the Model 4108 Base Unit to store and retrieve locks of data (records) onto and from rotating disks, thus providing storage for the MAI® 2000 Series Computer System. The drive functions as an input/output device in the Base Unit.

The 50 MB Winchester Drive contains four magnetic disks and has a total data storage capability of 42.07 megabytes, formatted. Access to data is provided by one moving head per disk surface. The heads are an integral part of the Head Disk Assembly (HDA) and never require alignment in the field. Data is recorded on the disk surfaces using modified frequency modulation (MFM) techniques.

The Winchester Drive incorporates a balanced, rotary, voice coil/swing arm motor positioning system. The major components of the drive are explained in the following paragraphs.

Head Disk Assembly - The Head Disk Assembly is a completely sealed module that houses the read/write heads, disks, positioner assembly, voice coil/swing arm motor and filters. The spindle-mounted disks are rotated by the dc motor as the read/write heads "fly" over the surface of the disk. The voice coil/swing arm motor positions the heads over the disk, using positioning information from a microprocessor. Within the sealed module, air movement generated by disk rotation causes air to flow from the disk chamber (upper chamber), through an aperture, into the drive chamber (lower chamber) and return via a 0.3-micron recirculating filter. DC Motor and Brake - The dc motor is a brushless, direct-coupled, twophase external rotor motor with integral hub. Commutation is effected by three Hall-effect sensors mounted within the drive motor assembly. The rotational speed of the motor is 3600 revolutions per minute (rpm). The disk hub is grounded to the Device Electronics PCBA via the motor shaft and a button contact. The brake is a plunger-solenoid designed to stop the motor in 20 seconds and to provide a restraining torque during handling.

Disk Electronics - The disk electronics consists of three standard printed circuit board assemblies (PCBAs): the Device Electronics PCBA; the Preamplifier PCBA; and the Motor Control PCBA.

Power Supply - The dc supply voltages (+12 and +5 volts) to the Winchester Drive are supplied by the Base Unit Power Supply and are input to the Drive on connector J3.

9.1.2 Functional Concepts

The simplified block diagram in figure 9-1 shows the functional concepts of the Winchester Drive, which are described in the following paragraphs. Additional detailed explanations of these logic areas are presented in paragraph 9.3.

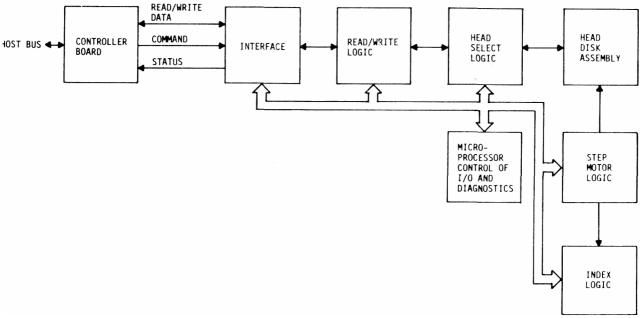


Figure 9-1. Simplified Block Diagram

<u>Interface logic</u> - The drive interface logic translates the input/output signals of the Winchester Drive to ensure drive-to-controller signal compatibility. Drive I/O logic signal levels are transistor-transistor logic (TTL) compatible. The transmission line signals are differential signals.

<u>Read/Write Logic</u> - To execute read or write commands, the drive must be free of faults, and the selected head must be at the correct location on the disk (i.e., "on cylinder"). During a read command, the read/write logic recovers data from the disk, processes the data, and transfers the data to the Winchester Drive Controller (WDC) board, in the Base Unit. During a write command, the read/write logic receives data from the WDC, processes the data and writes the data onto a disk.

 $\underline{\text{Head Select Logic}}$ - The head select logic receives and decodes the addresses of a specific head.

<u>Voice Coil/Swing Arm Motor Logic</u> - A voice coil/swing arm motor is used to controltheread/write heads in the proper sequence at a rate and direction determined by a single-chip microcomputer. Position reference is made to tracks recorded on a dedicated servo surface on the disk nearest the drive motor.

<u>Index Logic</u> - The square wave output of the Hall sensor in the dc motor is processed to produce a pulse every disk revolution. This pulse is used as an interface signal to mark a fixed reference point relative to the disk.

<u>Winchester Drive Controller</u> - The Winchester Drive Controller PCBA uses the Shugart Associates System Interface (SASI). It communicates with the Central Microprocessor Board (CMB) global bus via the WDC Bus Adapter PCBA. Together, these two boards interface the Winchester Drive to the CMB. The Winchester Drive Controller PCBA is mounted above the component side of the WDC Bus Adapter PCBA.

9.1.3 Equipment Specifications

Performance characteristics for the 50 Megabyte Winchester Drive are listed in table 9-1.

Table 9-1. Specifications

PARAMETERS

CHARACTERISTICS

Storage Capacity	
Unformatted	
Disks per drive	4
Data surfaces/heads	б
Data bytes per track	10,416
Tracks per drive	4,980
Capacity (megabytes)	51.9
Number of cylinders	830

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Table 9-1. Specifications (continued) PARAMETERS CHARACTERISTICS Storage Capacity Formatted (33 sectors) Data bytes per sector 256 Data bytes per track 8,448 Capacity (megabytes) 42.07 MBytes per surface 7.01 Recording Parameters Bit density 9,077 bpi (inner track, nominal) Coding Modified-frequency-modulation (MFM) Track density 960 tracks per inch (average) Rotational Parameters Disk rotational speed 3,600 (+0.5%) rpm Data transfer rate 5 megabits per second Seek Time Track-to-track 6 milliseconds Average 30 milliseconds One-third stroke 33 milliseconds 60 milliseconds Maximum Rotation Latency Average 8.33 milliseconds Maximum 16.67 milliseconds (nominal) Start Time 25 seconds maximum to Drive Ready Stop Time 20 seconds maximum Error Rates The following error rates are valid only when the drive is being used according to specifications. Media defects or equipment failures are excluded. Written data should be verified as being correctly written. Seek errors 1 in 1,000,000 seeks 1 in 10,000,000,000 bits Recoverable read errors Nonrecoverable read errors 1 in 1,000,000,000,000 bits

Table 9-1. Specifications (continued)

PACKAGED	UNPACKAGED	OPERATING
Temperature:		
-40°F to 149°F -40°C to 65°C	-40°F to 149°F -40°C to 65°C	50°F to 115°F 10°C to 46°C
Temperature Gradient:		
43.2°F per hour 24°C per hour	43.2°F per hour 24°C per hour	3.6°F per 5 minutes 2°C per 5 minutes
Humidity:		
10-80% RH no condensation	10-80% RH no condensation	10-80% RH no condensation
<u>Altitude</u> :		
-1,000 to 50,000 feet	-1,000 to 50,000 feet	-200 to 7,000 feet
<u>Vibration</u> :		
<pre>0.2 inches peak-peak displacement (5 Hz to 10 Hz). 1 G peak (10 Hz to 44 Hz). 0.01 inches peak-peak displacement (44 Hz to 98 Hz). 5 G peak (98 Hz to 300 Hz).</pre>	<pre>0.02 inches peak- peak displacement (5 Hz to 31 Hz). 1 G peak (31 Hz to 69 Hz). 0.004 inches peak- peak displacement (69 Hz to 98 Hz). 2 G peak (98 Hz to 300 Hz).</pre>	0.006 inches peak- peak displacement (5 Hz to 60 Hz). 0.5 G peak (40 Hz to 300 Hz).
Shock:		
Will withstand a drop of 36 inches. 1/2 50 G maximum, 20 milli- seconds duration, 1/2 sinusoidal 1/2	Will withstand a drop of 0.75 inches. 1/2 sinusoidal: 40 G maximum, 5 milli- seconds duration; 20 G maximum, 100 milli-	<pre>3.0 g, peak, 5 milli- seconds duration, sinusoidal. 1 G peak, 20 milli- seconds duration, sinusoidal</pre>
	seconds duration	

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9.2 INSTALLATION AND OPERATION

This subsection contains unpacking, installation and checkout information for the 50 Megabyte Winchester Disk Drive.

9.2.1 Unpacking

Prior to unpacking the drive, inspect the packaged drive to determine whether any damage was incurred during shipment.

- Using the shipping documents, verify that all items have been received.
- 2. Open the protective shipping carton at the top.
- 3. Remove the drive from the shipping carton.
- 4. Remove the plastic cover.
- 5. Inspect each package article to determine whether any damage was incurred during shipment.
- 6. Verify that connectors, indicators and protruding parts are undamaged.
- 7. Check the ID nameplate against the shipping papers to verify that the drive part number and serial number are correct.
- 8. When practical, store shipping containers for reuse.
- 9. Record any damage, and report damage to the applicable carrier.

9.2.2 Equipment Placement

Equipment placement consists of mounting the drive in the Base Unit, installing the Winchester Drive Controller (mounted atop the WDC Bus Adapter PCBA), and routing the input/output and power cables.

9.2.3 Shipping Lock (Read/Write Heads)

The voice coil/swing arm motor positioner latch is fixed in place automatically through a relay. The latch prevents movement of the read/write heads across the disk surface during shipment or other movement.

9.2.4 System Installation

Installation of the 50 Megabyte Winchester Drive system consists of plugging the WDC PCBA/WDC Bus Adapter PCBA combination into the Central Microprocessor Board, in the Base Unit, and then routing the Winchester Drive cables to the WDC and the power supply and connecting them. All components required to interface the 50 Megabyte Winchester Drive to the Central Microprocessor Board are included. Detailed installation procedures are provided in the following paragraphs.

9.2.5 Power and Interface Cables and Connectors

Electrical interface between the 50 Megabyte Winchester Drive and the WDC PCBA is accomplished via four connectors: Jl, J2, J3 and J4. The connectors and their mating connectors are shown in figure 9-2.

The signal interface connection is made through connectors Jl and J2 on the Device Electronics PCBA. Pin assignments for Jl, J2 and J3 are listed in table 9-2, 9-3 and 9-4.

Control signal Connector Jl is a 34-pin board-edge connector. The signals on Jl control the Winchester Drive and transfer status to the Winchester Drive Controller (WDC) PCBA.

Data transfer connector J2 is a 20-pin board-edge connector. The signals on J2 contain read or write data.

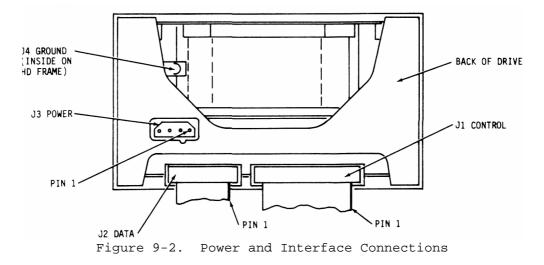
DC power connector J3 is a 4-pin keyed AMP connector, which delivers +5 volts and +12 volts to the drive.

Ground connector J4 connects the drive inner chassis ground to the system ground. J4 is located on the Head Disk Assembly, near the left-hand shock mount (as viewed from the rear of the drive).

9.2.6 Drive Addressing and Interface Termination

Figure 9-3 shows the locations of Drive Address jumpers W3, W4, W5 and W6 (for drive addresses 1, 2, 3 and 4) and Interface Terminator Pack RN1. Drive Address jumper W1 is used for write-fault latching, and W2 is reserved. Only one Drive Address jumper is installed on the drive, and it is addressed as drive 1 by the factory. Each Drive Select interface line connects the corresponding addressed drive to the Winchester Drive Controller PCBA.

In multiple drive systems, each drive must have its own unique address. Terminator Pack RN1 provides proper termination for the interface lines. When daisy-chaining multiple drives, the terminator is installed only in the last drive on the daisy chain.



	CTOR PIN Ground	SIGNAL NAME	SOURCE
2	1	Reserved	
4	3	Head Select 2*	WDC
6	5	Write Gate*	WDC
8	7	Seek Complete*	Drive
10	9	Track 00*	Drive
12	11	Write Fault*	Drive
14	13	Head Select 0*	WDC
16	15	Reserved	-
18	17	Head Select 1*	WDC
20	19	Index*	Drive
22	21	Ready*	Drive
24	23	Step*	WDC
26	25	Drive Select 1*	WDC
28	27	Drive Select 2*	WDC
30	29	Drive Select 3*	WDC
32	31	Drive Select 4*	WDC
34	33	Direction In*	WDC

Table 9-2. Control Signal Connector Jl Pin Assignments

* Signal level is low true.

Table 9-3. Data Transfer Connector J2 Pin Assignments

-		
J2	CONNECTOR	PIN

	Ground	SIGNAL NAME	SOURCE
1	2	Drive Selected*	Drive
3	4	Reserved	_
5	б	Reserved	_
7	8	Reserved	_
9	10	Reserved	
_	11	Ground	_
	12	Ground	
13	_	MFM Write Data+	WDC
14	_	MFM Write Data-	WDC
_	15	Ground	_
_	16	Ground	_
17	-	MFM Read Data+	Drive
18	_	MFM Read Data-	Drive
	19	Ground	
	20	Ground	

* Signal level is low true.

Table 9-4.	DC Power	Connector	J3 Pin	Assignments
J3 PIN			VOLTAG	E
1			+12VDC	
2			+12V RE	TURN
3			+5V REI	URN
4			+5VDC	

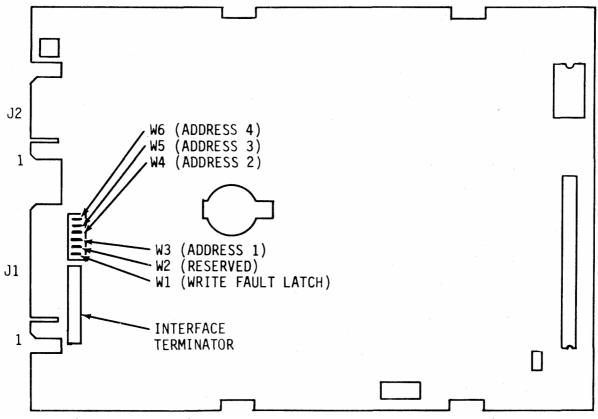
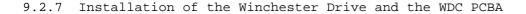


Figure 9-3. Drive Address Jumpers and Interface Terminator



To install the 50 Megabyte Winchester Drive system, proceed as follows:

- 1. Turn the Base Unit power OFF.
- 2. Insert a screwdriver, or similar device, into the slot at the bottom right-hand side of the Base Unit cover, and push in to disengage the the plastic latch. Repeat with the left-hand side, and remove the cover.
- 3. Remove the Memory Array PCBAs, located in the front right-hand corner of the CMB, by simply lifting the "stack" of PCBAs away from the CMB, unplugging the bottom memory array PCBA from the CMB.
- 4. Remove the front facia by pulling up slightly on the plastic card holder until the facia is disengaged from the card holder.
- 5. If the WDC PCBA is already installed in the Base Unit, continue with step 13.

6. Examine the new WDC PCBA and verify that the jumpers listed below are not installed, for normal operation. See figure 9-4 for the location of the jumpers.

Jumper A to BJumper E to FJumper 0 to PJumper C to DJumper G to H

- 7. If the WDC PCBA is already attached to the WDC Bus Adapter PCBA, continue with step 12.
- Set the appropriate switches on the WDC Bus Adapter PCBA for the correct bus arbitration number according to the listing shown below. See figure 9-4 for the location of the switches.

SWITCH SW1

Bus Arbitration							
<u>S1</u>	<u>S2</u>	<u>S3</u>	<u>S4</u>	<u>S5</u>	<u>S6</u>	<u>87</u>	<u>58</u>
OFF	OFF	OFF	ON	ON	ON	DON ' T	CARE

- 9. Lower the WDC PCBA onto the WDC Bus Adapter PCBA so that the Winchester Drive connectors (JO, Jl, J2, J3) are facing power connector J4 (on the Bus Adapter PCBA) and the four standoffs enter the holes in the WDC PCBA. Push down on each corner of the WDC PCBA until the retainers on the standoffs hold it securely in place.
- 10. Plug the ribbon cable coming the WDC Bus Adapter into connector J4 on the WDC PCBA.
- 11. Plug the 4-pin power connector coming from the WDC Bus Adapter into J3 on the WDC PCBA.
- 12. Plug the WDC Bus Adapter PCBA into the Central Microprocessor Board (CMB), or into the PCBA on the top of the "stack," at the rear right-hand corner of the CMB.
- 13. Lower the Winchester Drive chassis into position on the CMB.
- 14. Pull the drive slightly to the front of the CMB so that the flange at the bottom of the drive chassis enters the slot in the Base Unit front panel.
- 15. Connect the 4-pin power plug to the connector located at the bottom left-hand corner of the drive chassis (as viewed from the rear of the drive), on the Head Disk Assembly.
- 16. Lower the back of the drive chassis so that it pushes back the two (2[^] plastic latches on the CMB at the bottom rear of the drive. The drive chassis will "snap" in place.
- 17. Plug the ribbon cables from the Winchester Drive into the WDC PCBA. (Note: the two narrower ribbon connectors on the WDC PCBA are situated side by side; the right-hand connector [J0] receives the "0" cable, and the left-hand connector [J1] receives the "1" cable.)

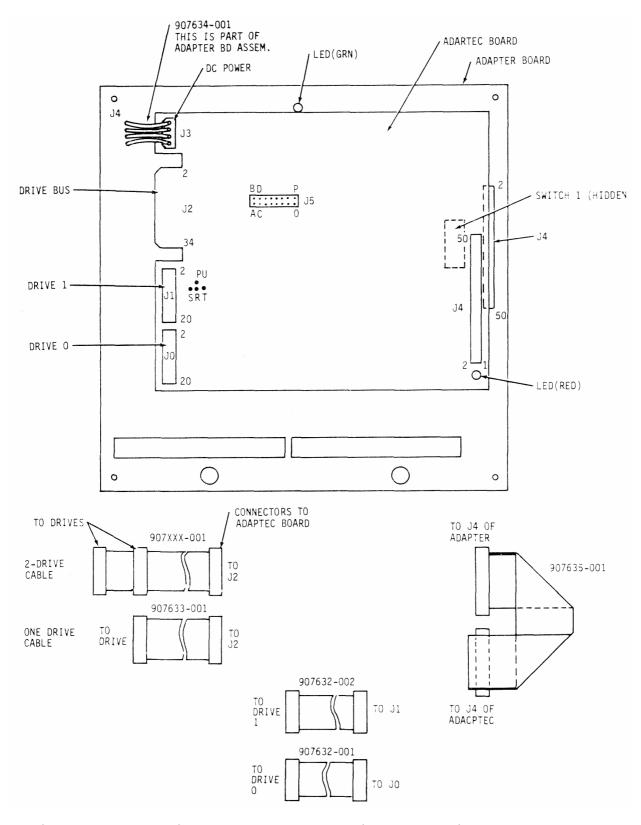


Figure 9-4. Location of Jumpers on the Winchester Drive Controller PCBA

- 18. Replace the front facia by reversing the removal procedure.
- 19. Reinstall the Memory Array PCBAs into the card cage at the front right-hand corner of the CMB by plugging the bottom PCBA into the CMB. (The entire stack may be reinstalled as a unit.)
- 20. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to snap into place.
- 21. Plug in all connections to the Base Unit, including all previously attached peripherals.

9.2.8 Operation

Operating instructions consist of indicator functions, power-on/off procedures and voltage checks.

<u>Indicators</u> - When lit, the LED, located on the bezel, indicates the drive has been selected by the Central Microprocessor Board and that the drive is ready.

<u>Power-On Procedures</u> - The Winchester Drive requires +12 volts and +5 volts dc source power, and these voltages are measured at drive connector J3. During seek, the drive takes 2.8 amperes at +12 volts, dropping to 1.8 amperes while idling. For power-up or power-down sequences, the +12 volt and +5 volt supplies may be applied or removed in any order. However, the rise time of the +5 volts must be less than 50 milliseconds for proper operation of the power-on reset circuits.

On power-up the drive performs an automatic recalibration sequence, which includes a disk speed check, accurate to +0.5% of nominal; a seek to track 00; and an index pulse selection. The Central Microprocessor Board uses status READY to sense the completion of this sequence. The time until READY turns true is typically 20 seconds after application of power.

<u>Power Supply Checks</u> - The following loads are used to check the power supplies. For the 12 volt supply, the power-up current is measured using a standard load of 3 ohms in parallel with 1 millihenry, and the operating current is measured using 5 ohms in parallel with 1 millihenry. With a 7 ohm resistive load on the 5 volt supply, and the aforementioned loads on the 12 volt supply, noise and ripple should be no more than 100 millivolts peak-to-peak, up to 500 Hz; and 50 millivolts peak-to-peak, from 500 Hz to 5MHz. The power requirements of the 50 MB drive are listed in table 9-5.

	Table 9-5.	Power Requirements	
VOLTAGE (VDC)	TOLERANCE	NOMINAL CURRENT	MAXIMUM CURRENT
+5	<u>+</u> 5%	0.9A	0.9A
+12	<u>+</u> 5%,	1.8A	3.7A

9.3 FUNCTIONAL INSCRIPTION

The following paragraphs describe the theory of the various electronic subsystems that comprise the 50 Megabyte 5.25" Winchester Drive. This information provides maintenance personnel with a comprehensive understanding of the functions of the drive.

A brief discussion of disk recording principles is followed by a functional description of the Winchester Drive unit, explaining how the drive interfaces with the Winchester Drive Controller.

The interconnection of the major logic blocks is shown in figure 9-5.

9.3.1 Basic Disk Principles

The recording medium for the 50 megabyte drive is a stack of four 5 1/4-inch disks with six recording surfaces (see figure 9-6). Each disk is coated with a layer of magnetic oxide. The coating is burnished to a flatness that allows the read/write heads to "fly" in proximity to the surface without actual physical contact.

Data is recorded in serial fashion on concentric rings on each disk surface by holding the head in a fixed position over the rotating disk. (These rings are referred to as "tracks." The disk drive unit positions the heads precisely over the tracks. Corresponding track positions, both upper and lower on each disk, are referred to as one "cylinder" of data.)

A center-tapped coil is mounted on the core of the read/write head to perform the read/write function. The recording flux direction is controlled by energizing the center tap connection, causing current to flow through the bifiler winding from the center tap to either one end or the other. When reading, the ends of the coil are switched to the input of the read amplifier. Data is erased by writing new data on the track. The read/write coil is mounted onto the core of the ferrite slider.

As the disk rotates, it creates an "air bearing" around its surface. This air bearing moves under the slider and exerts an upward force on the shoe. A downward pressure is placed on the slider by the spring flexure of the head. Supported by carefully balanced aerodynamic forces, the head shoe then flies at a point where the downward force of the load spring is equal in force to the air pressure under the head. The slider's flying height is influenced, in part, by the air-bleed channel in the middle of the slider. This channel allows some air to bleed from under the slider, decreasing the air pressure. This, in turn, allows the head to fly closer to the disk surface.

The slideris mounted to the head arm assembly via a spring gimbal-mount. This allows the flying attitude of the slider to vary slightly so that it can follow minor surface variations without contacting the disk surface. As the disk starts, or stops, the head takes off from, or lands in, a silicone-lubricated landing area. When the disk is not spinning, the head rests on, and actually contacts, the landing zone on the disk.

All heads are mounted on a carriage such that the heads and carriage move as one unit. The carriage moves the heads radially over the disks' surfaces. All the heads are positioned at the same cylinder at any given time.

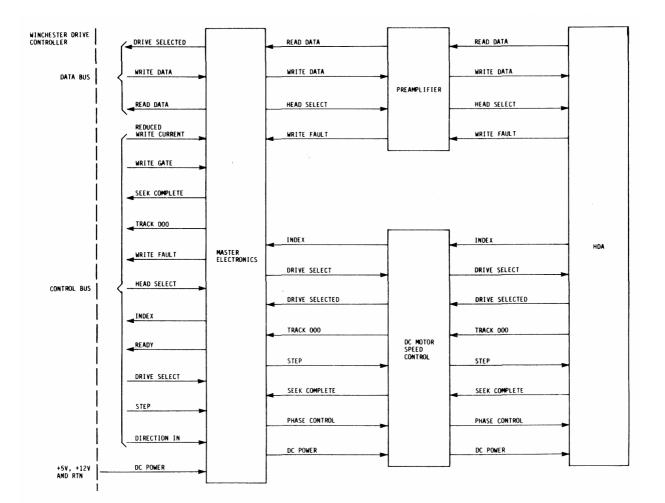


Figure 9-5. Winchester Drive Block Diagram

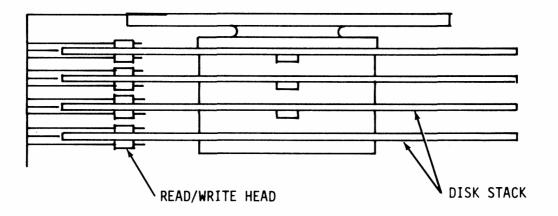


Figure 9-6. Surface and Head Geometry

9.3.2 Control Lines

The control data is exchanged between the Winchester Drive and the Winchester Drive Controller board (WDC), on the Central Microprocessor Board, via a control cable. The following paragraphs define each control line interface signal.

Write Gate - When true, the Write Gate signal from the WDC enables the current source and Write drive signals. When false, this signal enables Read Data to be transferred from the drive to the WDC.

Seek Complete - The Seek Complete status signal is generated by the microprocessor in the Device Electronics PCBA. Seek Complete occurs when the value of an internal 8-bit counter equals the desired number of track changes (determined by the Step and Direction In input signals).

Track 00 - The Track 00 status line is set true when the read/write heads are positioned over track 00.

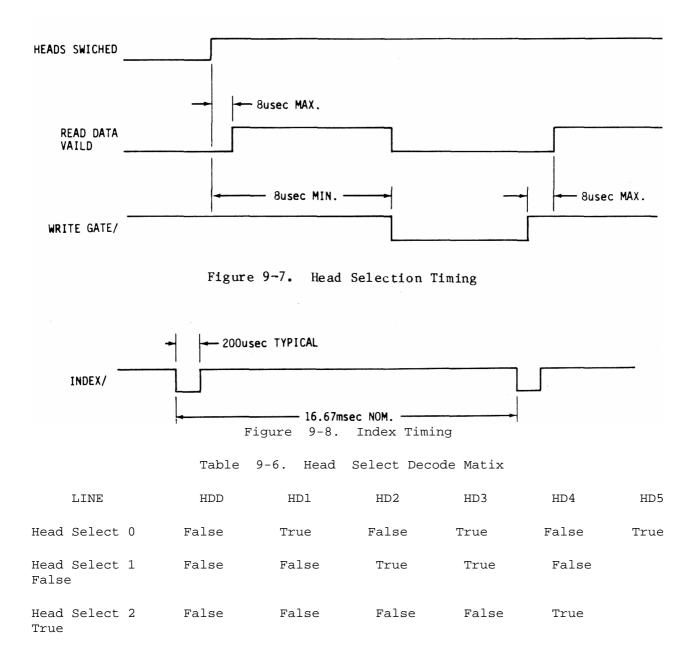
Write Fault - The Write Fault signal is true under the following fault conditions:

- a. Shorted head or open head
- b. No Write Data transitions
- c. No Write current
- d. The 5 volt supply is below 4.5 volts.
- e. Motor speed exceeds +1% tolerance after the power-up sequence is completed.
- f. Write Gate is true while Seek Complete is false, or the heads are not positioned at nominal track center.
- g. Power dc voltages are out of tolerance.
- h. Correct spindle speed cannot be reached or maintained.
- i. Servo fault prevents the completion of a seek operation.

Fault conditions g, h and i signal a serious malfunction. The positioner retracts, the spindle motor shuts down, and the Ready signal goes false.

When jumper Wl is installed, faults are latched until they can be cleared by a select-to-deselect transition lasting no less than 50 microseconds in each state. When Wl is out, fault conditions are not latched. A Write fault caused by an out-of-tolerance dc voltage is reset automatically when the voltage is restored to nominal.

Head Select - Up to six read/write heads may be selected using a 3-bit code on the Head Select 0, Head Select 1 and Head Select 2 lines. Table 9-6 is a head select matrix showing the logic level required on each Head Select line to select the desired read/write head. The head selection timing diagram is shown in figure 9-7.



Index - The Index signal is a 200-microsecond output pulse used to mark a fixed reference point relative to the disk. Figure 9-8 shows the Index timing.

Ready - The Ready signal is true when the Drive is ready to read or write (with or without an implied seek) and the other lines are valid. Ready remains true until power-off or until there is a Write Fault.

Drive Select - The Drive Select signal from the WDC corresponds with the Drive Select switch setting of the drive. If the Drive Select signal does not correspond, and the Ready signal is true, a Drive Select true signal is returned to the WDC, via the data lines.

Step - The Step signal pulse from the WDC is used in conjunction with the Direction In signal to move the read/write heads. This pulse input to the microprocessor is used to clock an internal 8-bit counter, which is reset

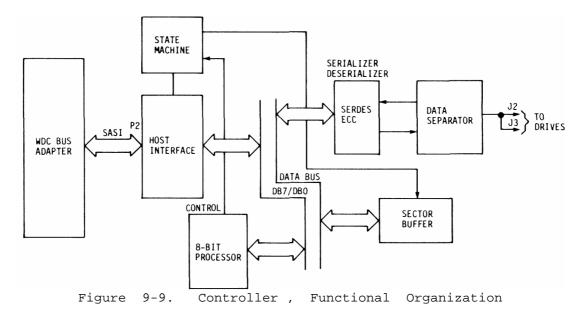
prior to each seek. Once the first step pulse is received, the drive immediately begins seeking. Additional pulses received before completion of the seek are buffered into the counter, and the heads move at a rate proportional to the Step pulse count.

Direction In - The Direction In signal from the WDC determines the direction of motion of the read/write heads. The microprocessor receives the first step pulse of a seek, samples the input and stores the result.

9.3.3 Winchester Drive Controller

The Winchester Drive Controller (WDC) operates in conjunction with an adapter board that permits the WDC to communicate with the Central Microprocessor Board global bus, via the SASI interface. The two boards are "piggybacked," with the WDC PCBA mounted above the component side of the WDC Bus Adapter PCBA. They are electrically interconnected by a 50-pin flat ribbon connector at J4 and by a 4-pin AMP connector at J3 (power). The simplified block diagram in figure 9-9 shows the functional organization of the WDC. Only the major areas are shown, and they are defined as follows:

- Host Interface The host interface connects the internal data bus to the WDC Bus Adapter PCBA. The state machine controls the movement of data and commands through the host interface.
- Processor The eight-bit microprocessor is the intelligence of the WDC. It monitors and controls the operation of the WDC.
- State Machine The state machine controls and synchronizes the operation of the host interface, serializer/deserializer (SERDES) and sector buffer.



- SERDES The serializer/deserializer (SERDES) converts parallel data from the internal data bus to serial data for transfer to a selected Drive. It converts serial data from the selected Drive to parallel data, which it places on the internal data bus.
- Data Separator The data separator converts serial TTL data to MFM for transfer to the selected Drive. It converts MFM data coming from the selected Drive to serial TTL data for the SERDES.
- Sector Buffer The sector buffer stages data transfers between the disk and the host to prevent data overuns. The sector buffer (FIFO) comprises 1K bytes of dual port RAM, for rapid data transfers. No sector interleaving is required.

9.3.3.1 Signal Definitions

Tables 9-7 through 9-11 list and define the signals that appear on the SASI bus ines between the WDC Bus Adapter and the Winchester Drive Controller.

The dash(-), or the lack of one, indicates the active state of a signal. The ctive state of a signal is that state which is required for a given operation. hen a dash is appended to the end of a signal name, the signal is active when t is low.

When no dash appears at the end of a signal name, the signal is active when it s high.

Some signal lines have two so-called active (or significant) states. When the evel on the line is high, a particular operation takes place. When the level on the line is low, a different operation occurs.

The following examples show the use of these conventions.

- BUSY- The signal BUSY- is active when it is at low level because it has the dash appended.
- BUSY The signal BUSY is active at a high level because it does not have the dash appended.
- C-/D The line C-/D (command-/data) has a dual purpose: the slash (/) indicates quality; that is, the dash after the C indicates that when this line is at a low level, command mode is indicated and when it is at a high level, data mode is indicated.

Other designations used to define signal lines are listed below.

- Drv Driver
- Rcvr Receiver
- OC Open collector
- Tri-State Line has three states: high, low, high impedance
- 220/330 Line termination: 220 ohms to source voltage/330 ohms to ground

Table 9-7. SASI Bus Status Signals

NAME DRV/RCVR DEFINITION

- I-/0 Drv OC Input-/Output: The controller drives this line. A low level on this line indicates that the controller is driving the data in on the SASI bus. A high level on this line indicates that the WDC Bus Adapter is driving the data out on the SASI bus. The WDC Bus Adapter monitors this line and uses it to enable and disable its data bus drivers. This signal is qualified by signal REQ-.
- C-/D Drv OC Control-/Data: This signal line indicates whether the information on the data bus consists of control or data bytes. A low means command bytes; a high means data bytes. This signal is qualified by signal REQ-.
- BUSY- Drv OC Busy: The controller generates this active low signal in response to the SEL- signal and the address bit (DBO- to DB7-) from the WDC Bus Adapter. The busy signal informs the WDC Bus Adapter that the controller is ready to conduct transactions on the SASI bus.

Table 9-8. Summary of SASI Bus Status Signals

I-/0 C-/D MSG- DEFINITION

DRV/RCVR

NAME

- High Low High The controller receives commands from the WDC Bus Adapter.
- High High The controller receives data from the WDC Bus Adapter.
- Low High High The controller sends data to the WDC Bus Adapter.
- Low Low High The controller sends an error status byte to the WDC Bus Adapter.
- Low Low Low The controller informs the WDC Adapter that it has completed the current command.

Table 9-9. Controller - Host Handshaking

DEFINITION

REQ- the	Drv OC	Request: The controller sends this active low signal to
		WDC Bus Adapter for each byte transferred across the inter- face. This signal qualifies signals I-/0, C-/D and MSG

ACK- Rcvr, Acknowledge: The WDC Bus Adapter generates this active low 220/330 signal in response to the REQ- signal from the controller when the host is ready to receive or transmit a byte of data. To complete the handshake, the WDC Bus Adapter must send an acknowledge in response to each request (REQ-). Table 9-10. Host Bus Control Signals

NAME DRV/RCVR DEFINITION

RST- Rcvr, Reset: The WDC Bus Adapter sends this active low signal to 220/330 the WDC to force the controller WDC to the idle state. After RST- has become active, any controller status is cleared. RST- also causes the deactivation of all signals to the drives. The time requirement for the RST- signal is as follows:

Minimum Maximum

100 nsec None

SEL- Rcvr, Select: The WDC Bus Adapter sends this active low signal to 220/330 the WDC to begin a command transaction. Along with SEL-, the WDC Bus Adapter also sends an address bit to select the controller (DBO- for controller). The controller must not be busy. The WDC Bus Adapter must deactivate SEL- before the end of the current command.

Table 9-11. Host Bus Data Signals

NAME DRV/RCVR DEFINITION

DBO- Tri-State These are the eight data bits (lines) of the host SASI bus to 220/330 (DBO = LSB). DB7-

The eight lines also are used as address bits to select a controller, in systems using multiple controllers. There is a one-to-one correspondence between the data lines and the controller select lines. The normal connection (hard-wired on the board) is to DBO-, which is the address of controller 0. Any other connection requires cutting the existing trace on the PCBA and adding a jumper.

The following list shows the bit assignments.

DBO-	Controller	0
DB1-	Controller	1
DB2-	Controller	2
DB3-	Controller	3
DB4-	Controller	4
DB5-	Controller	5
DB6-	Controller	6
DB7-	Controller	7

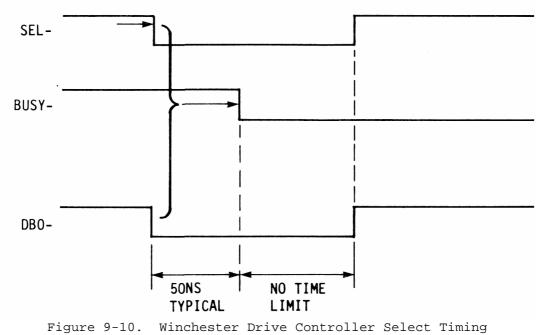
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9.3.3.2 Detailed Description (Handshaking and Timing)

The following paragraphs describe the interaction between the Winchester Drive Controller (WDC) and the WDC Bus Adapter.

Controller Selection - Before the WDC Bus Adapter can begin a transaction, it must select the controller. The WDC Bus Adapter selects the controller by activating the SEL- control signal and the address bit of the controller. Any bit, DBO- through DB7-, can be the address bit in a system with multiple controllers (all controllers leave the factory with DBO- connected to the controllers' address logic). For this discussion, the controller's address is 0.

The timing diagram in figure 9-10 shows the basic timing requirements. Upon receiving both the SEL- signal and DBO-, the WDC activates the BUSYsignal. As shown in the timing diagram, both SEL- and DBO- must be active (low) before the controller can activate the BUSY- signal. During the selection process, the host (the Central Microprocessor Board) has control of the data bus as signified by the deactivation of the I-/0 line. Selection is complete when BUSY- becomes active. The SEL- signal must be deactivated by the WDC Bus Adapter before the current controller operation has completed. It is recommended that the SEL- line be deactivated at or before the time the first control byte is sent to the controller (WDC). The controller then enters the command mode.



<u>Command Mode</u> - The Winchester Drive Controller (WDC) receives commands from the WDC Bus Adapter using a handshaking sequence. The controller places a low level on the C-/D (Control-/Data) line to indicate that it wants a command from the WDC Bus Adapter and places a high level on the I-/O line to indicate that the movement of information is from the Adapter to the controller. The MSG- line is high.

The controller activates the REQ- line within 10 microseconds after signals I-/0, C-/D and MSG- have been placed at high, low and high levels. The WDC Bus Adapter responds by activating the ACK- signal when a control byte is ready for the controller. The control byte placed on the data bus by the WDC Bus Adapter must be stable within 250 nanoseconds after the ACK- is activated. The control byte must be held stable until REQ- is deactivated. The WDC Bus Adapter deactivates ACK- after REQ- goes high. This completes the handshake for the first control byte. Each succeeding control byte from the WDC Bus Adapter requires the same complete handshake sequence. See figure 9-11 for data bus, REQ- and ACK- timing. See table 9-8 for I-/0, C-/D and MSG- definitions.

<u>Data Transfer</u> - The timing diagrams in figures 9-11 and 9-12 illustrate the required timing for data transfer. See table 9-8 for I-/0, C-/D and MSG- definitions.

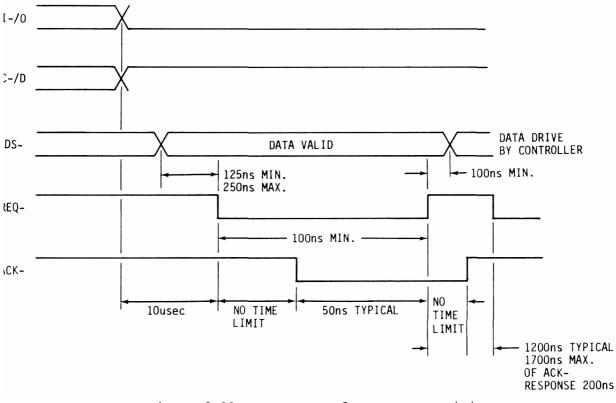


Figure 9-11. Data Transfer to Host, Timing

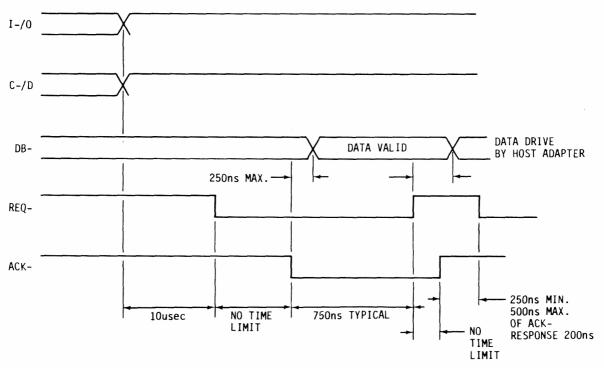


Figure 9-12. Data Transfer from Host, Timing

Status Bytes - Two bytes of status are passed to the host at the end of all commands. The first byte informs the host (Central Microprocessor Board via the WDC Bus Adapter PCBA) whether any errors occurred during the execution of the command. The second is a zero byte. It signals to the host that the command is complete. Figure 9-11 shows the data bus, REQ-, and ACK- timing. See table 9-8 for I-/0, C-/D and MSG- definitions. Figure 9-13 shows the format of these two bytes.

9.3.3.3 Programming Information

The following subsection discusses communication between the Winchester Drive Controller (WDC) and the host (Central Microprocessor Board) from the point of view of the codes that are passed. The host sends commands to the controller through the WDC Bus Adapter. The controller then implements the commands and reports back to the host.

9.3.3.4 Commands

The host sends a six-byte block to the controller to specify the operation. This block is the Device Control Block (DCB). Figure 9-13 shows the composition of the DCB. The list that follows figure 9-13 defines the bytes that make up the DCB. At the end of a command, the controller returns two completion status bytes to the WDC. The format of these bytes is shown in figure 9-14.

Control Byte - The control field, byte 5, of the DCB allows the user to select options for several different types and makes of disk drives. The following list defines the bits of the control byte.

- Bit 0 Half-step option: Seagate Technology and Texas Instruments.
- Bit 1 Half-step option: Tandon
- Bit 2 Buffer-step option: Computer Memories, Inc. and Rotating Memories, Inc. (200 microsecond pulse per step)
- Bit 3-5 Spare. Set to zero for future use.
- Bit 6 If one during a read sector command, the failing sector is not re-read on the next revolution before attempting correction. This bit should be set to zero for normal operation.
- Bit 7 Disable the retries by the controller on all disk-access commands. Set this bit only during the evaluation of the performance of a disk drive. Otherwise, the bit should be set to zero.

NOTE

The step option bits (0-2) are mutually exclusive, and only one option should be selected in any given configuration.

BIT		7	6 5	4	4	3	2	1	0
Byte C)	Class	Code	2		(Dpcode	2	
Byte 1	-	LU	JN	1	Logic	al B	lock A	ddre	SS
Byte 2	2		Logi	cal H	Block	Addı	ress		
Byte 3	3	I	ogical	Bloo	ck A	ddres	ss (LS	SB)	
Byte 4	Ł		Nu	mber	of E	lock	5		
Byte 5	5		Contr	ol I	Byte	(rese	erved)		
Figu	ire 9-1	L3. I	evice	Cont	rol E	Block	(DCB)	For	mat

Byte 0 Bits 7, 6 and 5 identify the class of the command. Bits 4 through 0 contain the opcode of the command. Byte 1 Bits 7, 6 and 5 identify the logical unit number (LUN). Bits 4 through 0 contain logical block address 2. Byte 2 Bits 7 through 0 contain logical block address 1. Byte 3 Bits 7 through 0 contain logical block address 0 (LSB). Bits 7 through 0 specify the block count. Byte 4 Byte 5 Bits 7 through 0 contain the control byte. Logical Address (High, Middle, Low) - The logical address of the drive is computed by using the following equation. Logical Address = (CYADR * HDCYL + HDADR) * BKTRK + BKADR Where: CYADR = Cylinder Address HDADR = Head Address BKADR = Block (Sector) Address HDCYL = Number of Heads per Cylinder BKTRK = Number of Blocks (Sectors) per Track Next to Last Status Byte BIT 7 6 5 4 3 2 1 0 0 0 0 d BUSY EQUAL CHECK 0 Bits 0, Set to zero. 5, 6, 7 Bit 1 Check condition. Sense is available. Bit 2 Bit 3 Equal. Set when any SEARCH is satisfied. Busy. Device is busy or reserved. Last Status Byte BIT 7 6 5 4 3 2 1 0 0 0 0 0 0 0 0 0 Bits Set to zero. 0-7

Figure 9-14. Completion Status Bytes

The commands fall into eight classes, 0 through 7; only classes 0 and 1 are used. Class 0 commands are data, non-data transfer, and status commands. Classes 1 through 6 are reserved. Class 7 are diagnostic commands.

Each command is described below. The description includes its class, opcode and format.

<u>Test Drive Ready (Class 0, Opcode 00)</u> - This command selects a particular drive and verifies that the drive is ready. The following diagram shows the format of the device control block for this command.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	0	0	0	0	0
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	00	
Byte 3	0	0	0	0	0	0	00	
Byte 4	0	0	0	0	0	0	00	
Byte 5	0	0	0	0	0	0	00	

Rezero Unit (Class 0, Opcode 01) - This command positions the read/write $(\mbox{R/W})$ arm to track 00.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	0	0	0	0	1
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	0	0	0	0	0	0	0	0
Byte 4	0	0	0	0	0	0	0	0
Byte 5	0	0	0	0	0	0	0	0

Reserved (Class 0, Opcode 02) - This opcode is not used.

<u>Request Sense Status (Class 0, Opcode 03)</u> - The host must send this command immediately after it detects an error. The command causes the controller to return four bytes of drive and controller status. The formats of these four bytes are shown after the DCB. When an error occurs on a multiple sector data transfer (read or write), the Request Sense Status command returns the logical address of the failing sector in bytes 1-3. If the Request Sense Status command is issued after any of the format commands or the Check Track Format command, then the logical address returned by the controller points to one sector beyond the last track formatted, or checked, if there was no error.

If there was an error, then the address returned points to the track in error.

Tables 9-12 through 9-15 list the error codes. Table 9-15 is a summary of the error codes returned as the result of the Request Sense Status command.

d = dr:	ive, 0 or 1								
	BIT	7	6	5	4	3	2	1	0
	Byte O	0	0	0	0	0	0	1	1
	Byte 1	0	0	d	0	0	0	0	0
	Byte 2	0	0	0	0	0	0	0	0
	Byte 3	0	0	0	0	0	0	0	0
	Byte 4	0	0	0	0	0	0	0	0
	Byte 5	0	0	0	0	0	0	0	0

SENSE BYTES

BIT	7	6	5	4	3	2	1	0
Byte O			SEE BEI	TOM				
Bits 0-3 Bits 4-6 Bit 7	Error	Code Type ss val	id, wher	n set				

The address valid bit in the error code byte (bit 7) is relevant only when the previous command required a logical block address. In this case it is always returned as a one; otherwise, it is set to zero. For instance, if a Recalibrate command is followed immediately by a Request Sense Status command, the address valid bit would be returned as zero. This is because this command does not require a logical block address to be passed in its DCB.

BIT	7	6	5	4	3	2	1	0	
Byte 1	0	0	0	Logical	Block	Address			
Byte 2	Logical Block Address								
Byte 3	Logical Block Address (LSB)								

Table 9-12. Type 0 Error Codes, Disk Drive

HEX CODE DEFINITION 00 The controller detected no error during execution of the previous operation. 01 The controller did not detect an index signal from the drive. 02 The controller did not get a seek complete signal from the drive after seek operation. 03 The controller detected a write fault from drive during last operation. 04 After the controller selected the drive, the drive did not respond with ready signal. 06 After stepping the maximum number of cylinders, the controller did not receive the track 00 signal from the drive. Table 9-13. Type 1 Error Codes, Controller HEX CODE DEFINITION ID Read Error: the controller detected a CRC error in the target ID 10 field on the disk. 11 Data Error: the controller detected an uncorrectable data error in the target sector during a read operation. 12 Address Mark: the controller did not detect the ID address mark. 13 Address Mark: the controller did not detect the data address mark. 14 Record Not Found: the controller found the correct cylinder and head, but not the target record. Seek Error: the controller detected an incorrect cylinder or track, or 15 both. 18 Data Check in No Retry Mode ECC Error During Verify 19 1A Interleave Error 1C Unformatted or Bad Format on Drive Self Test Failed 1D1 E Defective Track: the controller detected the bad track flag.

Table 9-14. Type 2 Error Codes, Command and Miscellaneous

HEX CODE	DEFINITION
20	Invalid Command: the controller has received an invalid command from the disk.
21	Illegal Block Address: the controller detected an address that is be- yond the maximum range.
23	Volume Overflow
24	Bad Argument
25	Invalid Logical Unit Number

Table 9-15. Request Sense Status Error Codes

ERROR CODE (HEX) DEFINITION

00	No error detected (command completed okay)
01	No index detected from drive
02	No seek complete from drive
03	Write fault from drive
04	Drive not ready after it was selected
06	Track 00 not found
10	ID field read error
11	Uncorrectable data error
12	ID address mark not found
13	Data address mark not found
14	Record not found
15	Seek error
18	Data Check in No Retry mode
19	ECC error during verify
1A	Interleave error
1C	Unformatted or bad format on drive
1D	Self test failed
1E	Defective track
20	Invalid command
21	Illegal block address
23	Volume overflow
24	Bad Argument
25	Invalid logical unit number

NOTE: 05, 07-OF, 16/17, 1B, 1F, 22 and 26-2F are not assigned. The address valid bit (bit 7) may or may not be set and is notincluded here, for clarity. Format Unit (Class 0, Opcode 04) - This command formats all sectors with ID and data fields, according to the selected interleave factor. The controller will write from index to index all ID and data fields with a block size as specified by an immediately previous Mode Select command. If no Mode Select command has been executed, the previous data block size will be used. On unformatted disks, or on those whose format is determined bad (sense byte error code 1C [hex] returned following a Read command), a Mode Select command is required prior tothe Format Unit command. Data fields are completely written with 6C (hex) unless otherwise specified in the Format Unit command.

The ID fields will be interleaved as specified in bytes 3 and 4 of the Command Description Block (CDB). Under normal conditions, the Winchester Drive Controller does not require interleaving, because of its high speed buffer control.

An interleave number of 1 results in sequential ID fields being written on the disk. Any interleave number greater than 1, but less than the total number of sectors per track, results in interleaved formatting. A 00 in this field will cause the default interleave factor of 2 to be used. The interleave number is equivalent to the number of disk revolutions required to sequentially read one track.

When the data bit is set (bit 4, byte 1), the controller expects a list of known bad areas in the data portion of the command (defect skipping).

Bit 3 (byte 1) is the complete list bit. It specifies that all the known defects on the drive are contained in the list.

Bit 2 (byte 1), if set, indicates that the next two bits (1 and 0) will be used to define the format. A zero indicates default. Bit 1, if set, indicates that the data pattern in byte 2 is to be used to format the disk. A zero indicates default. A zero in bit 0 indicates that a "Cylinder/ Head/Byte Count" format is used in the data list.

d = drive, 0 or 1

b = data bit

c = complete list bit

f = list format bit

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	0	0	1	0	0
Byte 1	0	0	d	b	С	f	f	f
Byte 2			Data Pa	ttern				
Byte 3	0	0	0	0	0	0	0	0
Byte 4	Interleave Number							
Byte 5	0	0	0	0	0	0	0	0

Reserved (Class 0, Opcode 05) - This opcode is not used. Reserved (Class 0, Opcode 06) - This opcode is not used. Reserved (Class 0, Opcode 07) - This opcode is not used.

<u>Read (Class 0, Opcode 08)</u> - This command transfers to the host the specified number of blocks starting at the specified logical starting block address. The controller will verify a valid seek address and proceed to seek to the specified starting logical block address. When the seek is complete, the controller then reads the starting address data field into the buffer, checks the ECC and begins DMA data transfer.

Subsequent blocks of data are transferred into the buffer in a similar manner until the block count is decremented to zero. Cylinder switching is transparent to the user.

On a data ECC error, the block is re-read up to five times to establish a "solid error syndrome." Only then is correction attempted. Correction is done directly into the data buffer, transparent to the user.

d = drive, 0 or 1

BIT	7	б	5	4	3	2	1	0
Byte O	0	0	0	0	1	0	0	0
Byte 1	0	0	d	Log	ical 1	Block	Addr	ess
Byte 2			Logic	al Bl	ock Ad	ddress	5	
Byte 3		Log	ical	Block	Addre	ess (I	LSB)	
Byte 4			Bl	ock C	ount			
Byte 5	0	0	0	0	0	0	0	0

Reserved (Class 0, Opcode 09) - This opcode is not used.

<u>Write (Class 0, Opcode OA)</u> - This command transfers to the target device the specified number of blocks, starting at the specified logical starting block address. The controller seeks to the specified logical starting block. When the seek is complete, the controller transfers the first block into its buffer and writes its buffered data and its associated ECC into the first logical sector.

Subsequent blocks of data are transferred as they become available from the FIFO buffer, until the block count is decremented to zero. Cylinder switching and defect skipping are transparent to the user.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	0	1	0	1	0
Byte 1	0	0	d	Log	ical	Block	Addr	ess
Byte 2		L	ogica	l Bl	ock A	ddress	3	
Byte 3		Logi	cal B	lock 2	Addre	ss (LS	SB)	
Byte 4			Blo	ock C	ount			
Byte 5	0	0	0	0	0	0	0	0

<u>Seek (Class 0, Opcode OB)</u> - This command causes the selected drive to seek to the specified starting address. The controller returns completion status immediately after the seek pulses are issued and head motion starts. This allows the controller to free the bus and accept further commands prior to actual seek completion.

NOTE

Any command received for a unit with a seek in progress will immediately complete with the busy command completion status (bit 3 set). This is done to allow the host to use the SASI bus to do other processing while waiting for seek to complete.

The drive is stepped to the addressed track position, but no ID field verification is attempted. When the seek is complete, the controller reconnects to the host and responds with the completion status.

The Winchester Drive Controller uses an implied seek on READ, WRITE and SEARCH commands, obviating the need for issuance of SEEK commands with each operation.

```
d = drive, 0 or 1
```

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	0	1	0	1	1
Byte 1	0	0	d	Logi	cal B	lock	Addre	SS
Byte 2			Logic	al Bl	ock A	ddres	S	
Byte 3		Logi	cal E	lock .	Addre	ss (L	SB)	
Byte 4	0	0	0	0	0	0	0	0
Byte 5	0	0	0	0	0	0	0	0

Reserved (Class 0, Opcode 0C) - This opcode is not used.

Reserved (Class 0, Opcode OD) - This opcode is not used.

Reserved (Class 0, Opcode OE) - This opcode is not used.

<u>Translate (Class0, Opcode OF)</u> - This command performs a logical address to physical address translation and returns the physical location of the requested block address in a cylinder/head/bytes-from-index format. This data can be used to build a defect list for the FORMAT command.

Eight bytes are returned in the format of defect descriptors, required by FORMAT.

A data error in the ID field will cause an error status to be returned. It is then necessary to TRANSLATE the blocks before and after the targeted block to determine the location of the target block. The use of interleaved sectors and formatted (skipped) defects may complicate the determination of the error location.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	0	1	1	1	1
Byte 1	0	0	d	Log	ical	Block	Addr	ess
Byte 2		L	ogica	l Blo	ck Ad	dress		
Byte 3		Log	ical 1	Block	Addr	ess (I	LSB)	
Byte 4	0	0	0	0	0	0	0	0
Byte 5	0	0	0	0	0	0	0	0

Reserved (Class 0, Opcode 10) - This opcode is not used.

Reserved (Class 0, Opcode 11) - This opcode is not used.

Reserved (Class 0, Opcode 12) - This opcode is not used.

<u>Write Data Buffer (Class 0, Opcode 13)</u> - This command serves buffer RAM diagnostic purposes. The controller will fill the buffer with IK bytes of data from the host. There is no guarantee that this data will not be overwritten by other operations initiated by other initiators.

d = drives 0 or 1	d =	drives () or 1
-------------------	-----	----------	--------

BIT	7	б	5	4	3	2	1	0
Byte O	0	0	0	1	0	0	1	1
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	0	0	0	0	0	0	0	0
Byte 4	0	0	0	0	0	0	0	0
Byte 5	0	0	0	0	0	0	0	0

Read Buffer RAM (Class 0, Opcode 14) - Read Buffer RAM will pass the host IK bytes of data from the buffer. It is intended for RAM diagnostic purposes. There is no guarantee that this data will not be overwritten by other operations initiated by other initiators. In addition, although data remains in the buffer after normal data operations, the ordering of the data found there is undefined.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	1	0	1	0	0
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	0	0	0	0	0	0	0	0
Byte 4	0	0	0	0	0	0	0	0
Byte 5	0	0	0	0	0	0	0	0

<u>Mode Select (Class 0, Opcode 15)</u> - This command is used to specify FORMAT parameters and should always precede the FORMAT command.

A blown format error (code 1C) is detected when the controller is unable to read the drive information from a drive already formatted. The user should use this command to inform the controller about the drive information. Then the drive should be backed up and reformatted.

Byte 4 of the command specifies the number of information bytes to be passed with the command. A minimum of twelve bytes (OC [hex]) must be specified. If drive parameters are being specified, the count should be 22 bytes (16 [hex]). The Parameter List (shown in table 9-16) is four bytes long, with the first three bytes reserved (zero filled). The fourth byte contains the length, in bytes, of the Extent Descriptor List; this is always eight. (Only a single extent is supported.)

	Table 9-16.	Mode	Selec	t Par	Parameter		List	
BIT	7 6	5	4	3	2	1	0	
Byte O	0 0	0	0	0	0	0	0	
Byte 1	0 0	0	0	0	0	0	0	
Byte 2	0 0	0	0	0	0	0	0	
Byte 3	0 0	0	0	1	0	0	0	

Byte 0 of the Extent Descriptor List (shown in table 9-17) specifies the data density of the drive. The Winchester Drive Controller supports only MFM, and a value of 00 is required in this byte. Bytes 1, 2 and 3 are reserved and must be zero, specifying that the entire drive is to be formatted. Bytes 5 through 7 are used to specify the data block size. The block size must not be less than 256 or exceed the RAM buffer capacity, which is IK bytes, or 1,024 characters. In this controller the block size must be set up with a value 256, 512 or 1024 bytes. Violation of this constraint results in Check Status with an Error Code of 24 [hex], indicating an invalid argument in parameter data.

The Extent Descriptor List and the Drive Parameter List (described next) are a single large block of data that follows the command. The Drive Parameter List (shown in table 9-18) includes all the data necessary to specify a drive. It is optional, but if present, it must be complete, and the items must be within the limits stated. If these parameters are not supplied, the format operation will use previously supplied values, if available, or the default values given on the following page.

The List Format Code must be 01.

The Cylinder Count is the number of data cylinders on the drive. Because of the inline defect skipping formatting, cylinders normally set aside as spares may be included in this total. The minimum is one. The maximum supported is 2,048. The default value is 306.

The Data Head Count is the number of usable data surfaces. The heads will be selected from 0 to head count minus 1. The minimum is 1; the maximum is 16. A drive with nine or more heads will use the Reduced Write Current line as the high order head select. The default value is two.

The Reduced Write Current Cylinder is the cylinder number beyond which the controller will assert the Reduced Write Current line. The minimum value is 0; the maximum is 2,047. The default value is cylinder 150.

The Write Precompensation Cylinder is the cylinder beyond which the controller will compensate for inner track bit shift. The specifications for this function agree with those of most disk manufacturers. Minimum value is 0; maximum is 2,047.

BIT	7 6	5 4	3	2	1	0
Byte O	0 0	0 0	0	0	0	0
Byte 1	0 0	0 0	0	0	0	0
Byte 2	0 0	0 0	0	0	0	0
Byte 3	0 0	0 0	0	0	0	0
Byte 4	0 0	0 0	0	0	0	0
Byte 5		Block Si	ze (MS	SB)		
Byte 6		Block	Size			
Byte 7		Block Si	ze (LS	SB)		
	Table 9-18.	Drive P	aramet	ter L	ist	
BIT	7 6	5 4	3	2	1	0
Byte O	L	ist Form	at Coo	de ==	01	
Byte 1		Cylinder	Count	(MSB)	
Byte 2		Cylinder	Count	(LSB)	
Byte 3		Data He	ad Coi	unt		
Byte 4	Reduced	Write C	urrent	c Cyl:	inder	(MSB)
Byte 5	Reduced	Write C	urrent	c Cyl:	inder	(LSB)
Byte 6	Write	Precompen	satio	n Cyl:	inder	(MSB)
Byte 7	Write	Precompen	satio	n Cyl:	inder	(LSB)
Byte 8	L	anding Zo	ne Pos	sitio	n	
Byte 9	Step	Pulse O	utput	Rate	Code	

Table 9-17. Extent Descriptor List

The Landing Zone Position is used with the Start/Stop command to indicate the direction and number of cylinders from the last data cylinder to the shipping position. The most significant bit indicates the direction, with a zero meaning that the landing zone is beyond the highest track, and a one indicates the landing zone is outside track 00. The low seven bits gives the number of cylinders. The default value is zero (land on innermost track).

d = drive, 0 or 1

The Step Pulse Output Rate Code specifies the timing of seek steps. Three options are available:

00 = non-buffered, 3 ms; 01 = buffered, 0.028 ms; 02 = buffered, 0.012 ms.

Reserved (Class 0, Opcode 16) - This opcode is not used.

Reserved (Class 0, Opcode 17) - This opcode is not used.

Reserved (Class 0, Opcode 18) - This opcode is not used.

Reserved (Class 0, Opcode 19) - This opcode is not used.

<u>Mode Sense (Class 0, Opcode 1A)</u> - This command is used to interrogate the Winchester Drive Controller parameter table to determine the specific characteristics of any disk drive currently attached.

The attached drive must have been formatted by this controller for this to be a legal command.

Byte 4 of the command specifies the number of data bytes to be returned from the command. A minimum of 12 bytes (OC [hex]) must be specified. If the drive parameter list is required, the count should be 22 bytes (16 [hex]).

The returned information will be the four-byte parameter list, the Extent Descriptor List and the Drive Parameter List (if requested). These lists take the exact format of those in the MODE SELECT command. Please reference that command for details.

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	1	1	0	1	0
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	0	0	0	0	0	0	0	0
Byte 4		Nu	mber	of By	tes R	eturn	ed	
Byte 5	0	0	0	0	0	0	0	0

Start/Stop Unit (Class 0, Opcode 1B) - Byte 4, bit 0 of this command should be set if this is a START command; otherwise, it is a STOP command.

This command is designed for use on drives with a designated shipping or landing zone.

A STOP command will move the head to the landing zone position.

d = drive, 0 or 1

s = Start/Stop, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	1	1	0	1	1
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	0	0	0	0	0	0	0	0
Byte 4	0	0	0	0	0	0	0	S
Byte 5	0	0	0	0	0	0	0	0

<u>Receive Diagnostic Result (Class 0, Opcode 1C)</u> - This command sends analysis data to the host (Central Microprocessor Board) after completion of a SEND DIAGNOSTIC command. Bytes 3 and 4 designate the size of the available buffer (in bytes).

READ DIAGNOSTIC is used to transfer data to the host and must immediately follow a SEND DIAGNOSTIC command, which initiates the dump action. Otherwise, the command will be rejected.

The data length specified should be 104 (hex) or more; however, if a smaller buffer is provided, only that much data will be transferred, and the command will terminate normally.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	0	1	1	1	0	0
Byte 1	0	0	d	0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3			Data	Leng	th (M	SB)		
Byte 4			Data	Leng	th (L	SB)		
Byte 5	0	0	0	0	0	0	0	0

The data received as a result of a dump will be formatted as follows (next page):

BIT	7	6	5	4	3	2	1	0
Byte O		Data	Blo	ck Le	ngth	(MSB)		
Byte 1		Data	Blo	ck Le	ngth	(LSB)		
Byte 2	St	arting	g Add	ress	of	Dump	(MSB)	
Byte 3	St	arting	g Add	ress	of	Dump	(LSB)	
Byte 4 • *		Di	umped	Dat	a (x	x00)		
• Byte 103		D	umped	Dat	a (x	xFF)		

<u>Send Diagnostic (Class 0, Opcode 1D)</u> - This command sends data to the controller to specify diagnostic tests for controller and peripheral units.

Bytes 3 and 4 specify the length of the data to be sent.

The data length specified in the command must be at least 4 bytes long and should be equal to the length of the data block to be passed over to the controller. If the length specified is longer than needed, the excess is ignored and not read.

The first byte of the data block specifies the particular function being requested. The options available, along with their associated codes are:

HEX CODE	DEFINITION
60	Reinitialize Drive
61	Dump Hardware Area (4000-40FF)
62	Dump RAM (8000-80FF)
63	Patch Hardware Area
64	Patch RAM
65	Set Read Error Handling Options

Of these options, only the patch options require a data block longer than four bytes.

The second byte specifies a subtest or qualifiers specific to the test selected by the first byte. (Because of the potential danger in patching controller programs, this byte provides a safety mechanism to prevent obsolete patches.) The second byte is not checked if the 65 (hex) option code is specified.

The third byte specifies the starting address (in RAM or the memory-mapped registers) to be patched. The high byte of the address is implicit in the

diagnostic specified. Therefore, a Patch RAM operation with a third byte of A1 (hex) will overwrite an area of RAM starting with 80A1 (hex).

The fourth byte gives the number of bytes to be overwritten. This can range from 1 to 256, with a zero yielding 256. the data block for the Send Diagnostic Command is as follows.

BIT	7	б	5	4	3	2	1	0
Byte O			Diagno	ostic	Spec	ifier		
Byte 1	Dia	gnost	ic Opt	cion/(Coded	Relea	ase L	evel
Byte 2	Pat	ch St	arting	g Addi	ress	LSB/Q	ualif	ier
Byte 3		Patc	h Data	a Leng	gth o	r Res	erved	
Byte 4			Optior	nal Pa	atch	Data		
*								
•								
Byte N+3			Optior	nal Pa	atch	Data		

Byte 2 of the data block specifies the actions to take place upon encountering an ECC check, if option 65 (hex) is selected. The default state is established by a controller reset.

These options, once set, stay in effect until the next reset. They apply only to the Logical Unit Number addressed by the command.

The Set Read Error Handling Options are:

HEX CODE

DEFINITION

- 00
- Selects default operation where a correctable error will be corrected without comment and all data transferred without check status.

If the error is not correctable, the controller will transfer the uncorrected data and set check status with an error code 91 (hex). The valid address will be that of the bad block.

01 Report all corrections and stop. A correctable error will be corrected and the data transferred, but the operation will stop with a check status and an error code (hex).

An uncorrectable error will be handled as in 00 (hex), above.

Do not correct. All ECC errors will be treated as uncorrectable, except that the error code is set to 98 (hex). Reserved (Class 0, Opcode 1E) - This opcode is not used.

Reserved (Class 1, Opcode 1F) - This opcode is not used. Reserved (Class 1, Opcode 20) - This opcode is not used. Reserved (Class 1, Opcode 21) - This opcode is not used. Reserved (Class 1, Opcode 22) - This opcode is not used. Reserved (Class 1, Opcode 23) - This opcode is not used. Reserved (Class 1, Opcode 24) - This opcode is not used.

<u>Read Capacity (Class 1, Opcode 25)</u> - If byte 8 of the Device Control Block (DCB) is 00, this command will return the address of the last block on the unit. It is not necessary to specify a starting block address in this command mode.

If byte 8 is 01 (hex), this command will return the address of the block (after the specified starting address) at which a substantial delay in data transfer will be encountered (e.g., a cylinder boundary). Any value other than 00 or 01 (hex) in byte 8 will cause Check Status with an Error code of 24 (hex), for an invalid argument.

In both cases, the format block size is defined by the last four bytes of the eight-byte data field returned as a result:

4 bytes, Block Address 4 bytes, Block Size

d = drive, 0 or 1

r = relative address, 0 or 1

BIT		7	б	5	4	3	2	1	0
Byte	0	0	0	1	0	0	1	0	1
Byte	1	0	0	d	0	0	0	0	r
Byte	2		Logio	cal B	lock i	Addres	ss (MS	SB)	
Byte	3		I	Logica	al Blo	ock Ad	ldress	5	
Byte	4		I	Logica	al Blo	ock Ad	ldress	5	
Byte	5		Logio	cal B	lock i	Addres	ss (LS	SB)	
Byte	6	0	0	0	0	0	0	0	0
Byte	7	0	0	0	0	0	0	0	0
Byte	8	Η	Full d	or Pa	rtial	Media	a Indi	lcator	2
Byte	9	0	0	0	0	0	0	0	0

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Reserved (Class 1, Opcode 26) - This opcode is not used. Reserved (Class 1, Opcode 27) - This opcode is not used. Reserved (Class 1, Opcode 28) - This opcode is not used. Reserved (Class 1, Opcode 29) - This opcode is not used. Reserved (Class 1, Opcode 2A) - This opcode is not used. Reserved (Class 1, Opcode 2B) - This opcode is not used. Reserved (Class 1, Opcode 2B) - This opcode is not used. Reserved (Class 1, Opcode 2D) - This opcode is not used. Reserved (Class 1, Opcode 2C) - This opcode is not used.

<u>Write and Verify (Class 1, Opcode 2E)</u> - This command is similar to the traditional "read after write" function. It is an extended address command that operates like a WRITE command over the specified number of blocks and then verifies the data written on a block by block basis. The verify function transfers no data to the host.

Since no data is transferred to the host during verify, correctable data checks will be treated in the same manner as uncorrectable data checks.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	1	0	1	1	1	0
Byte 1	0	0	d	0	0	0	0	0
Byte 2		Logi	cal B	lock A	Addre	ss (M	SB)	
Byte 3		L	ogica	l Blo	ock A	ddres	S	
Byte 4		\mathbf{L}	ogica	l Blo	ock A	ddres	S	
Byte 5		Logi	cal B	lock A	Addre	ss (L	SB)	
Byte 6	0	0	0	0	0	0	0	0
Byte 7			Nui	mber d	of Bl	ocks		
Byte 8			Nui	mber d	of Bl	ocks		
Byte 9	0	0	0	0	0	0	0	0

 $\underline{Verify}~(Class~1,~Opcode~2F)$ - This command is similar to the previous WRITE AND VERIFY except that it verifies the ECC of an already existing set of data blocks.

It is the responsibility of the host to provide data for rewriting and correcting when an error is detected.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte O	0	0	1	0	1	1	1	1
Byte 1	0	0	d	0	0	0	0	0
Byte 2		Logi	.cal	Block	Addr	ess (MSB)	
Byte 3		I	ogica	l Blo	ck Ad	dress		
Byte 4		I	logica	l Blo	ck Ad	dress		
Byte 5		Logi	.cal	Block	Addr	ess (LSB)	
Byte 6	0	0	0	0	0	0	0	0
Byte 7			Nun	iber o	f Blo	cks		
Byte 8			Nun	iber o	f Blo	cks		
Byte 9	0	0	0	0	0	0	0	0

Reserved (Class 1, Opcode 30) - This opcode is not used.

<u>Search Data Equal (Class 1, Opcode 31)</u> - This powerful extended address command provides for a "search-and-compare-on-equal" of any data on the disk. The starting block address and number of blocks to search are specified, and a search argument, which includes a byte displacement and the data to compare, is passed from the host.

The Invert bit (byte 1, bit 4) inverts the sense of the search comparison operation. With invert on, a SEARCH DATA EQUAL command would succeed on data not equal; SEARCH DATA LOW would succeed on data greater or equal. The invert bit allows SEARCH EQUAL inverted, which succeeds on the first block not equal to the pattern.

When a search is satisfied, it will terminate with a Condition Met Status. A Request Sense Command can then be issued to determine the block address of the matching record. A Request Sense following a successful Search Data command will:

- Report a Sense Key of Equal, if the search was satisfied by an exact match. If the search was satisfied by an inequality, a Sense Key of No Sense is reported.
- 2. Set the Valid bit to one.
- 3. Report the address of the block containing the first matching record in the Information Bytes.

The Request Sense command following an unsuccessful Search Data Command will: 1) Report a Sense Key of No Sense, provided no errors occurred; and 2) Set the Valid bit to zero.

```
d = drive, 0 \text{ or } 1
i = invert, 0 or 1
        BIT
                  7
                        6
                             5
                                  4
                                      3
                                           2
                                                1
                                                     0
                                  1
        Byte 0
                   0
                        0
                             1
                                       0
                                           0
                                                0
                                                     1
                   0
                                  i
                                       0
                                                0
                                                     0
        Byte 1
                        0
                             d
                                           0
        Byte 2
                        Logical Block Address (MSB)
                          Logical Block Address
        Byte 3
        Byte 4
                          Logical Block Address
        Byte 5
                        Logical Block Address (LSB)
                             0 0 0 0 0
        Byte 6
                   0
                        0
                                                   0
                             Number of Blocks
        Byte 7
        Byte 8
                             Number of Blocks
                               0 0
        Byte 9
                   0
                        0
                             0
                                         0
                                                0
                                                     0
```

The argument following a SEARCH command is presented in table 9-19; a definition of the required data in the argument is presented in table 9-20. Table 9-19. Search Command Argument

BIT		7 6	5 5	4	3	2	1	0
Byte	0		Reco	rd Siz	e (M	ISB)		
Byte	1		R	ecord	Size			
Byte	2		R	ecord	Size			
Byte	3		Reco	rd Siz	ze (I	SB)		
Byte	4	I	'irst Re	cord C)ffset	(MS	В)	
Byte	5		First	Recor	d Of	fset		
Byte	6		First	Recor	d Of	fset		
Byte	7	I	'irst Re	cord C)ffset	LS (LS	В)	
Byte	8		Number	of Rec	cords	(MSB)		
Byte	9		Numb	er of	Recor	ds		
Byte	10		Numb	er of	Recor	ds		
Byte	11		Number	of Rec	cords	(LSB)		
Byte	12	Se	earch Ar	gument	: Leng	ſth (MSB)	
Byte	13		Search	Argum	lent I	length	L	
Byte	14	Sea	arch Fie	ld Dis	place	ement	(MSB)	
Byte	15		Search	Field	Displ	aceme	nt	
Byte	16		Search	Field	Displ	aceme	nt	
Byte	17	Sea	arch Fie	ld Dis	place	ement	(LSB)	
Byte	18		Patte	rn Ler	ngth (MSB)		
Byte	19		Pa	ttern	Lengt	h		
Byte *	20		D	ata Pa	atterr	1		
•								
Byte	M+19		D	ata Pa	attern	l		

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Table 9-2	0. Search Command Argument Required Data
BYTES	PARAMETER
0 to 3 blocksize	Record Size (bytes) - This must equal the
DIUCKSIZE	or zero. Zero will be taken to mean the format blocksize.
4 to 7	First Record Offset (bytes) - This must be zero.
8 to 11	Number of Records - This must be less than or equal to the number of blocks specified in the command and greater than zero. The search will terminate upon a match or when the smaller value is encountered.
12 to 13	Search Argument Length (bytes) - The number of bytes in the following search argument. Must equal the pattern length plus six.
14 to 17	Search Field Displacement - The displacement from the beginning of the record to the first byte to be compared. Must be zero.
18 to 19	Pattern Length (M bytes) - The number of bytes in the following data pattern to be compared with a like size field in each record. Pattern length must equal blocksize.
20 to M+19	Data Pattern - A variable length field of M bytes up to blocksize minus displacement bytes. The pattern must be one block long.

SECTION X

REFERENCE DATA

FIGURE	TITLE	PAGE
10-1	PCBA, Central Microprocessor Board	10-2
10-2	Logic Diagram, Central Microprocessor Board (59 drawings)	10-3

PCBA, Central Microprocessor Board

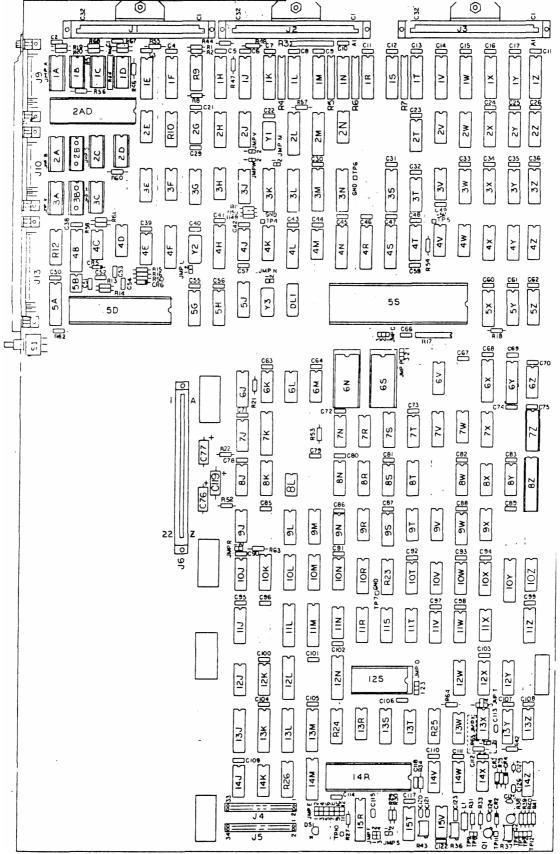


Figure 10-1. PCBA, Central Microprocessor Board

POWER CHART (UNLESS OTHERWISE SPECIFIED)									
DEVICE +5V/+5VB 4 GND +12V-12V -8									
1488		7	14	1					
2732	24	12							
2210	18	8							
ALL ZO PIN	ZØ	10							
ALL 16 PIN	16	8							
ALL 14 PIN	14	7							
NE 555	4,8	1							
75452	в	4							

REFERENCE DESIGNATIONS							
LAST USED	NOT USED						
R68							
C127	C19,20,27,28,37 58 -						
TPIZ							
02							
Y3							
CR6	CRI						
DL1							
JMP X	M'O'O' N						
DSI							
51							
LI							

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 1 of 58)

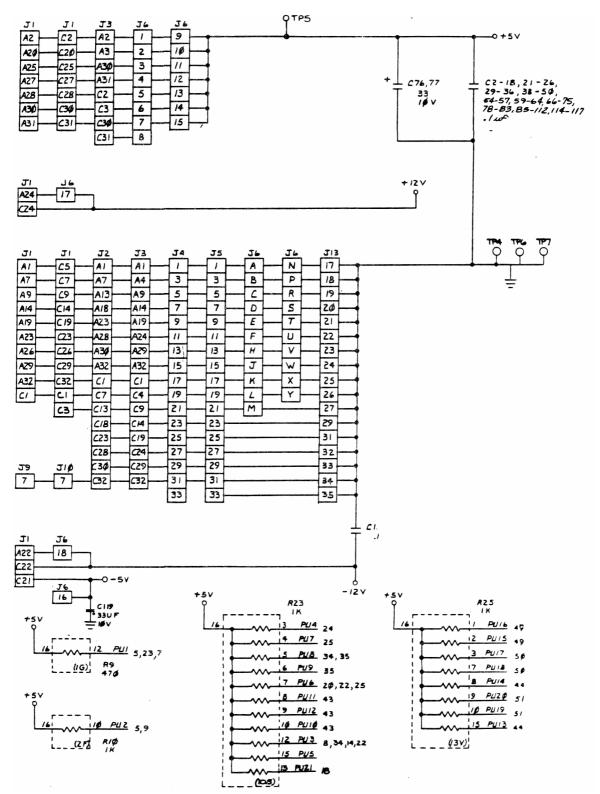


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 2 of 58)

COMPONENT MAP

						_											
						4+	745240	5	5	5	5	10L	7413138	20		\sim	1
							\rightarrow	29	29	23		11	74L9244	42	42	42	42
					T	3+	1 745112	23	23	∇	∇		\geq	42	42	42	42
24	0 28530	28	28	1/	\sim	1 Г	1	1	1	T	T	121	74L5374	45	\square	\square	\sim
54	7415244	27	27	-	27	TT I	745240	16	16	16	16	1 DL	7413875	47	\sim	\sim	
-	$\mathbf{>}$	27	27	27	27			16	16	16	16	1 -		1	1	1-	
		-		1			TALSISS	29	17	17	17			+	+	1	1
18	1488	28	28	28	28	1 33	7418151	29	1>	1>	17			1	1		+
-	+	+	+	+		43	74510	23	22	1	1>	1 IM	743240	17	17	17	17
	+	+	+	+	+	57	745112	5	23	+>	1>			17	17	17	17
48	7415244	27	27	27	27		745161	5	+=>	\leftarrow	1	21	741.9244	19	17	19	10
F		27	27	27	27		745260	23	23	\leftarrow	\leftarrow			19	10	0	19
		21	+	+->	1->	a.	74558	6	16	23	\leftarrow	34	741.5244	19	19	19	19
58	1489A	28	28	28	\leftarrow	Te l	741.5161	24	+	+->				19	10	19	19
					28.1			+	\vdash	\leftarrow	\leftarrow	444	241 4322	28	28.1	+	
20	1488	28.		-		10		25	+ -	\leftarrow	\leftarrow	===	74L532				+
30	1489A	28.			28.1		7415157	48	K	K	K		2485	1.	+ <u></u>		
40	26LS32	28.1	28.	28.1		12		47	47	47	50	GM	74851	16	16	\vdash	\vdash
			I			ter l	74L5273	47	K						 		
						Z N	74.006	47	49	49	49	BM	SPARE			L	<u> </u>
10	1489A	28	28	28	28		\geq	49	+	\leq	\leq	944	74195/	25	25	K	$ \leftarrow$
20	1489 A	28.1	28.1	28.1								10M	741.5259	19		\leq	\swarrow
30	SPARE			I					-			IIM	74L8244	42	42	42	42
4D	261531	28.	28.	1		IK	74L5240	16	16	16	16		\geq	42	42	42	42
	1						\geq	16	16	16	16	IZM	SPARE				
50	6823Ø	26				2K	(11)	29				13M	7418245	42			
						ЗK	745375	29				1444	741.8244	44	50	50	50
IE.	74A5244	8	8	8	28.1	4K.	74'L5138	9		\sim			\sim	50	50	52	
\geq	\sim	22	22	26	28	5K	(¥3)	5		\mathbb{Z}							
2E	741514	21	21			L.K.	74574	6	7								
æ	7415148	22	\sim		\square	TK	745299	6	\bigtriangledown	\square	\square	IN	745240	15	15	15	15
4E	741.500	21	21			8K	745151	6	\square	\square	\geq		\times	15	15	15	/5
						9K	SPARE	1	Γ	Γ		2N	74L538	40		\geq	\square
						KOK	THLEISI	22	$\overline{\mathbf{z}}$			BN	74.5 374	41			
F	745240	6	7	22		lik	SPARE	1	r	r	~	AN	741.5244	15	15.	15	15
5		14	14	14	14	IZK	7418895	45	45				\sim	15	15	15	15
					-	ISK	T4L8275	47	17		$\boldsymbol{\succ}$						
3F	741.556	6	21	21	21	HAK		47	47	47	47	GN	2732/2764	18			
4F	745240	21	21	21	26			47	47	$\mathbf{\dot{>}}$	>	TN	74550	6	6	6	
-		26						+			\sim	BN	745//	40	40		
							+					91	74502	6	6	8	ZØ
							7413240	17	17	17	17	KON	74520	20	49	-	\rightarrow
26	74838	23	23	Z 3	23			17	17	17	17	IIN	741.8393	45	45	\sim	\sim
34	7415163	29			3	21	7413245	25	17			IZN	741.5374	45			$ \prec $
4G	(Y2)	29	\leq	\leq	\triangleleft		7418245	27			\prec					\leq	\sim
56	745112	23	23	\leq	\triangleleft	3L		36			4						
		23		\leq	\leq	4L	NVRAM		\leq	$\langle \rangle$	4						
	24404					SL	DELAY	37	\leq	\leq	\leq						
н	745244	14.	14	14	14	GL	74800	7	35								
_	\geq					71	SPARE										
ZH	74L5155	29	\leq	\leq		BL	75452	36									
3H	74L5393	29				19L	7415/53	25									

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 3 of 58)

IR	745240	12	12	12	112
-	5	12	12	12	12
2R	SPARE	+		1	1
3R	SPARE		+	+	+
AR	7413244	12	12	12	.12
		12	112	112	112
-		12	116	112	+'-
	+				
			+	+	-
7R	74LS04	18	7	7	
		34	35		K
BR	74L3138	7	\leq	12	12
9R	741304	7	20		
			1		V
ØR	7415105	35	T		1
IR	74L5157	46			17
	1	1	r	1-	1
BR	741300	49	49	49	+
14R	1793-02	50	17	12	1>
ISR		52	K	6	K
JOR	WDI691	132	K	K	K
	748945	12	1/2	113	115
15	745240	13	/3	13	/3
_	\geq	13	13	13	/3
2.5	SPARE	ļ			
5	74L5240	40	40	<u> </u>	
S	7415244	13	13	13	13
\sum	\sim	13	13	13	13
s	68010	11		1	
5	2732/2764	18		1	1
15	74L5109	34	35	1	
IS IS	74L510	34	21	+	
	and the second		Charles and the second	13-	
9	74L508	6	8	35	
15	7413157	43	4	K,	K
25	6116-4	46	Ζ,	4	K
35	7413195	49	_	\leq	\leq
т	745240	24	24	24	24
\supset	\sim	24	24	24	24
T	74.5393	24	/		and the second division of the second divisio
ST	745157	32	7		7
π	745139	31			
<u> </u>				\sim	
π	SPARE				
T	74508	8	14	6	
T	7413112	8	18	\leq	\leq
T	741.500	7	14	16	
DT	741502	29	43	24	
	74LS175	43	1	21	-

COMPONENT MAP

		-		-	-
131	7415157	50		1	1/
			T	1	T
BT	14LS161	51		17	17
	1	-	1-	F	1-
IV	145244	38	38	38	38
1.4	145244	38	38	38	
-			130	130	130
2∨	74F280	39	K	\swarrow	\leftarrow
37	74F280	39	4	\swarrow	\swarrow
4 V	741.504	3/	3/	30	
					1
67	74A5/000	37	37	37	
TN	7415151	34		17	∇
8	SPARE	1	T	1	1
97	741.582	14	1 .	+	1
10V	74.504	35	50	24	+
		133	50	15	+>
		100	100	K	K
IIV	745260	43	43	\vdash	\triangleleft
21	SPARE.				
4 V	741974	44	51		1
57	4024	51		\square	\square
	1	T	T		T
w	745244	38	38	38	38
	5	38	38	38	38
2W	74L504	40			
SW SW		31	1>	17	+>
	745189		-	120	
4W	741500	31	3/	35	
	<u> </u>				
ŚW	SPARE		L		L.
W	74L508	34	34	38	
BW	74304	35	38	40	
		40			
9W	74L52Ø	16		\square	
ów	741551	35	44		
IW	7415164	43	>	7	
ZW	74,539	44		7	5
	741504	42	42	43	44
BW		51	-TL		
_			Ei		\leq
ew	74LSØ2	51	51	51	51
X	745240	3Ø	3Ø	3Ø	3Ø
\geq	>	3Ø	3Ø	3Ø	3Ø
x	745285	30			\geq
3X	745189	30			5
	746189	32	$ \rightarrow $	\sim	\leq
HK I	74585	33	\leq	\leq	4
*	14363	35	2	\leq	\leq
	0000 mm carried and a range				

-		-	-	-	
GX	745240	34	-		
-	$\geq \leq$	37	37	37	1
XF	745189	34	-	\geq	\swarrow
BX	The second s	30	37	38	
9X	741321	6	_	\swarrow	\mathbb{Z}
KOX	74530	35	1	12	\square
IIX	74510	40			
12X	And the second se	44	1	\square	\square
13X	741551	51	51		\square
14×	741374	51	5/	\swarrow	
		1			
IY	74 5240	8	9		
	\mathbb{P}	39	39	39	39
ZY	745283	3Ø	-	\square	
37	745189	3ø		\mathbb{Z}	2
44	745189	32	\checkmark		\square
5Y	74585	33		\square	
64	PAL	40	\checkmark	\mathbb{Z}	\checkmark
TY	SPARE				
BY	74508	6	22	35	
97	SPARE				
IPY	74524Ø	37	37		
		35			
114	SPARE				
12Y	74L5138	44		\square	\checkmark
13Y	74L5629	52		\bigvee	
12	745244	31	31	3/	3/
	\geq	39	39		
2₹	745283	31			
3£	745189	31			\square
48	745189	33	\sim		\geq
52	74585	33	\square		\geq
62	74574	22	23		\geq
72	DECODER	9	\geq		\geq
BZ	DECODER	10	\geq	\geq	\geq
92	SPARE				
102	74311	37	37	40	
112	7419138	42	\angle	\square	\angle
12문	SPARE				
52	741.508	42	43	44	
142	7415221	5/	51	\square	\geq
A DOMESTIC OF	CONTRACTOR OF THE OWNER	-			

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 4 of 58)

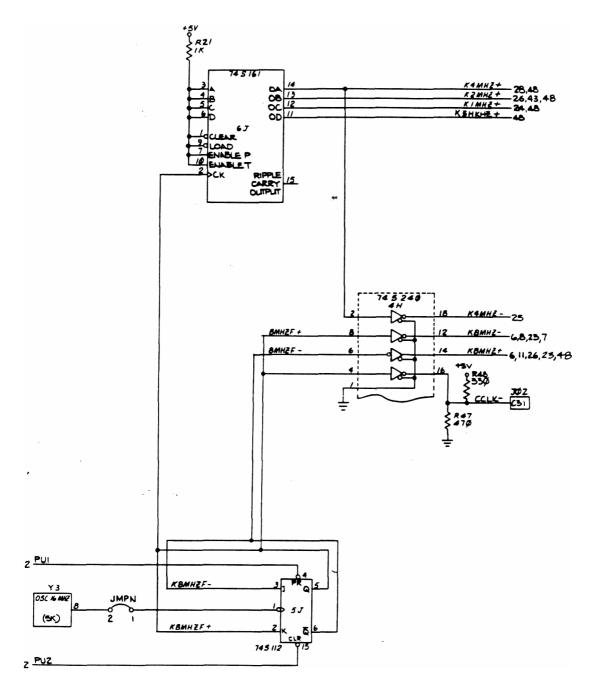
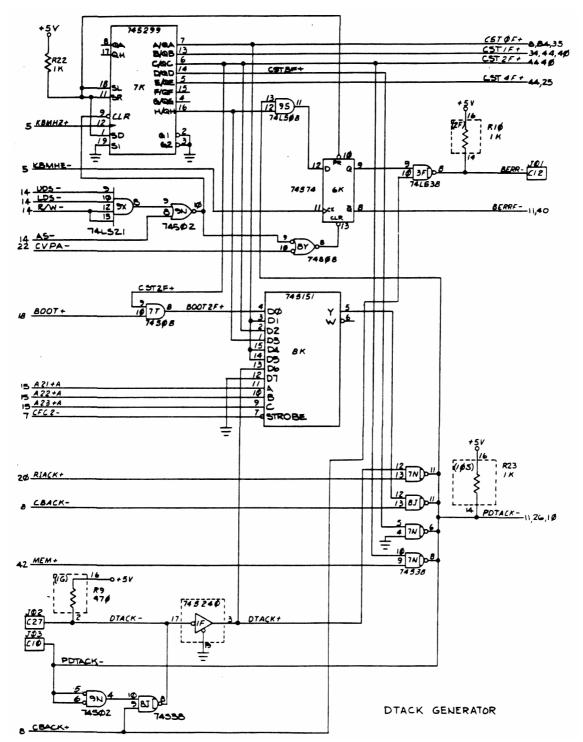


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 5 of 58)





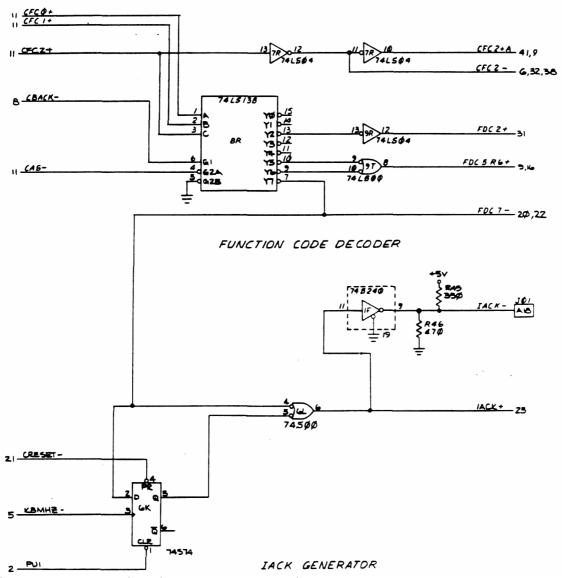
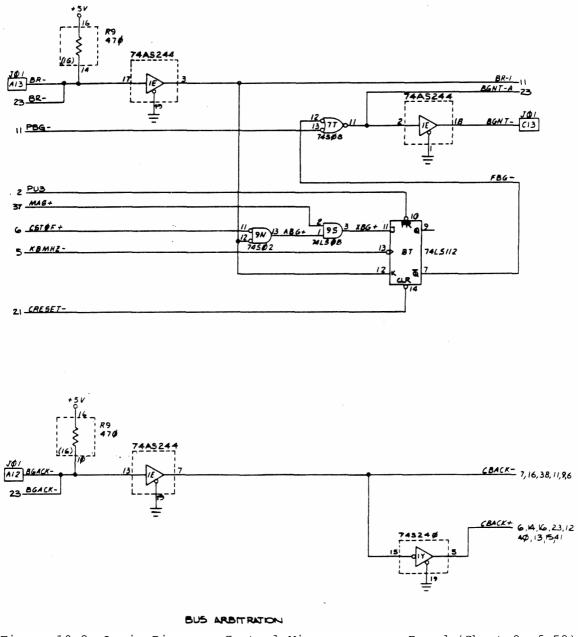
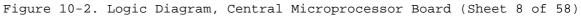
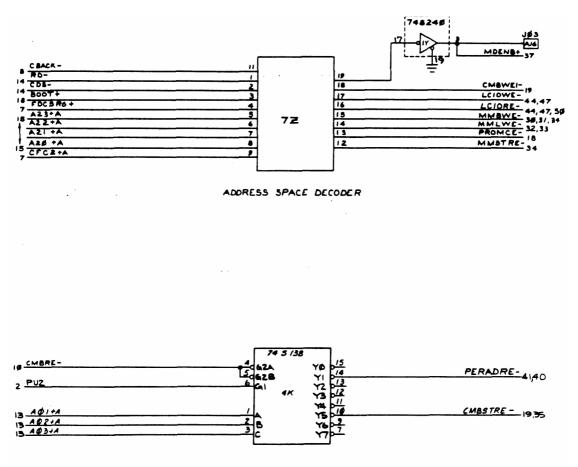


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 7 of 58)

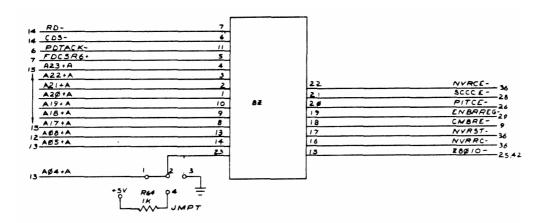




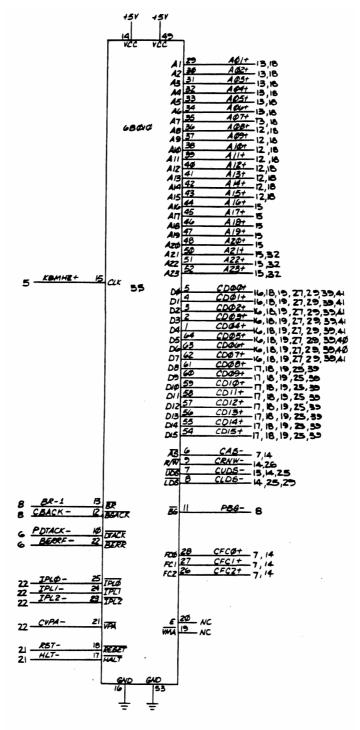


READ STATUS DECODER

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 9 of 58)

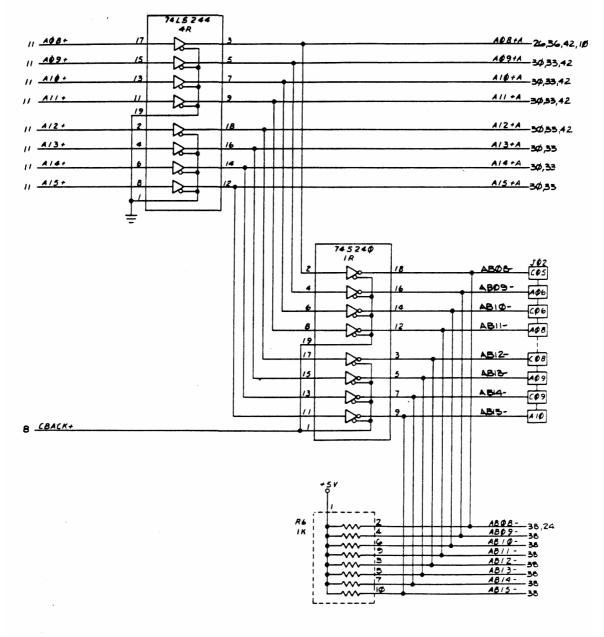


LOCAL 1/0 DECODER Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 10 of 58)



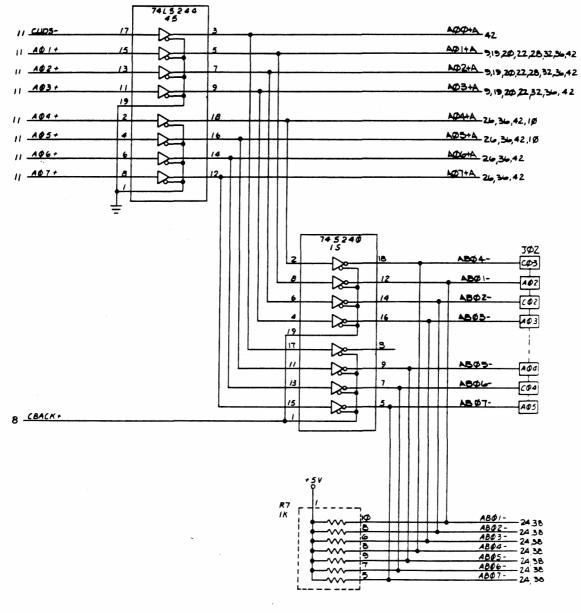
MICRO PROCESSOR

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 11 of 58)



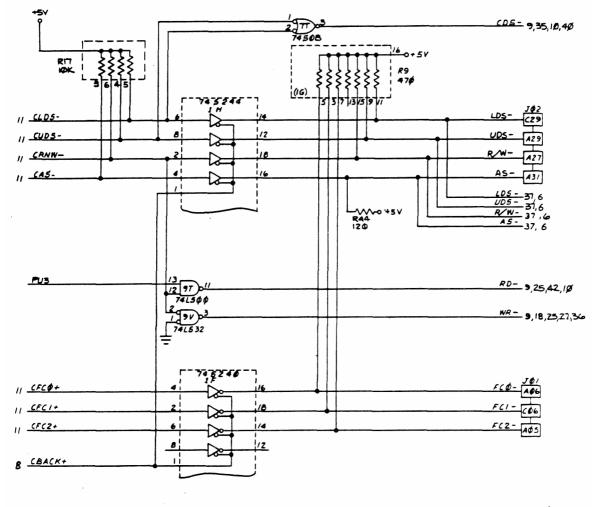
ADDRESS DRIVERS

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 12 of 58)



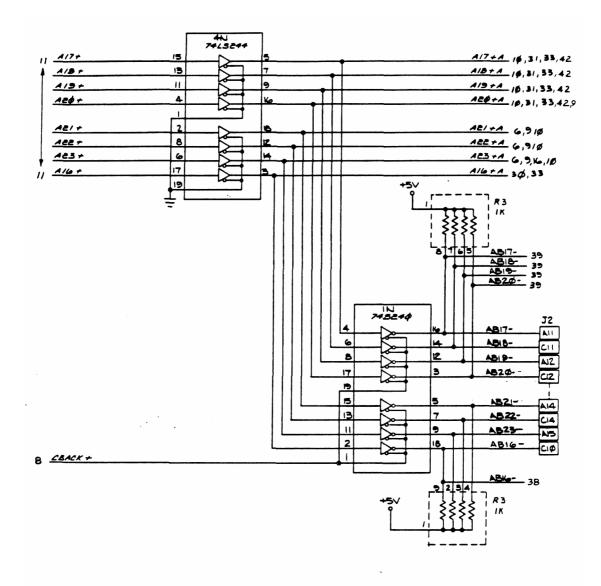
ADDRESS DRIVERS

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 13 of 58)



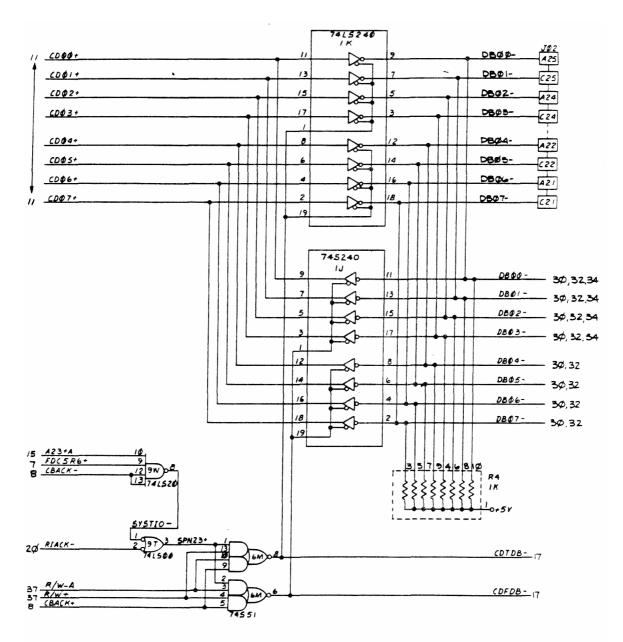
SYSTEM BUS CONTROL

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 14 of 58)



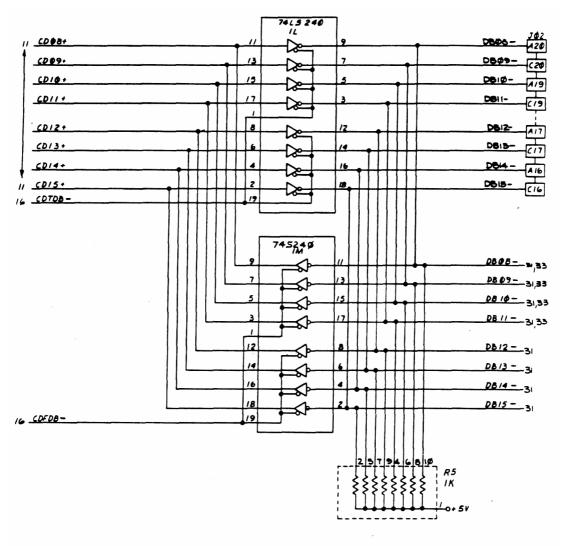
ADDRESS DRIVERS

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 15 of 58)



DATA BUS BUFFER

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 16 of 58)



DATA BUS BUFFER

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 17 of 58)

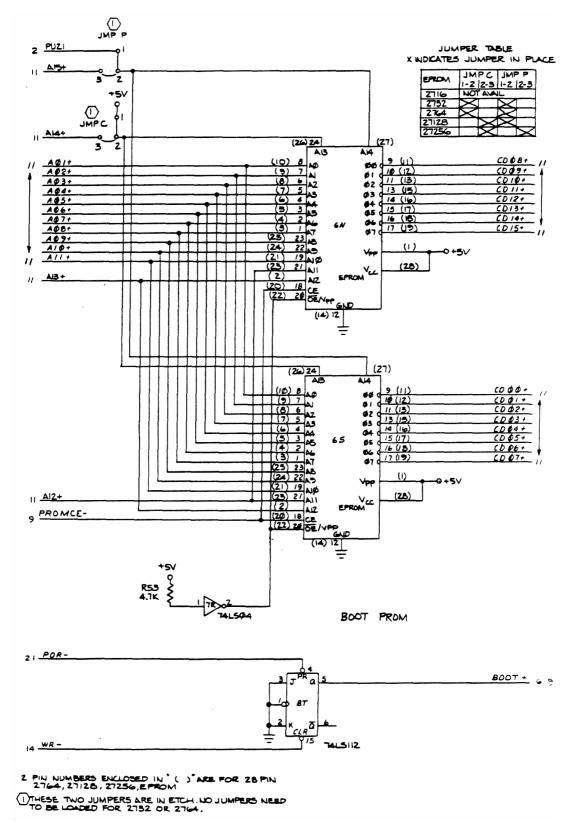
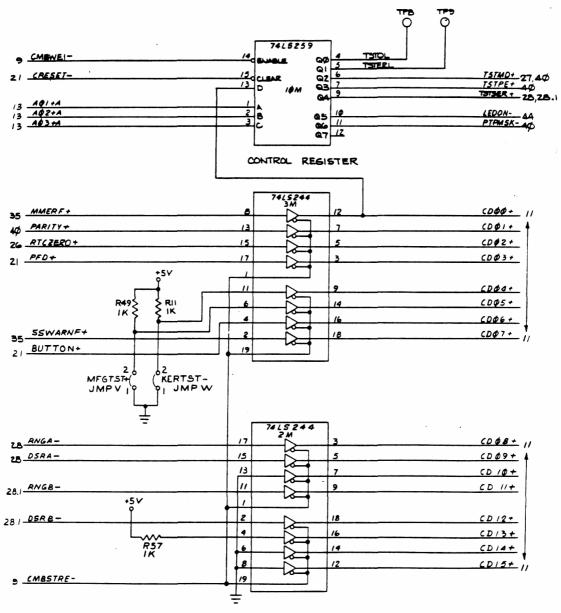
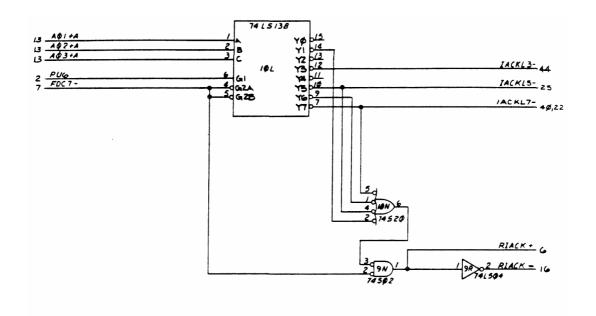


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 18 of 58)



STATUS DRIVERS

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 19 of 58)



INTERRUPT ACKNOWLEDGE DECODER

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 20 of 58)

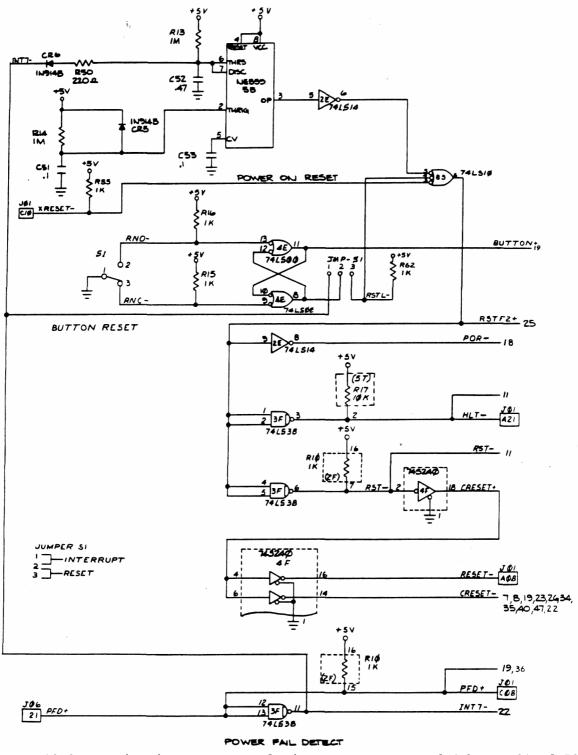
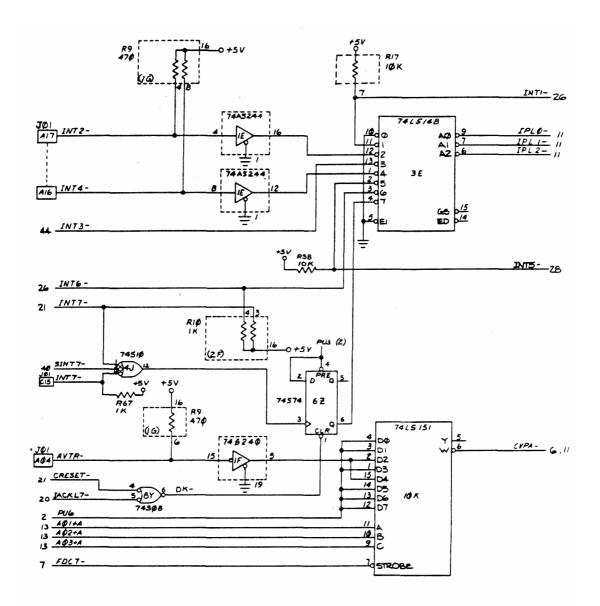
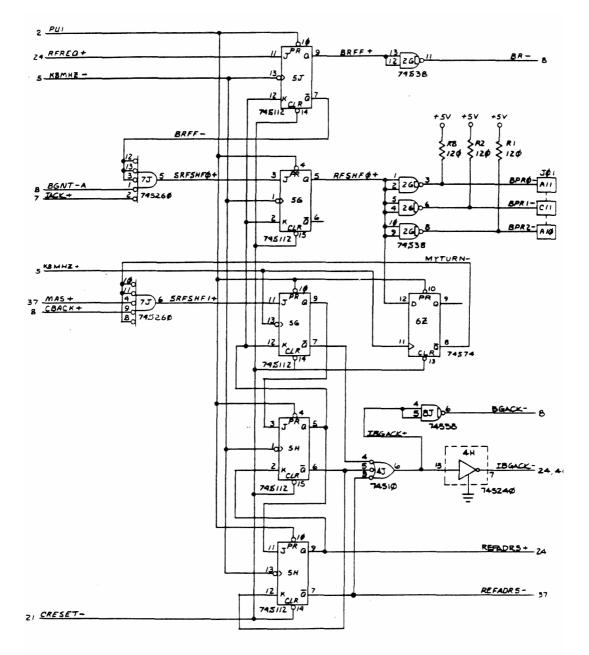


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 21 of 58)



INTERRUPT CONTROL LOGIC

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 22 of 58)



REFRESH ARBITRATION

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 23 of 58)

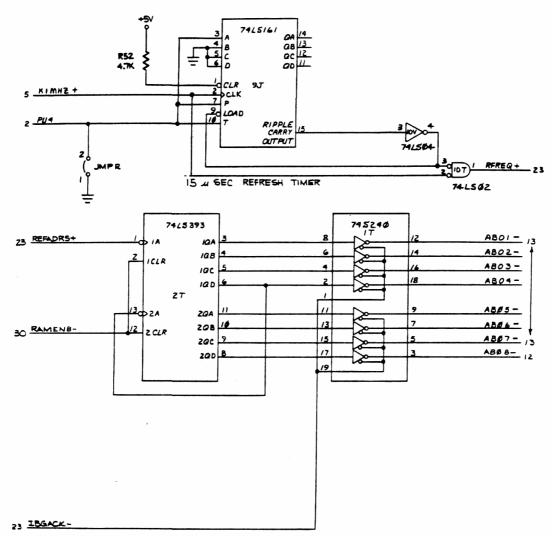
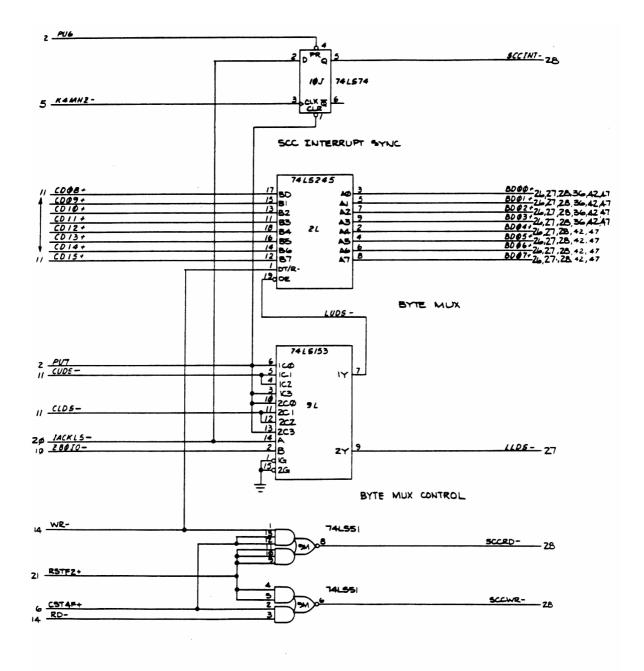
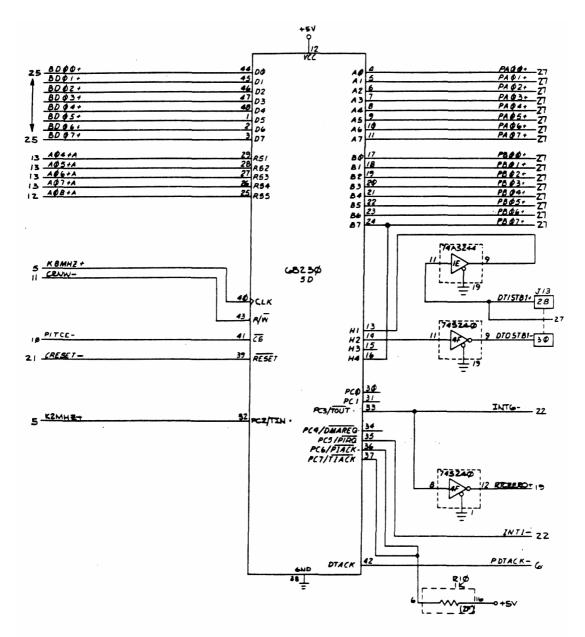


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 24 of 58)



SCC R/W CONTROL

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 25 of 58)



PARALLEL INTERFACE AND TIMER

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 26 of 58)

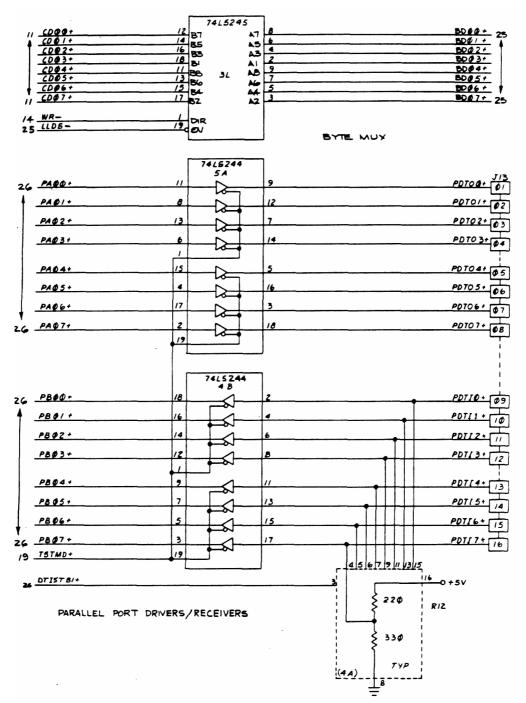
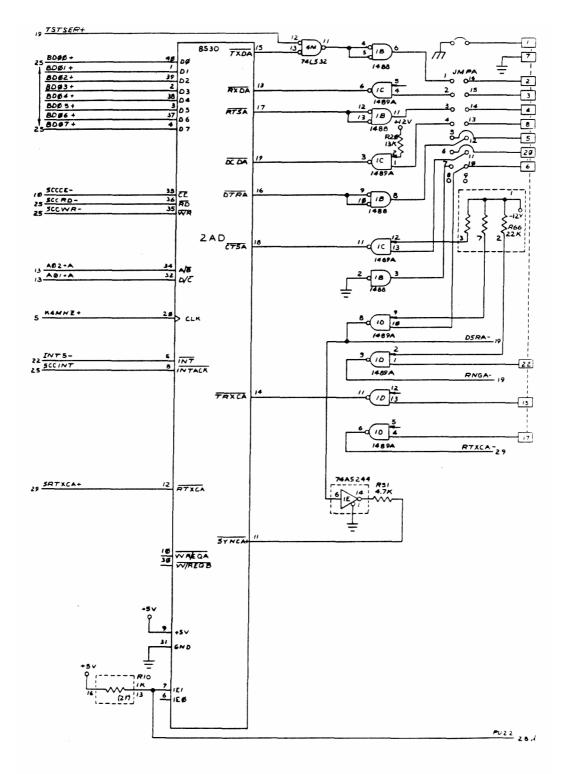


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 27 of 58)



SERIAL PORT A Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 28 of 5)

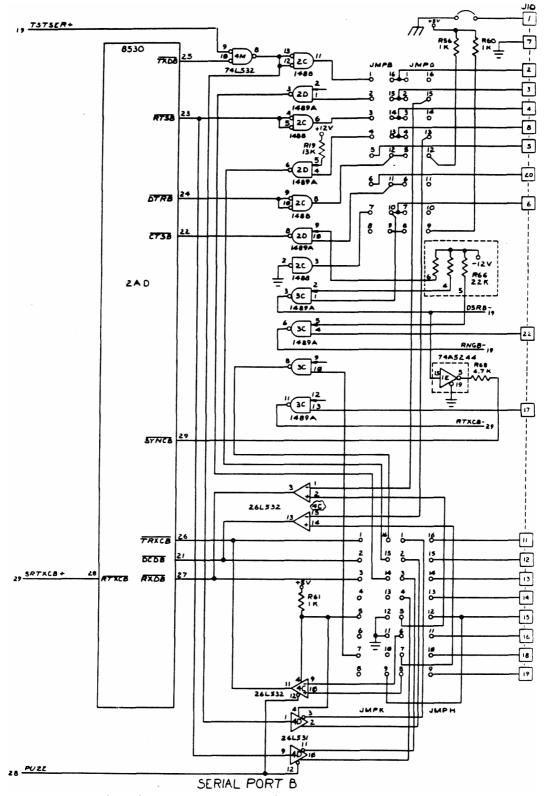


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 28.1 of 58)

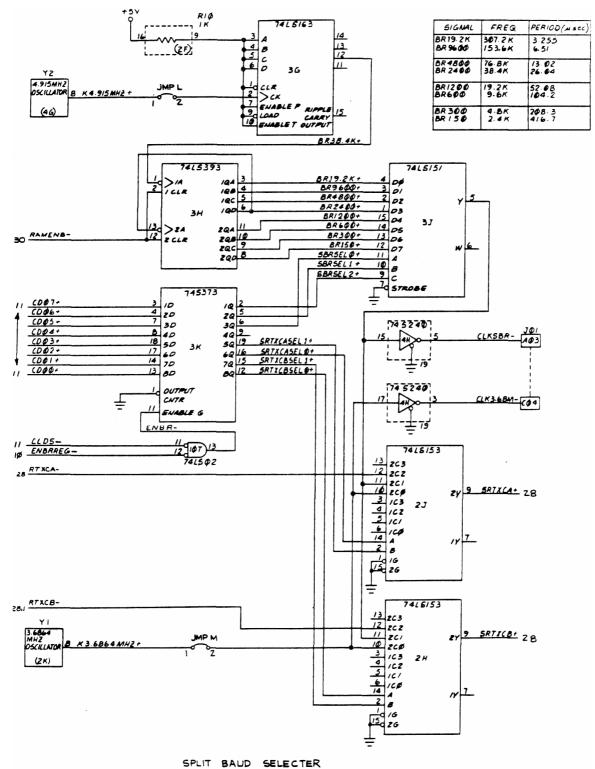
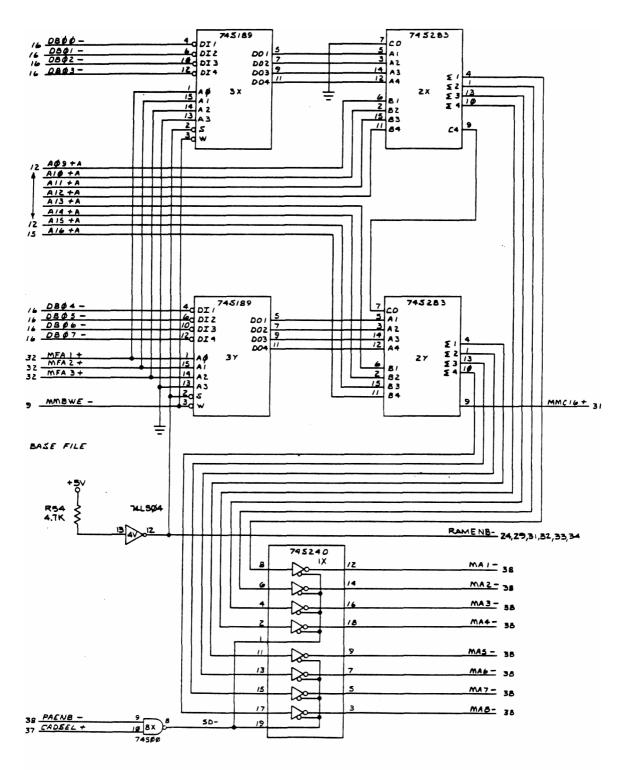
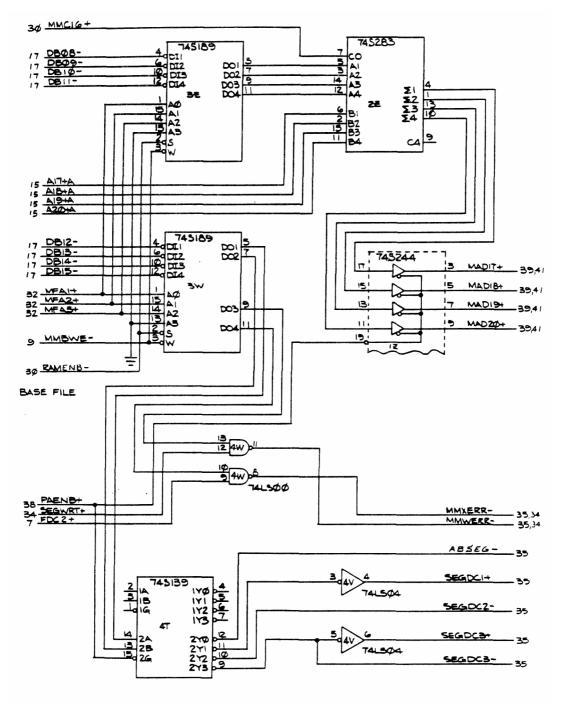


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 29 of 58)

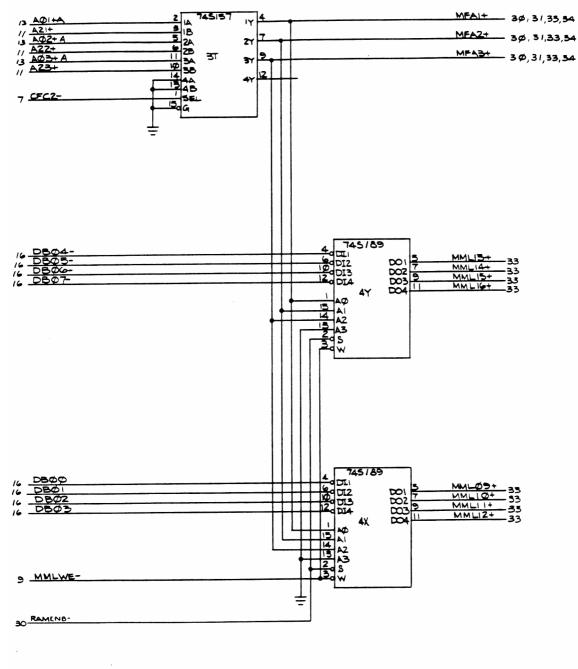


MEMORY MANAGEMENT UNIT Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 30 of 58)



MEMORY MANAGEMENT UNIT

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 31 of 58)



MEMORY MANAGEMENT UNIT

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 32 of 58)

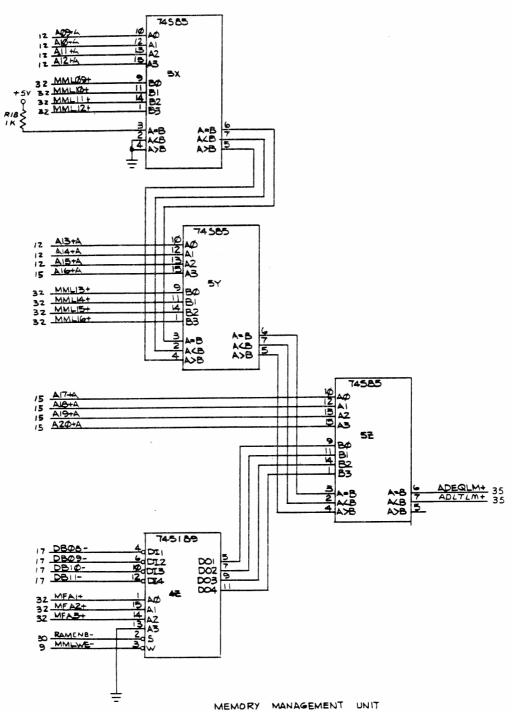
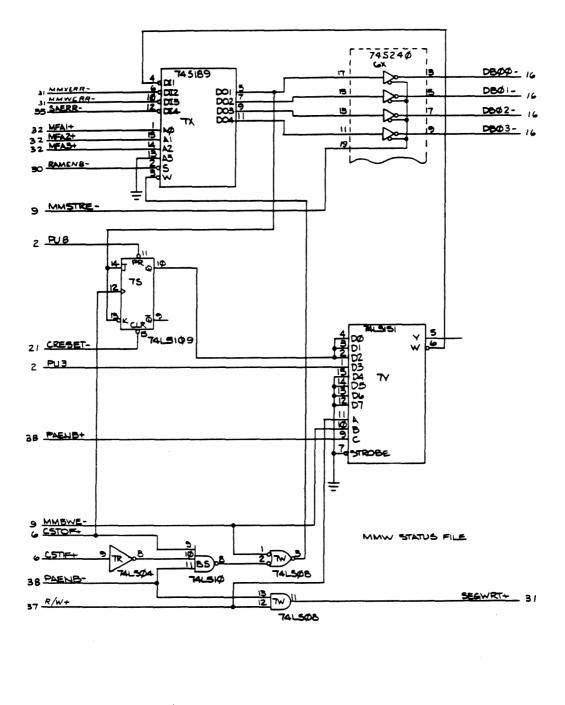
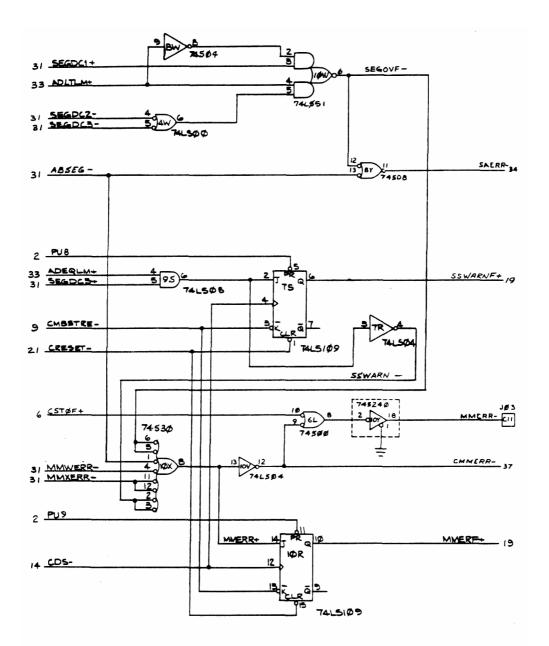


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 33 of 58)



MEMORY MANAGEMENT UNIT

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 34 of 58)



MEMORY MANAGEMENT UNIT

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 35 of 58)

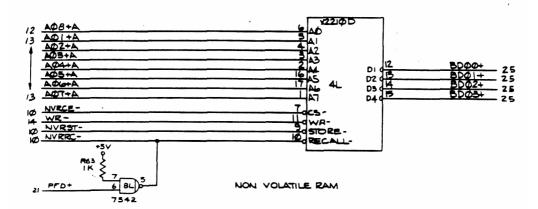
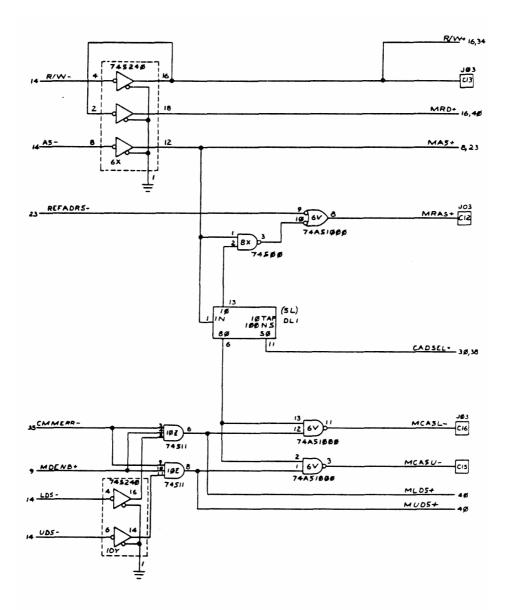
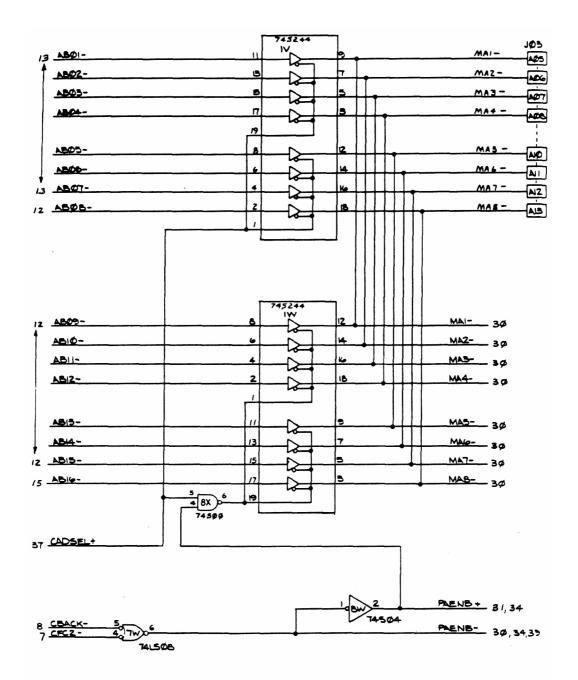


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 36 of 58)



MEMORY TIMING Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 37 of 58)



MEMORY ADDRESS BUFFERS

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 38 of 58)

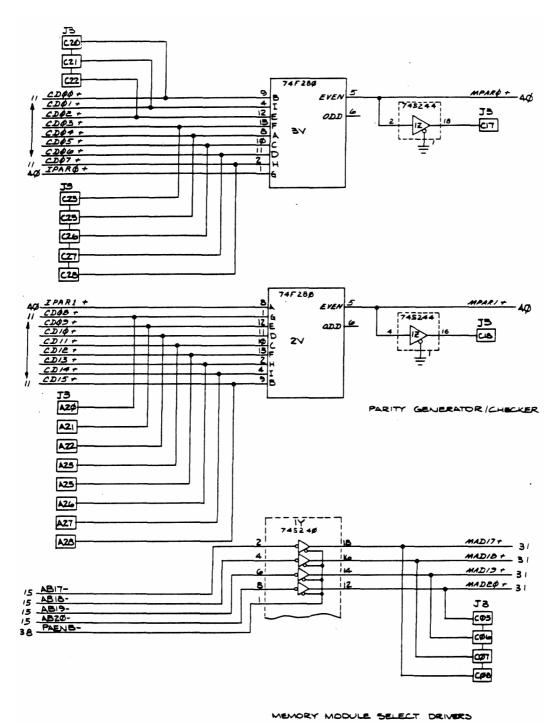
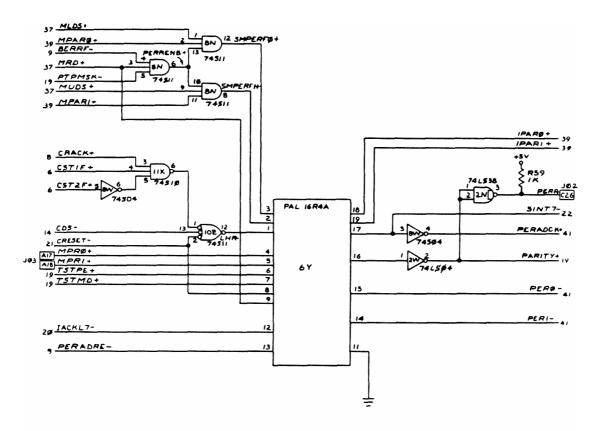
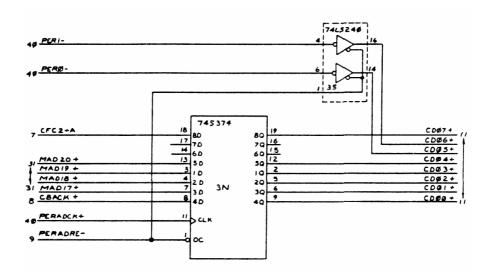


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 39 of 58)



PARITY LOGIC
Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 40 of 58)



PARITY ERROR REGISTER Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 41 of 58)

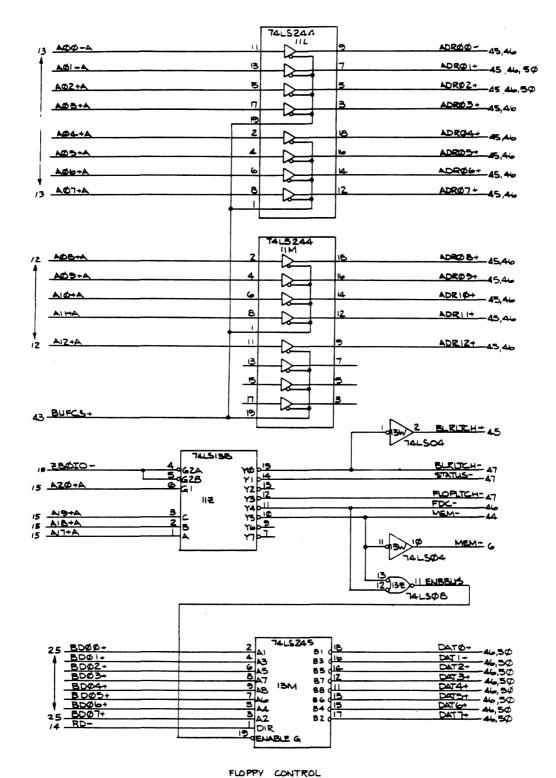
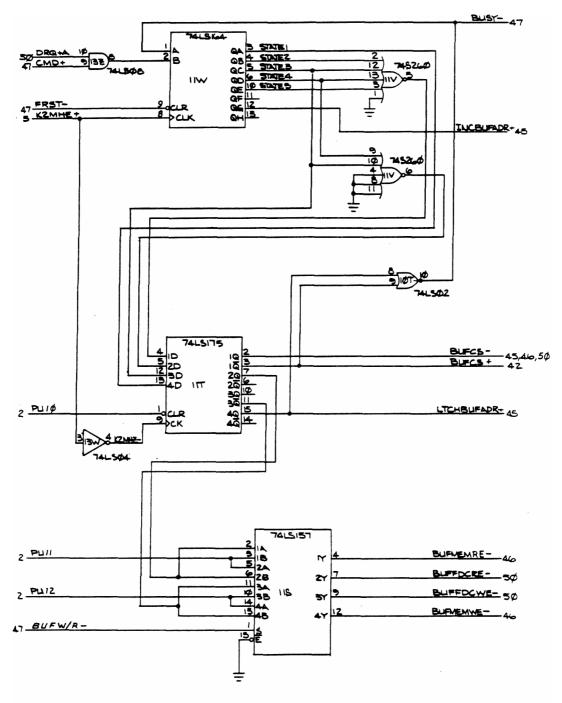


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 42 of 58)



FLOPPY BUFFER STATE MACHINE

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 43 of 58)

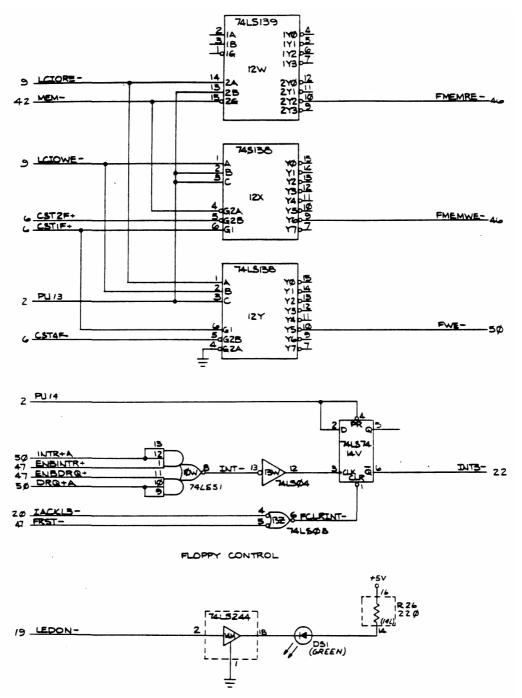
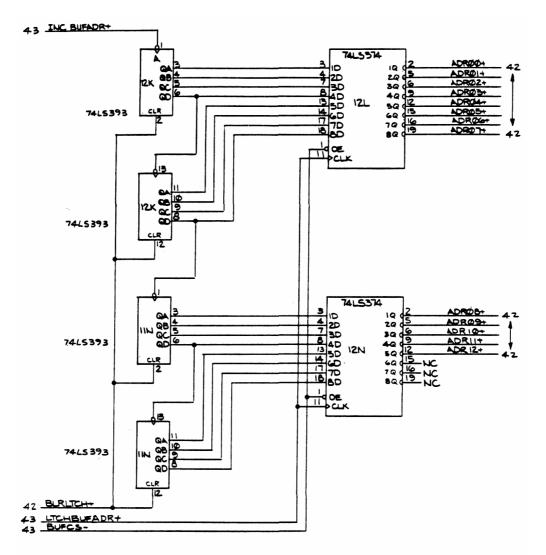
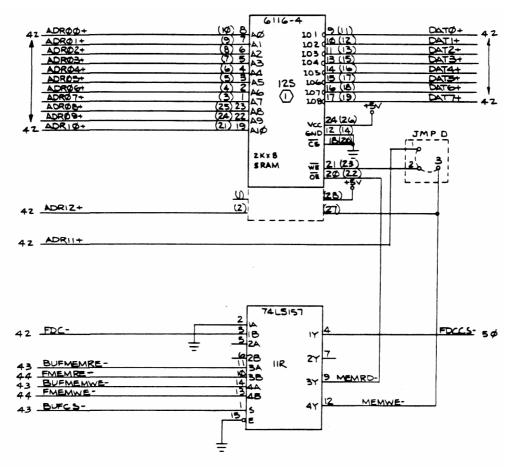


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 44 of 58)



FLOPPY BUFFER ADDRESS COUNTER

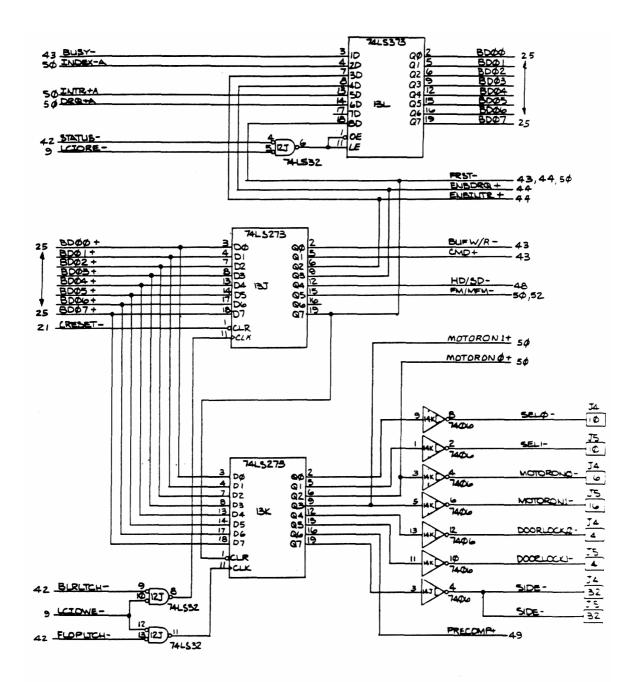
Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 45 of 58)



FLOPPY DATA BUFFER

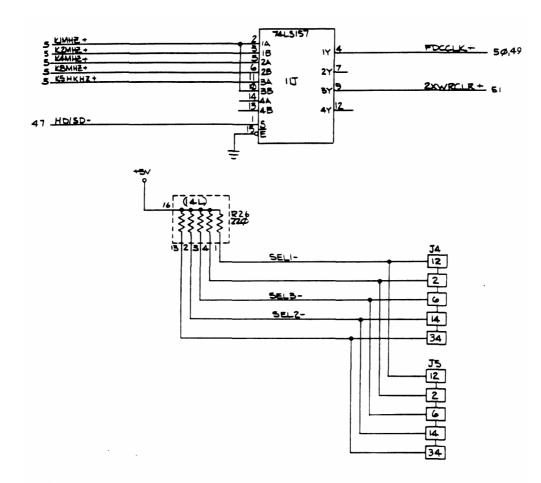
() OCATION 128 PIN DESIGNATIONS IN PARENTHESIS ARE FOR 24 PIN I.C. CONFIGURATION.

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 46 of 58)

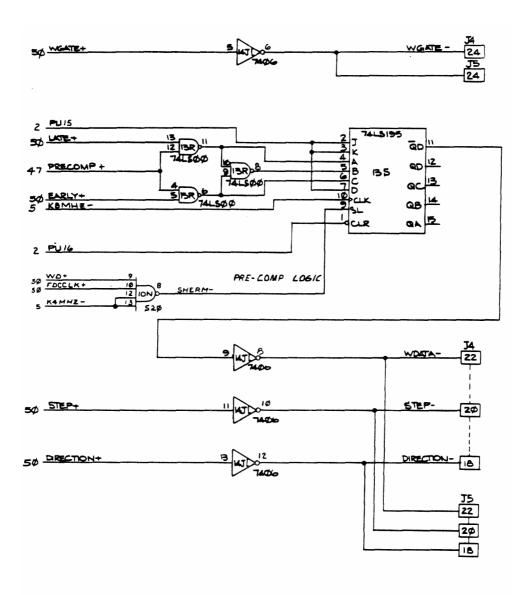


FLOPPY DRIVE INTERFACE

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 47 of 58)



FLOPPY DRIVE INTERFACE Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 48 of 58)



FLOPPY DRIVE INTERFACE

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 49 of 58)

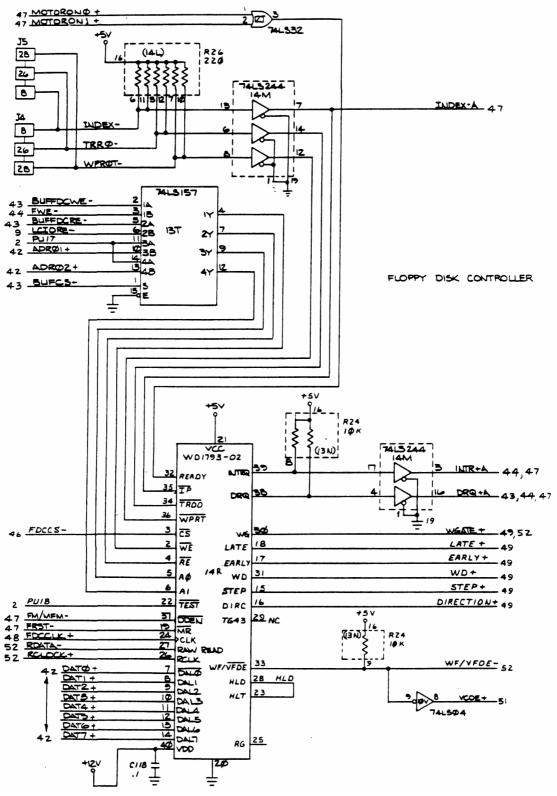


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 50 of 58)

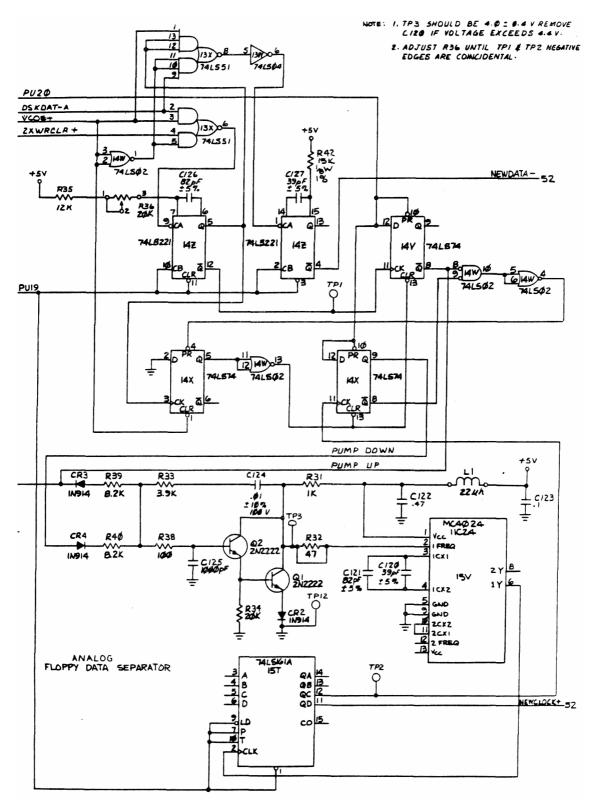


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 51 of 58)

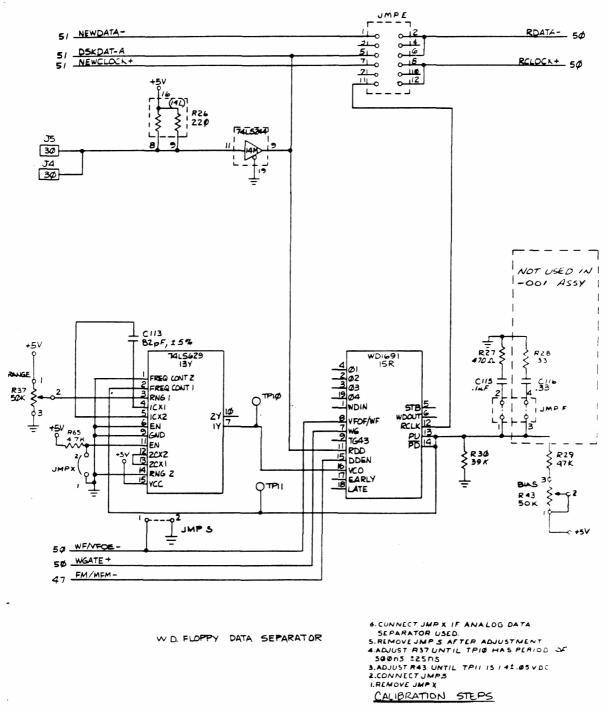


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 52 of 58)

JI	GND		JI	GND
AI			[c/]-	Contractory of the Contractory o
A2-	+5 VDC	-	C2-	+5 VOC
A3-	CLKSBR-	- 29	C3-	GND
Ad	AVTR-	- 22	CA-	CLK 3.68M-
AS	FC2-	-/4	C5-	GND
	FCO-	-/4	6	FCI-
A6-	GND	-/-		6ND 14
A7 -	RESET-	-	C7-	PFD+
AB	GND	- 2/	<u>C8</u>	GND 21
19-	BPRZ-	-	C9-	
AID		- 23	CIS-	and the second
A11-	BPRØ-	- 23	C/1	BPR123
A12_	BGACK-	- 8	CIZ-	BERR- 6
A13-	BR-	-8	C/3-	BGNT- B
A/4	GND		C/4-	GND
	INTG-	_		INTT-
A15-	INTA-	-	C15-	INT5- 22
A16	INTZ-	- 22	C16	INT3-
A17-	IACK-	- 22	C17	INTI-
A/8-	GND	-7	C18-	GND
A19-	+5 VDC	-	C/9	+5 VDC
A20-		-	(20-	and the second secon
AZI	HLT-	- 21	C21	-5VDC
A22-	-12 VDC	-	CZ2-	-12 VDC
A23 6	NO (+IZV RETURN	2	CZ3 6	ND (-IZV RETURN)
A24	+12 VOC		C24	+12 VDC
A25	+5 VDC		C25	+5 VDC
	GND	-		GND
A26-	+5 VDC	-	C26	+5 VDC
A27-	+5 VDC		C27	+5 VDG
A28	GND		C28-	GND
AZ9-	+5 VDC		c29-	
A3Ø-		-	C30	+5 VDC
A31-	+5 VDC	-	C3/	+5 VDC
432	GND		C32	GND

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 53 of 58)

J2	e		JZ	<i></i>
A/-	GND		61-	GND
AZ	A80/-	/3	CZ	A B 02-
43	A803-	- /3	- 63	A804-
44	AB05-	— /3	C4	AB\$6-
	A807 -			A808-
A5 -	A809-	- /3	<u>cs</u>	A810 -
A6	GND	_12	<u>c</u> 6	GND
A7 -	AB//-		C7	A8/2-
A8	A0/3-	<u> </u>	C8	AB/4-
A9	A8/5-	— /Z	C9	
A10-		- 12	C10-	48/6-
A11-	A8/7-	- 15	C//	AB/8-
A/2	A8/9-	- 15	C/2	A820-
4/3	GND	_	C/3	GND
A/4	ABZ/-	- /5	C/4	A822-
1/5	AB23 -	-		SPARE
	0814 -	- 15	C/5	D815-
4/6	08/2-	- 17	C/6	08/3-
4/7	GNO	- 17	C/7	GND
a/8	0810-	-	C18	DB//-
1/9	0808-	- /7	C/9	0809-
120	0806-	- 17	C20	
421-		- 16	C2/	0807-
222	0804-	- 16	C22	0805-
723	GND	_	C23	GND
24	0802-	- 16	C24	0803-
25	D800-	-16	C25	0801-
26	SPARE	-	C25	PERR-
_	R/W-	-5		DTACK-
27	GND	-/4	C27	GND
78	UDS -	-	C28	LDS -
29	GND	-/4 .	C29	
30-		-	C3Ø	GND
3/	A5 -	-/4	C3/	CCLK-
32	GND	_	C32	GND

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 54 of 58)

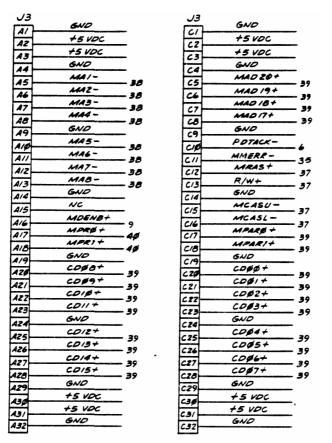
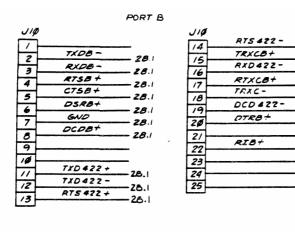


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 55 of 58)

J4	(1000)			J5	_	(FDØI)	
	GND				}	GND	-
2 -		48		2	}	C110	- 48
3-	GND			З	┣—	GND	-
4	DOORLOCKØ-	47		4	1	DOORLOCK 1-	- 47
3-	GND .			5	1	GND	-
		48		6			- 48
19-	GND			7		GND	-
17-	INDEX-					INDEX-	
8-	GND	5¢		B		GND	- 5 ø
9-	SEI D			9		SEL1-	-
10	GND	47		Þ		GND	- 47
	GND			11	├	Gilly	-
12	CUD	48		12		GND	- 48
13-	GND			15		GNU	-
14-		48		14		4	- 48
15	GND			15		GND	-
16-	MOTORONØ-	47		16		MOTORON 1-	- 47
HT-	GND			17		GND	-
18	DIRECTION-A	49		18		DIRECTION-B	- 49
	GND					GND	
19	STER A			10		STEP-B	-
20-	GND	49		20		GND	- 49
21		21		21		WDATA-B	-
22-	GND	49		22		GND	- 49
23-	WCATE-A			23			-
24		48,	49	24		WGATE-B	- 48, 49
25-	GND			25			-
26-	TRRØ-	5Ø		26		TRRØ -	-5Ø
27-	GND			27		GND	-
28-	WPROT-	5Ø		28		WPROT-	- 5Ø
29-	GND			29		GND	-
30-	DSKDAT-			30		DSKDAT-	-
31-	GND			31		GND	-
32-	SIDE-A	47		32		SIDE-B	- 47
33-	GND			33		GND	-
34-				34			-
<u>ג</u>	TOVSENSE				<u>J6</u>	+5V RTN 58	NSE
1	+51				Δ	+5Y RTN	
2	+5				В	+5V RTN	
3	+5				С	+SV RTN	
4	+5V				D	+5VRTN	
5	+5V				E	+5V RTN	
6	+5V				F	+5V RTN	
–					I		
e	+51	·			J	+5V RTN	
9	+50			1	ĸ	+ SV RTN	
19	7 +5∨				L	+5V RTN	
					M	+ 5V RTN	
				ł		+5V RTN	
12					ZD	+5V RTN	
1					P	+5V RTN	
4					R	+SV DRIVE F	TN
1	-5~				5	-SV RTN	
10	+121/				T	+12V RTN	
71	-12V				U	-IZV RIN	
18	+5V COLTER				<	12V RTN	
19	HON CONTRO				W	AUXILLIARY	BTN
20	0	(1)	C1	1	X		
2	PFD+		21		Y	AUXILLIARY	RIN
2					Z		(NC)
							>

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 56 of 58)



- 28.1

- 28.1

. 28.1

28.1

-28.1

28.1

28.1

28.1

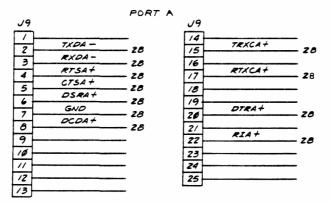


Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 57 of 58)

)13		JI3
POTOP	<u> </u>	20 GND
POTO I	4 H	21 GND
2 PDTO 2	≠ F	ET GND
5 POTO 3		23 GND
BOTO 4	∡ ⊨	24 GND
5 POTO 5	∡ ⊢	25 GND
7 0006	4 L	26 GND
	4 H	27 GND
9 POTTO	+ -	28 DTISTBI-
10 POTII	_ F	29 GND
II POTI 2		30 DTOST 8/-
POTI 3	+ +	3/ GND
B POTIA	_ _	32 GND
A POTIS	4	33 GND
5 POTI 6		30 GND
6 POTIT		35 GND
7 GND		
8 GND		36
9 GND	L	<u> </u>

Figure 10-2. Logic Diagram, Central Microprocessor Board (Sheet 58 of 58)

Memory Array PCBA

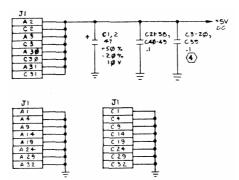
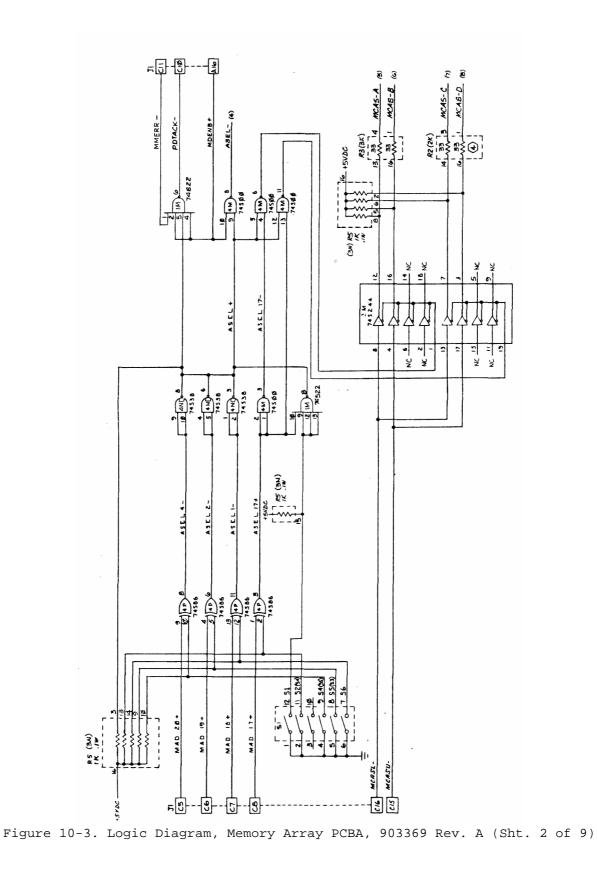


Figure 10-3. Logic Diagram, Memory Array PCBA, 903369 Rev. A (Sht. 1 of 9)



10-64

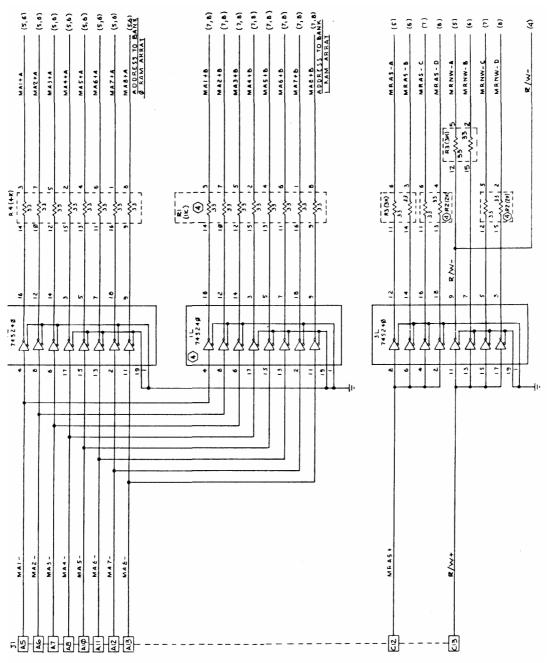


Figure 10-3. Logic Diagram, Memory Array PCBA, 903369 Rev. A (Sht. 3 of 9)

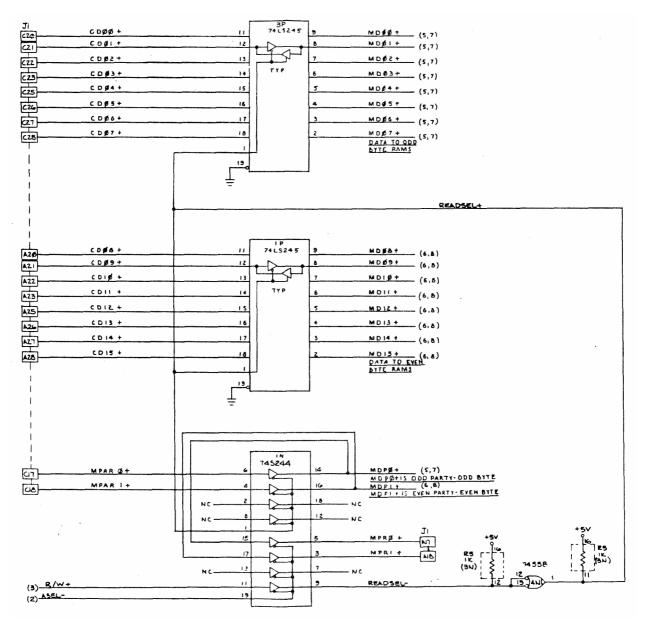


Figure 10-3. Logic Diagram, Memory Array PCBA, 903369 Rev. A (Sht. 4 of 9)

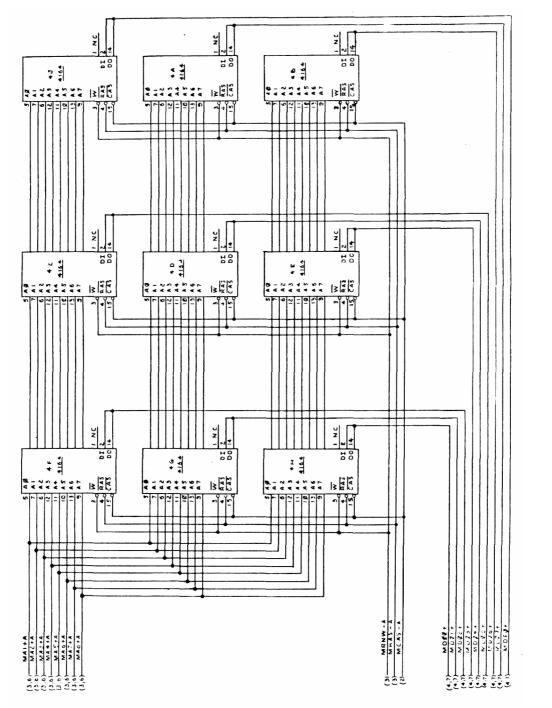


Figure 10-3. Logic Diagram, Memory Array PCBA, 903369 Rev. A (Sht. 5 of 9)

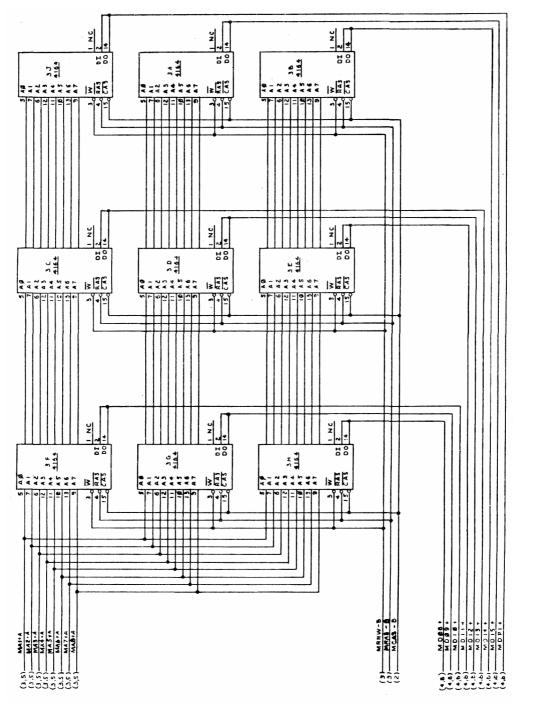


Figure 10-3. Logic Diagram, Memory Array PCBA, 903369 Rev. A (Sht. 6 of 9)

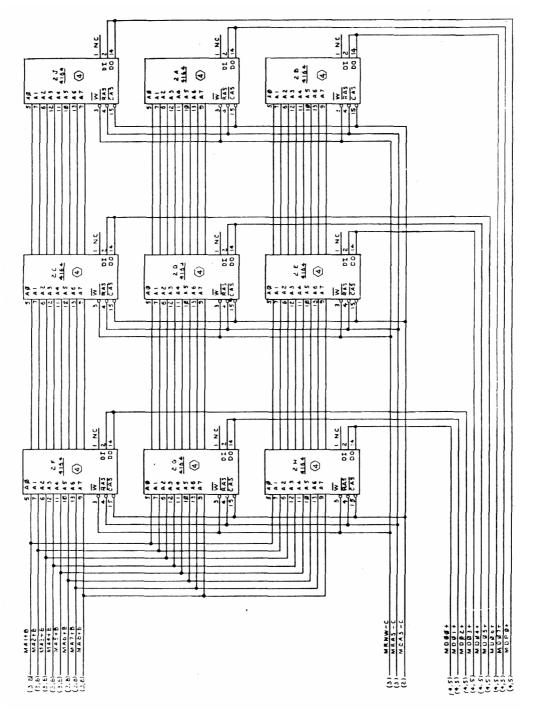


Figure 10-3. Logic Diagram, Memory Array PCBA, 903369 Rev. A (Sht. 7 of 9)

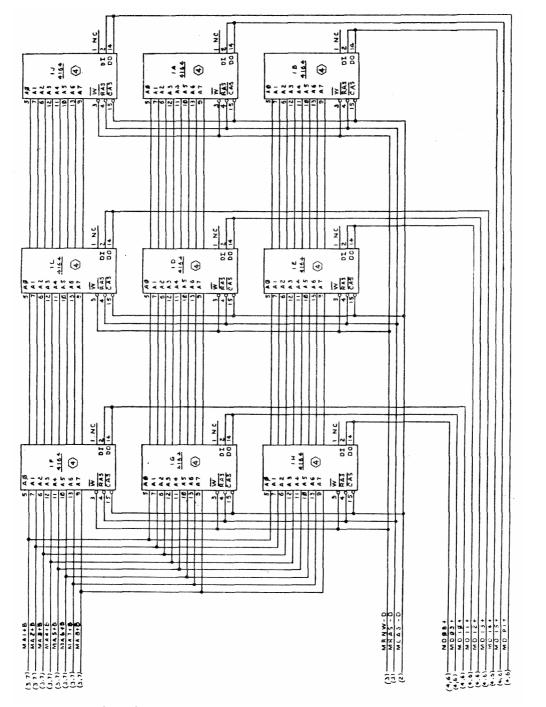
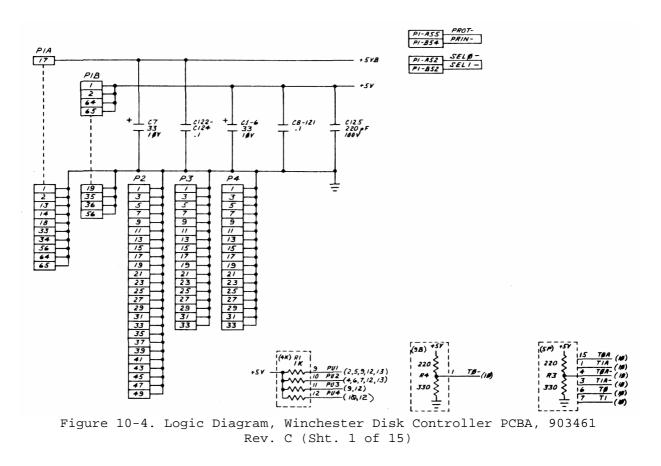


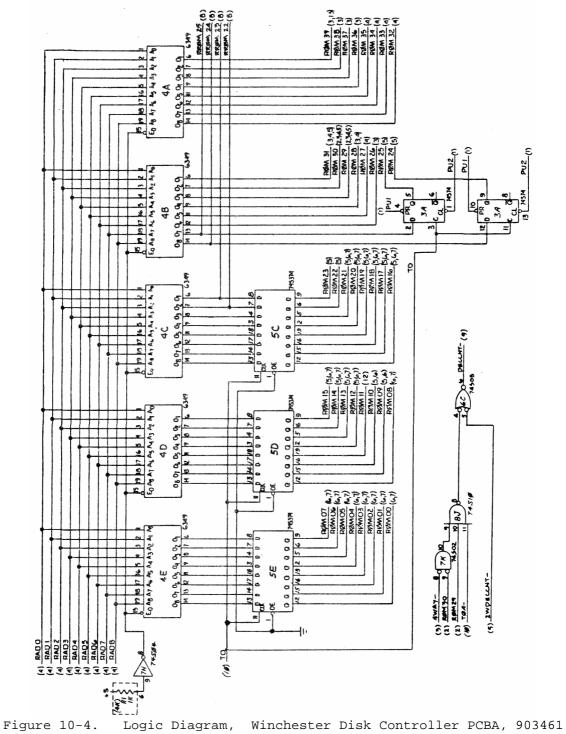
Figure 10-3. Logic Diagram, Memory Array PCBA, 903369 Rev. A (Sht. 8 of 9)

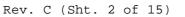
JI		-	
	<u>GND</u> (I)	11	GND
AZ	+ 5 VDC (1)	C 1	15400
A 3	+ 5 Y D C (1)	C 2	+ 5 4 0 6
	GND . (1)	C 3	GND (1)
AS	MA1- (3)	C 4	MAD 2 0+ (1)
AG	MA2- (3)	c 5	1440 184
A 7	MA 3- (3)	C 6	MAD IA+
AB	(3)		MAD 17+ (2)
AB	GND (1)	<u> </u>	GND (2)
	MA 5- (3)	e 0	CDTACK - (1)
AID	MAG- (3)	C 10	MAE 88 - (2)
AIL	MA7- (3)	C 11	MRASA
AIZ	MA 8- (3)	C 12	R/W+ (3)
AI	<u>GND</u> (I)	C 13	())
AIS	NC	C 14	MCASU- (1)
A 16	MDENE + (2)	C 15	16
A 16	<u>MPRØ+</u> (2)	C 16	(2)
AIO	MPRI+ (4)	C 17	MPARUT (4)
	CNID	C IE	GND (4)
A 19	<u>CDØ8+</u> (1)	C 19	(I)
	<u>CDØ9+</u> (4)	C 20	(+)
A21	CD10 + (+)	C 21	(*)
	<u>CDII + (4)</u>	55.2	(4)
A 23	<u>GND</u> (1)	C 23	$\frac{CDP3+}{GND}$ (4)
A 24	(1) + 51 00	C 24	(1) (DØ++ (4)
A 25	CD13 + (4)	C 2 5	CDAS+
A 26	<u>CD14 + (4)</u>	C 26	code (4)
A 27	CD15 + (4)	C 27	(*)
	C 0	C 28	(+)
- 65 A		C 23	+ EVDC (1)
A 30		c 29	(1)
A31	(1)	C 31	(1)
A 32	<u> </u>	C 32	<u> (1)</u>

MEMORY ARRAY BUS CONNECTOR PINOUT

Figure 10-3. Logic Diagram, Memory Array PCBA, 903369 Rev. A (Sht. 9 of 9)







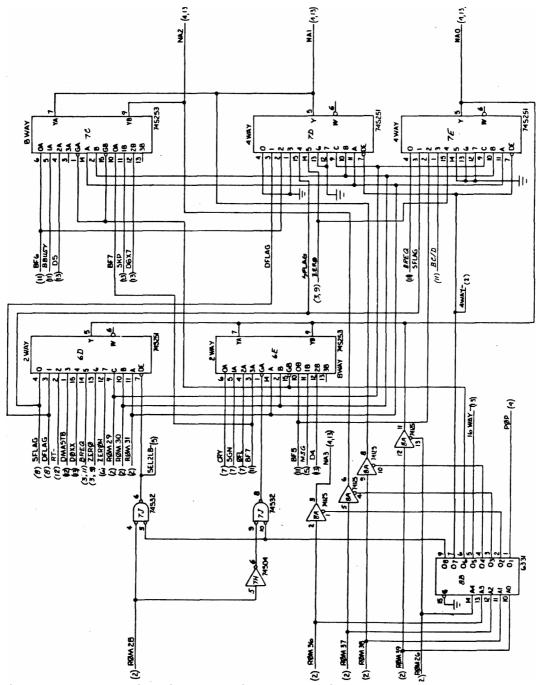
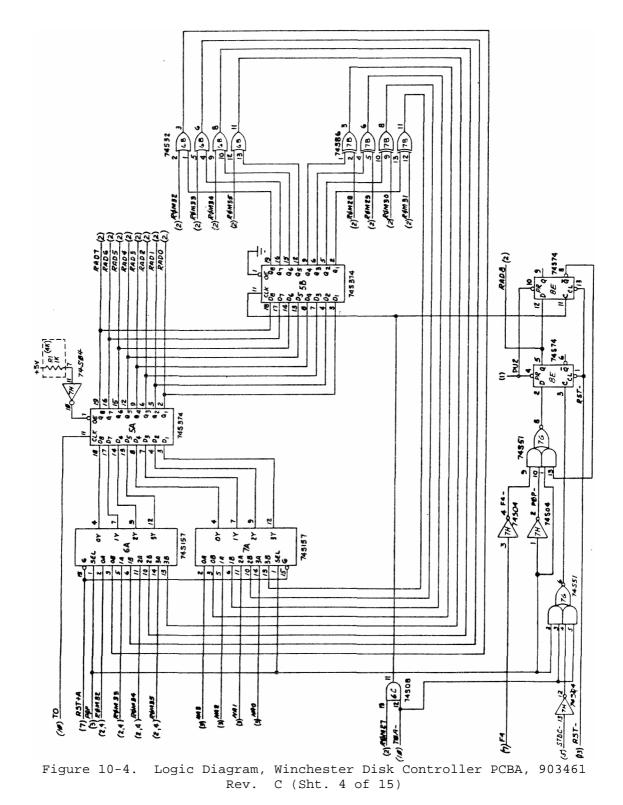


Figure 10-4. Logic Diagram, Winchester Disk Controller PCBA, 903461 Rev. C (Sht. 3 of 15)



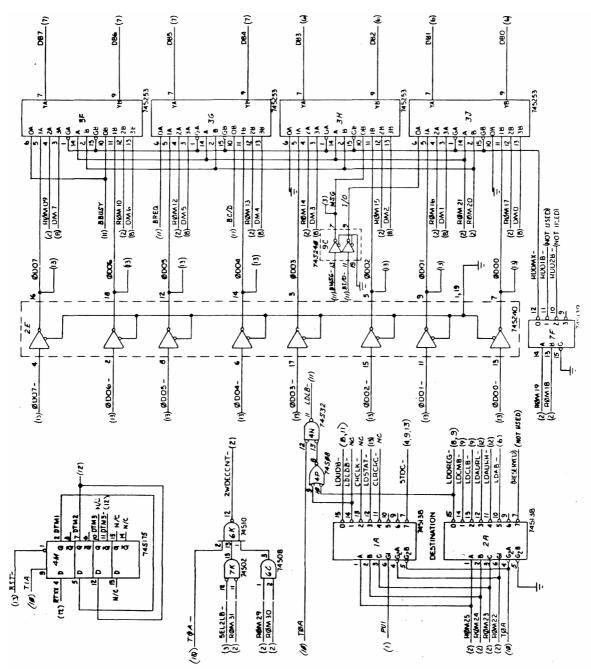
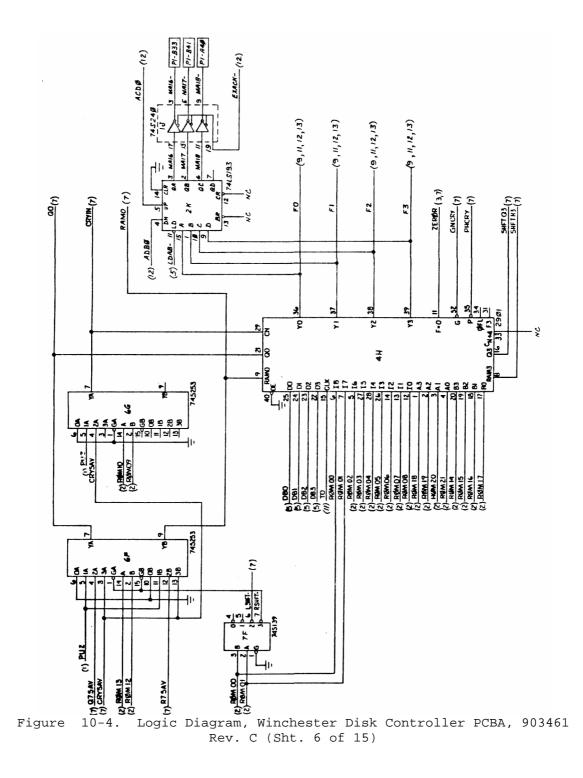
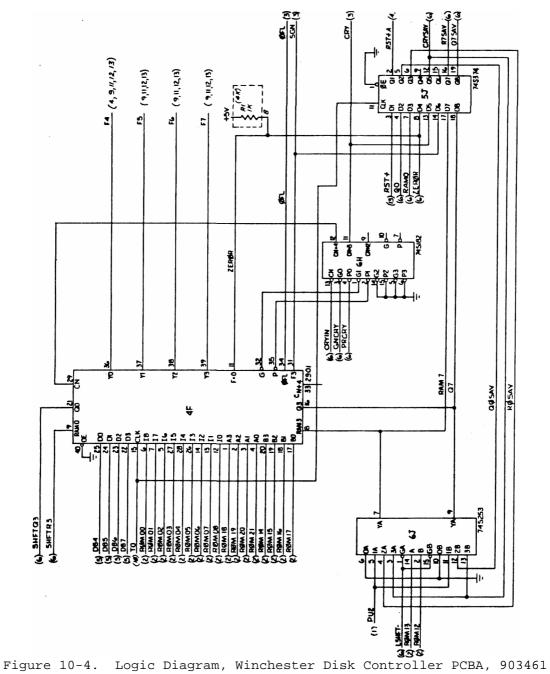
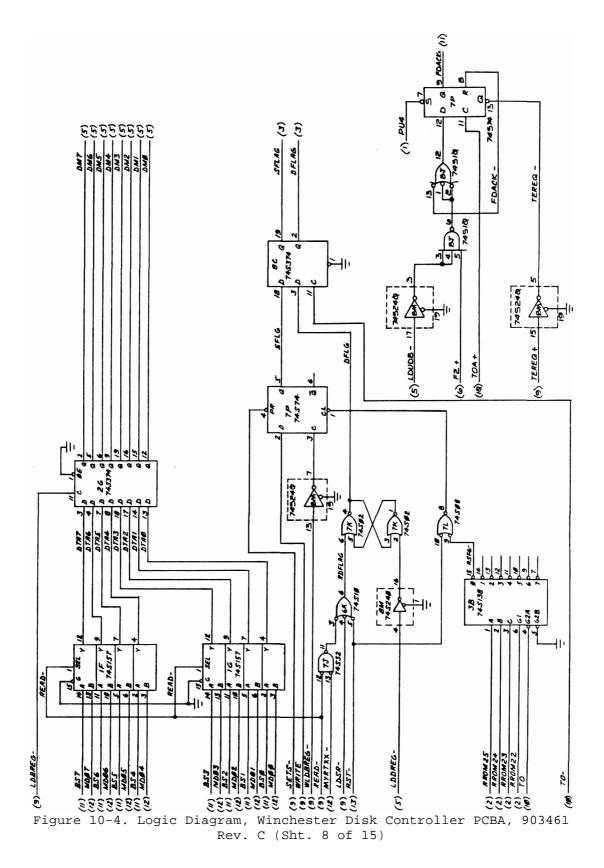


Figure 10-4. Logic Diagram, Winchester Disk Controller PCBA, 903461 Rev. C (Sht. 5 of 15)





Rev. C (Sht. 7 of 15)



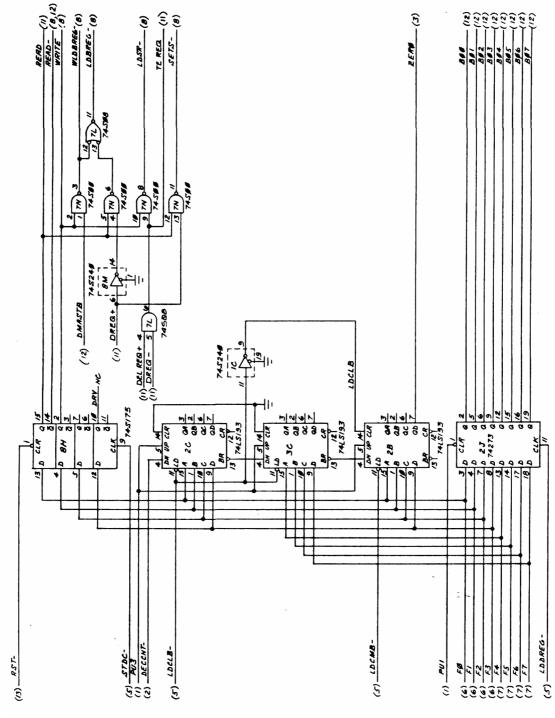
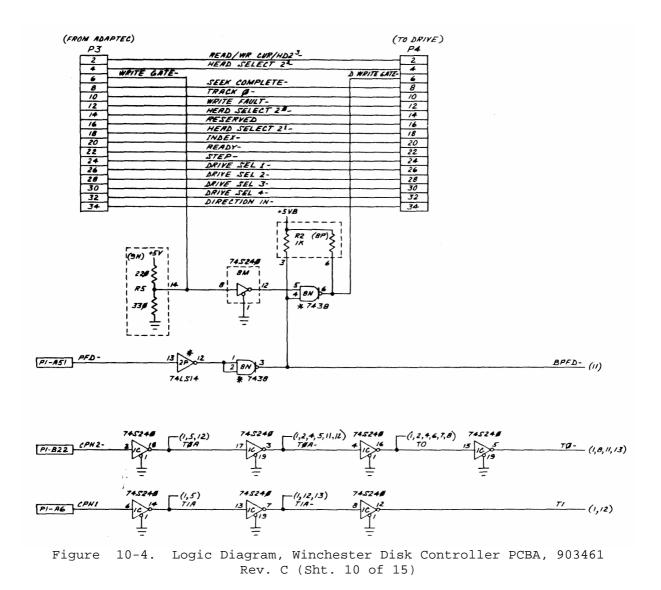
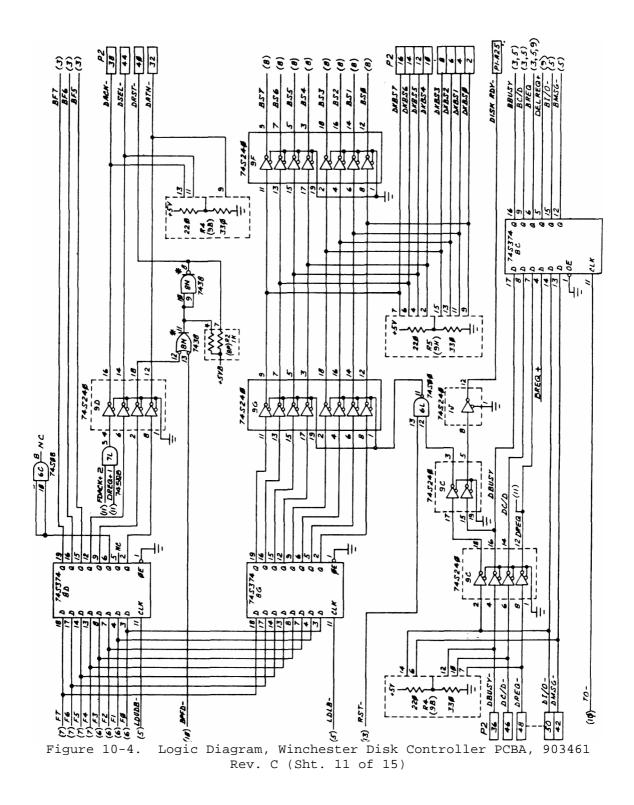


Figure 10-4. Logic Diagram, Winchester Disk Controller PCBA, 903461 Rev. C (Sht. 9 of 15)





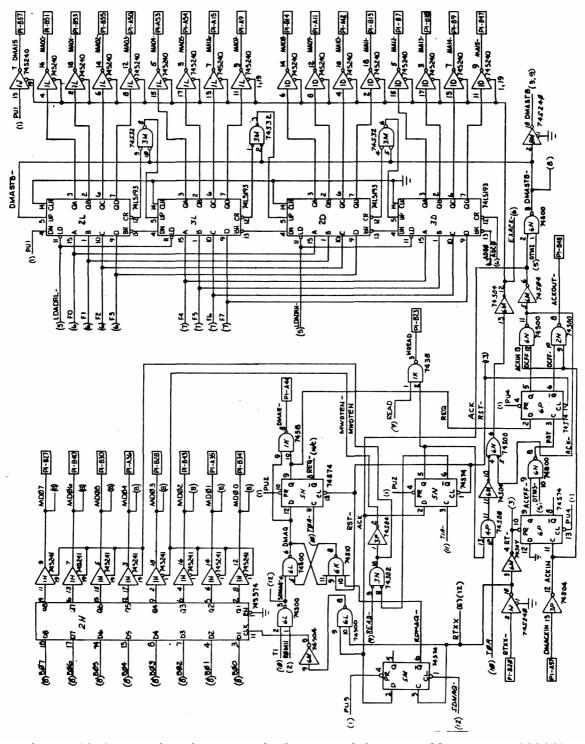


Figure 10-4. Logic Diagram, Winchester Disk Controller PCBA, 903461 Rev. C (Sht. 12 of 15)

PAGE MISSING

This Page was misprinted in my original documentation, is was page 10-85 and 10-87 printed on one page $% 10^{-1}$

PAGE MISSING

AAM 6 8	74/255 J J J	80 745374 8 //	8E 74574 4 4 8F SPARE	86 745374 11 BH 745/75 9	SPARE	BL SPARE	BW 745240 8 9 10 12	11 11 ØI ØI 8242 NB	8P RES NTWX 10 10 11 11			94 SPARE	11 11 11 11 11 11 11 11 11 11 11 11 11	220/330 11 11 11 11	" (***	9C 74S246 5 5 // //	11 11	9E SPARE 13 13 13 13	9F 745246	11 11 11 11 UN 11 11 11 11 11 11 11 11 11 11 11 11 11		11 11 11 11 BEEVANX 10 11 11 11								
2004	2901 SPARE	MA MED MIMA / / / / /	19 19 19 19 19 19 19 19 19 19 19 19 19 1	74532	*	58 745374 4 50 745374 2	1 1	EI EI +25+2 NS	SL SPARE	21 +25+2	50 74574 12 12 1	1 1 022/022		1 22 CLEZ	* * ZES*2	60 745288 2 4 5 11 60 745251 3 1	74.5253	66 745253 6	61 745282 7 61 745253 7	6K 74506 5 8 12	74504 12 12 12	6N 74500 12 12 12 12	74574 12 12	X.	++++	76 745251 3	5 65/5+4	76 74551 4 4 4 4 7H 74594 2 3 4 4	E1 8 E E ZES+1 11	74502 2 5 8
5 95/542 9/ 5 95/542 9/ Figure	10 745246 12 12 12 745246 12 12 12 12 12	16 745157 8	Tesser 12 12 12 12 12 12 12 12 12 11 745246 6 6 6 1	7438 12 12	14 74524D 12 12 12 12	Ξ	IN 6331	88/342 NZ		2/ 6/57+2 02	25 / +5240	SF SPARE	\$42344 92	2N 2.7	24 741.5/93	2N 5N	2N 74500		ĥ	36	Z/ E6/57#2 DE	0 35 745263 5 10	36 745253	3H 74.5253	3K 6331		E/ 2/ 20202 12 12	E/ E/ Z/ Z/ +052/ AF	6+F9 V4	48 6349

Rev. C (Sht. 15 of 15)

4-Way Controller

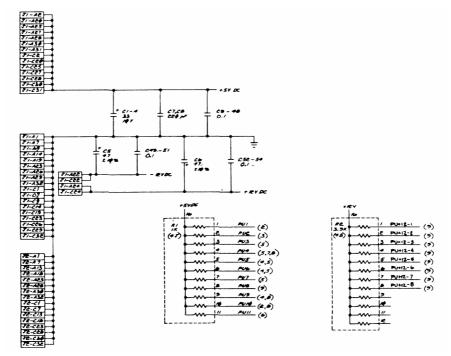
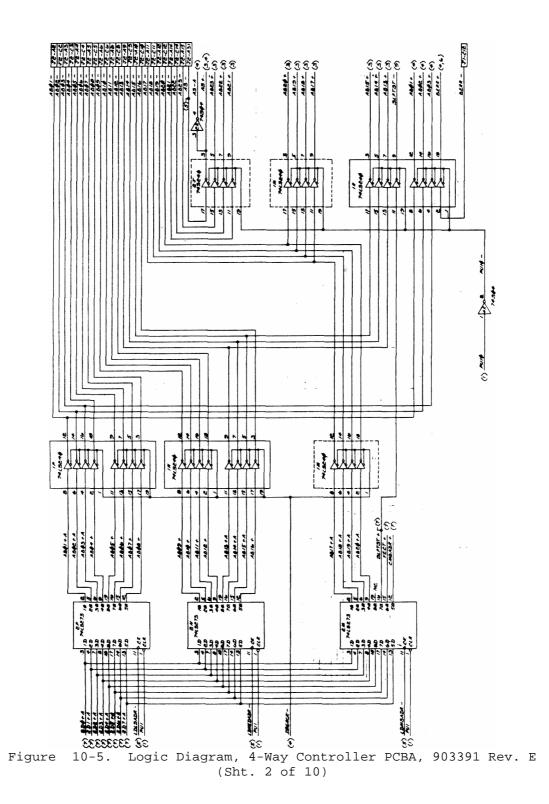
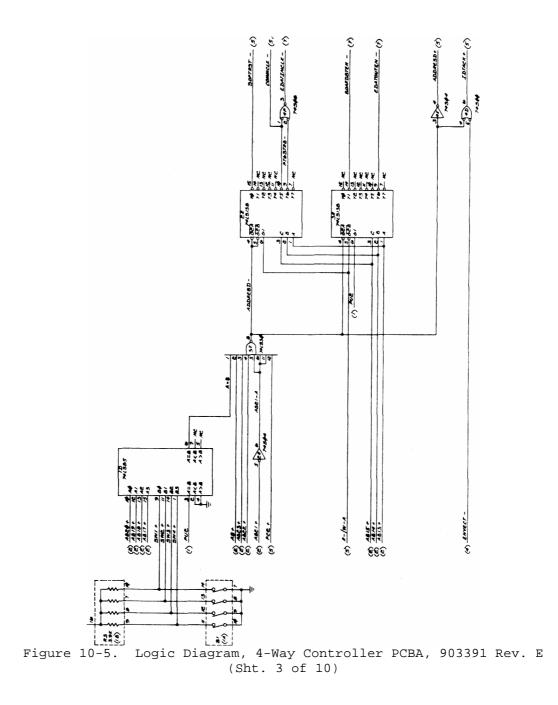
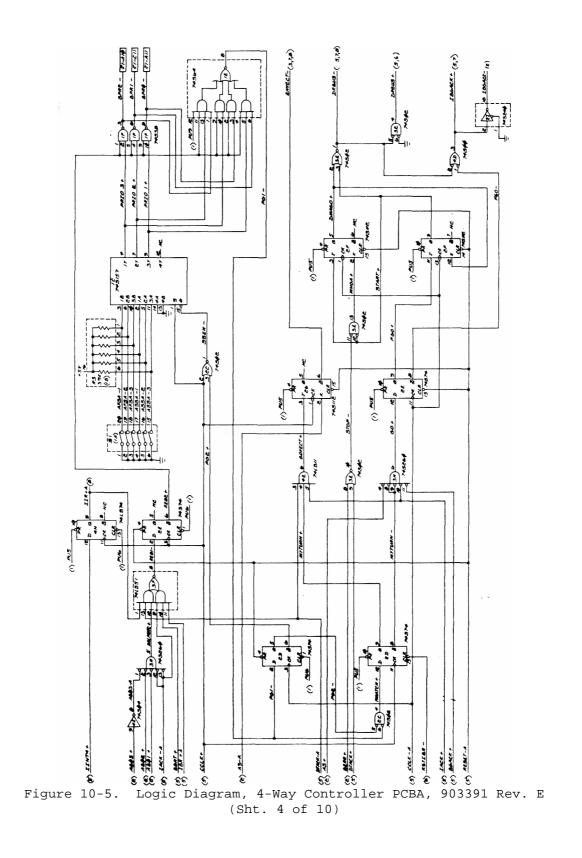


Figure 10-5. Logic Diagram, 4-Way Controller PCBA, 903391 Rev. E (Sht. 1 of 10)







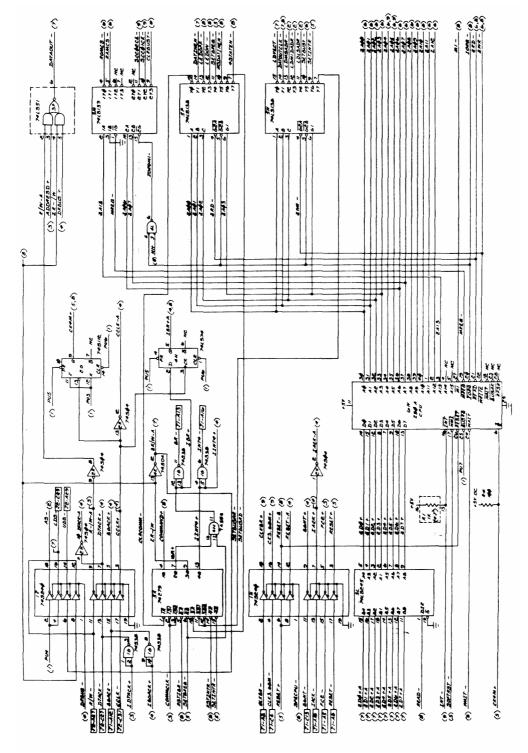


Figure 10-5. Logic Diagram, 4-Way Controller PCBA, 903391 Rev. E (Sht. 5 of 10)

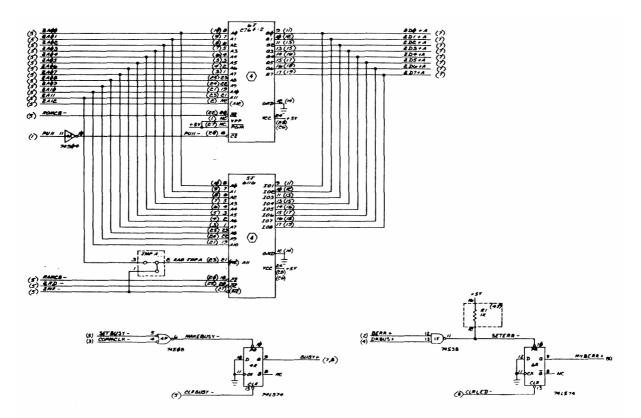


Figure 10-5. Logic Diagram, 4-Way Controller PCBA, 903391 Rev. E (Sht. 6 of 10)

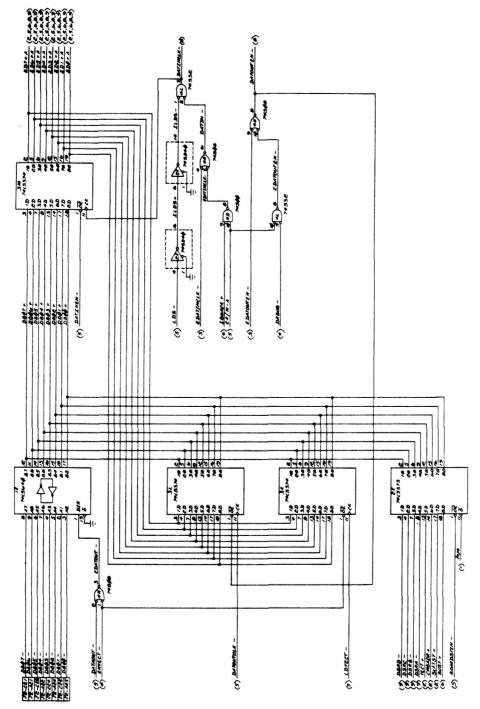
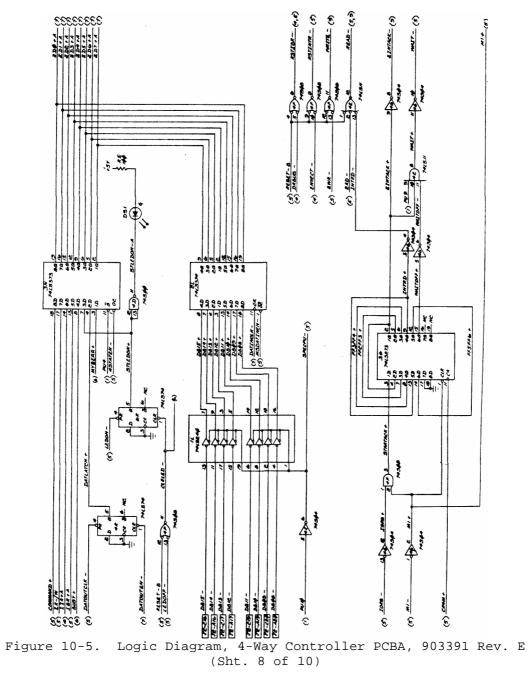


Figure 10-5. Logic Diagram, 4-Way Controller PCBA, 903391 Rev. E (Sht. 7 of 10)



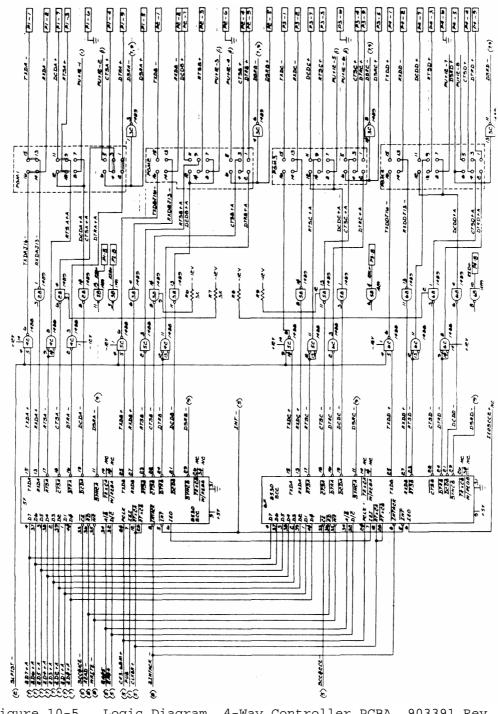


Figure 10-5. Logic Diagram, 4-Way Controller PCBA, 903391 Rev. E (Sht. 9 of 10)

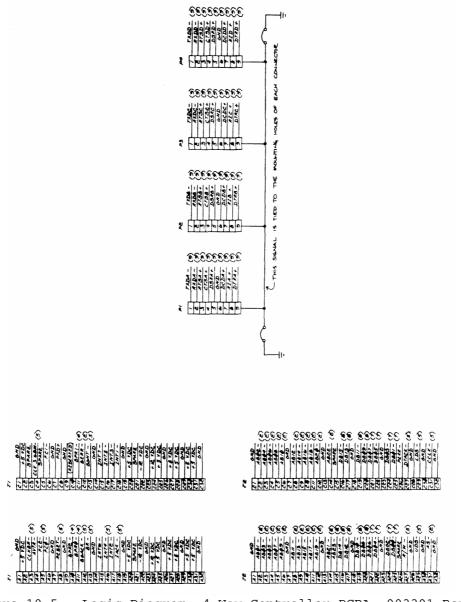


Figure 10-5. Logic Diagram, 4-Way Controller PCBA, 903391 Rev. E (Sht. 10 of 10)

Local Area Network Controller

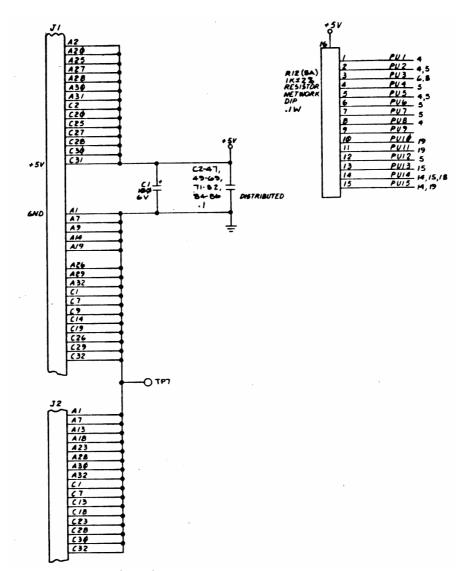


Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 2 of 20)

IA								
	SPARE	T	T	1	T	1		[
2A	75175	18	1	\bigtriangledown		11		
			1	-	K-	11	1G	74538
4A	OIP SHATCH	13	18	\bigtriangledown			26	74564
		1		1	1-		36	74574
				1		l t	đG	7415112
					1	1 t	56	74532
		1	1	1.		11	66	74532
IB	746112	5	5	\square	\square	l f		
28	74502	5	5	19	1			
38	75/74	18	18	\square	\triangleright	l f	IH	SPARE
		1	1			l t	2H	7415374
5B	741504	9	10	10	19	1 T	ЗН	7415374
\backslash	\sim	19	1	\square	\square	1 T	4H	741510
68	741551	9		\square		l t	5H	74LSØ8
				[l t	6 H	74Ø7
								\geq
10	74574	5	5	\bigtriangledown				
26	74500	5	9	10	18			
36	74511	4	5	19			13	7415244
40	741574	19	19					\sim
5C	7415112	5		\square			25	74L5273
60	74L52Ø	9	9				ЗJ	7415374
							43	SPARE
10	745240	4	4	5	9			
	\sim							
20	745260	4	5			F	IK	745240
30	74504	4	4	5	5			\geq
	\sim	18		\geq		I T	ZK	7415240
40	741500	9	15	18	19	Γ		\geq
50	741574	14	14	\geq		l r	3K	7415244
60	741854	14	\geq	\geq	\square	Г		\geq
						Γ	4K	7415374
						Γ	5K	68A54
IE .	74538	4	5	10	14	Γ		
3E	74551	4	19		\square			
4E	741674	18	19		\square	Γ	IL	746240
5E	741504	6	13	14	15		\supset	>
\geq	\sim	18	19	\geq	\square		21	7415240
6E	741551	9	17	\leq		E	\geq	\geq
						Γ	31	7415374
							AL	7415374
/F	745157	4	\square	\square			5L	SPARE
3F	74502	4	5	5	5		6L	7416244
4F	74L5Ø8	5	18	18	19		\geq	\geq
5F	7415138	10	\square	\square				
65	7415138	10		\leq		and the second		

COMPONENT MAP

						IM	745240
_					diam.	2	\geq
	4	4	4	4		214	74LS174
	4	\swarrow		\leq		3M	745244
	4	5	\leq	\leq			\geq
	19	19			Manual Providence	4M	741.6244
	10	NO	10	10		2	$\geq \leq$
	9	10	18	4			
	ļ					6M	74LS1/2
			L				
_	ļ	L	L				
	20	K	\leq	4		IN	74L524Ø
	20		\leq	\leq		_	\geq
	19	19	19	\leq		ZN	7415283
-	10	15	16	18		3W	74L524Ø
	17	17				-	\geq
			\leq	\leq		AN	745133
						5N	GATE ARRAY
_	L						
	14	14	14	14			
	14	14	14	14			
	14		\leq	\leq		IP	74L524Ø
	2Ø			\leq		\geq	\geq
						2P	7415374
						3P	74LS24Ø
-							\geq
-						4P	7415244
	11	11	11	11		2	\geq
	11	11	11	//			
	11	11	11	11			
	11	11		11			
	//	//	//	11			
	11	11	11	11		IR	7416240
_	16		\square				\geq
	16		\square	\square		2R	7415374
						ЗR	SPARE
						4R	SPARE
	12	12	12	12			
	12	12	12	12		5R	6801
	12	12	12	12			
	12	12	12	12			
	13			\square			
	16		\square				
J					Contraction		
J	10	14	14	14	and the second se		
1	14	15					
]					and the second se		
J					access (Mar)		
1	and the second se					and the second se	

6 8

13 13

13 13 13

7 7

10 10 10 10

10 10 10 10

7 7

9 9

10 10 10 10

13 13 13

7 7 7

 /

/

/

Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 3 of 20)

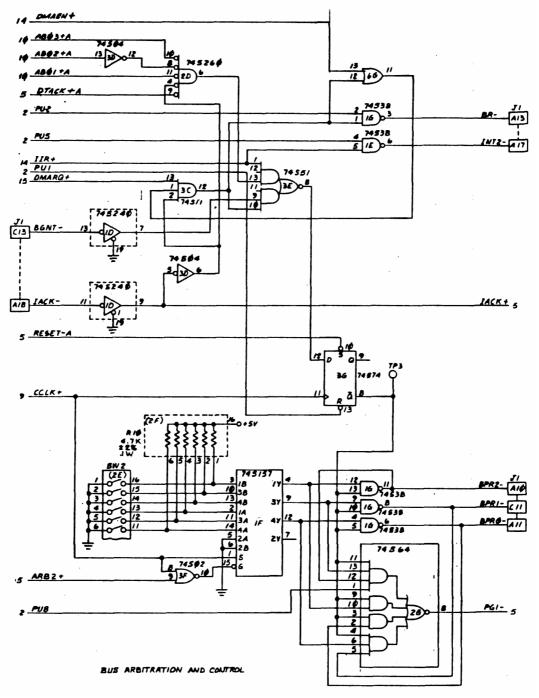
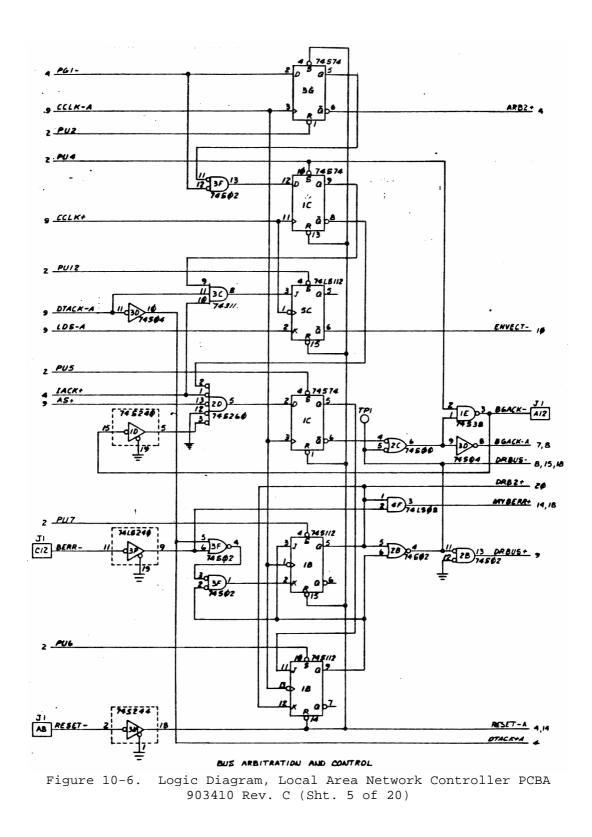
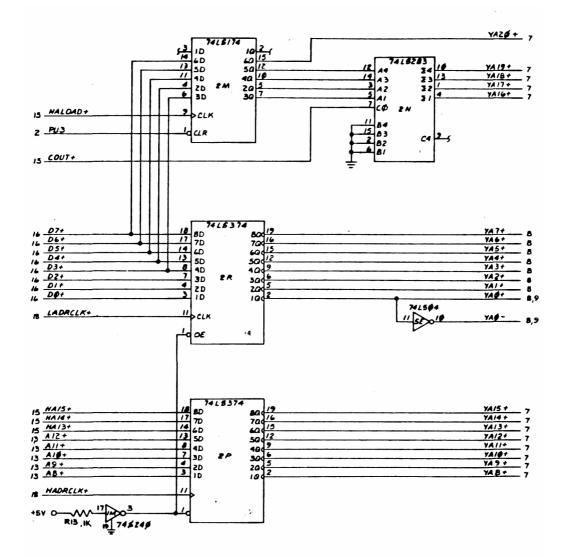


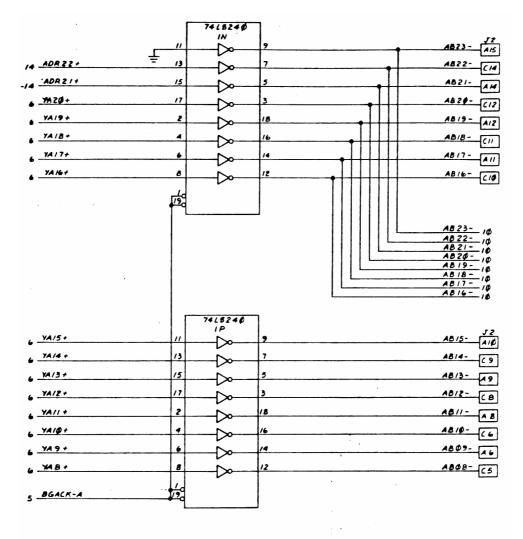
Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 4 of 20)





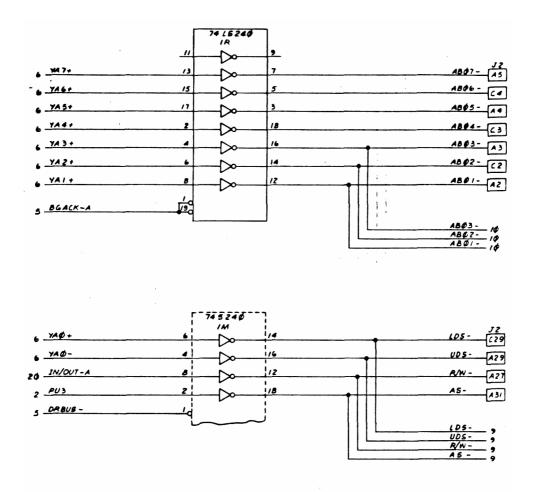
DMA ADDRESS GENERATION

Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 6 of 20)



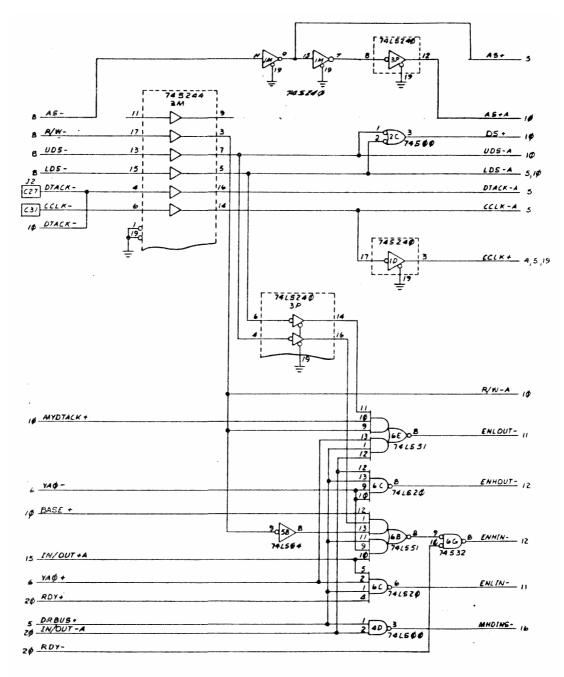
DMA ADDRESS DRIVERS

Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 7 of 20)



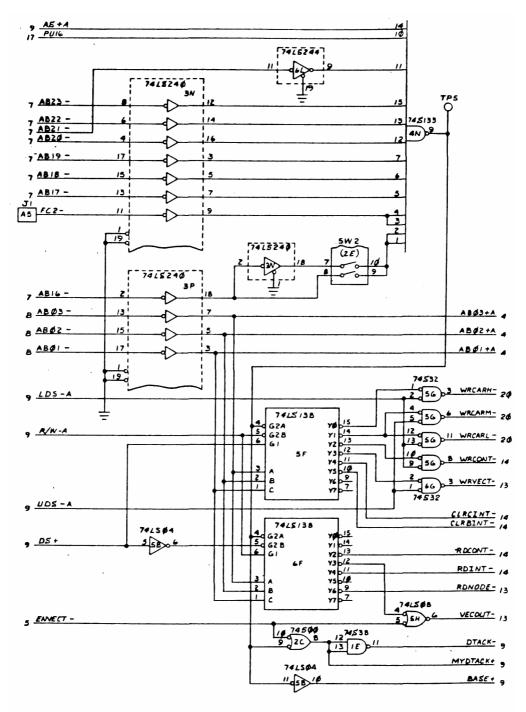
DMA ADDRESS AND CONTROL DRIVERS

Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 8 of 20)



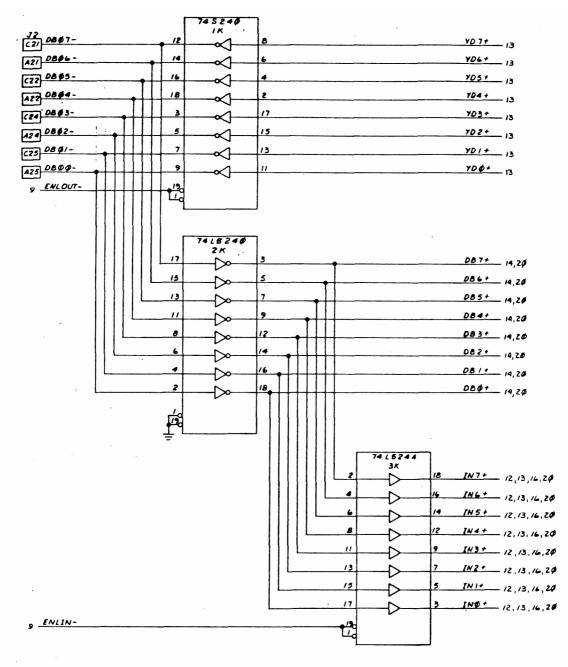
BUS CONTROL BUFFERS AND DATA BUS GATING

Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 9 of 20)



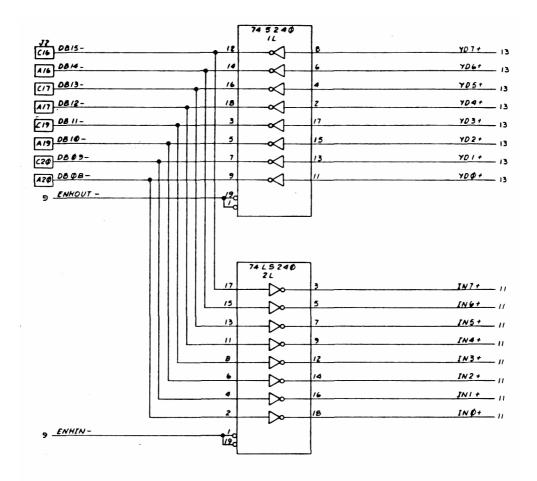
1/0 ADRRESS DECODE

Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 10 of 20)

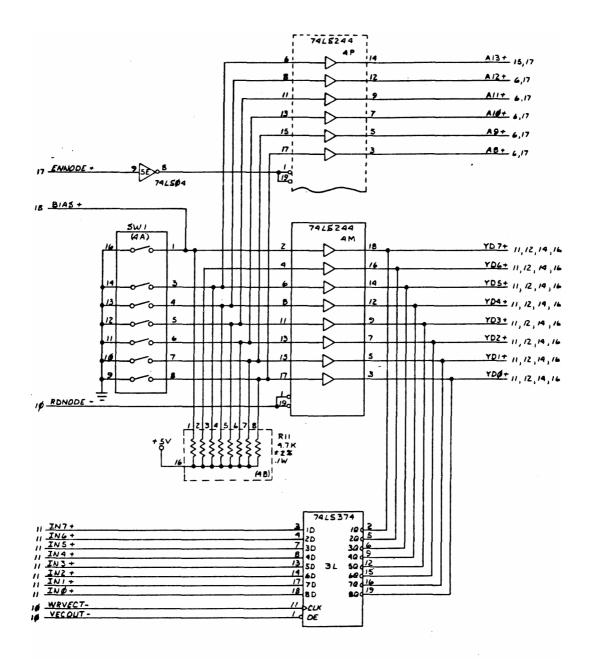


LOWER DATA BUS BUFFERS

Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 11 of 20)

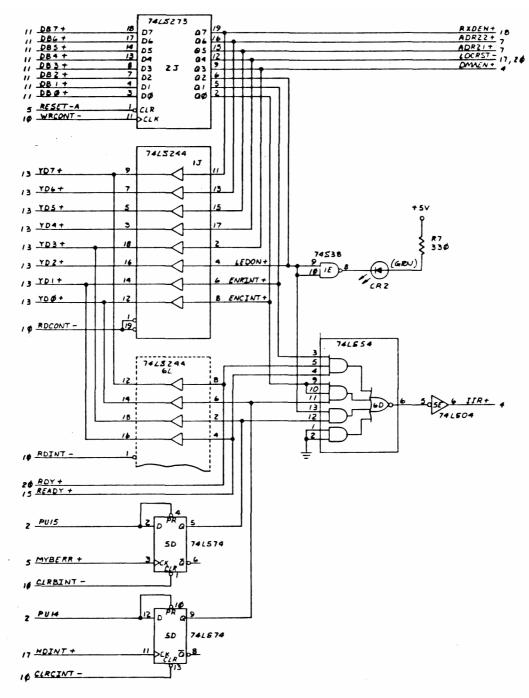


UPPER DATA BUS BUFFERS Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 12 of 20)



NODE ADDRESS REGISTER AND INTURRUPT VECTOR REGISTER

Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 13 of 20)



CONTROL REGISTER AND INTERRUPT LATCHES

Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 14 of 20)

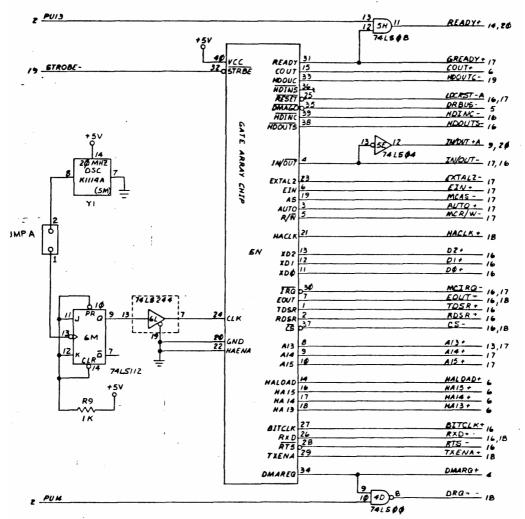
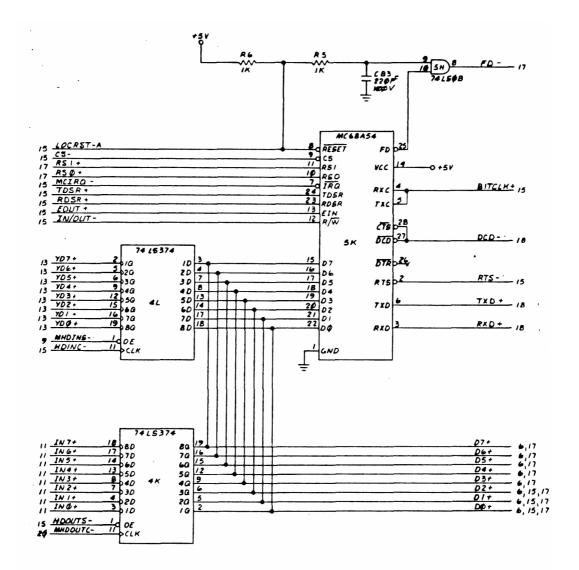
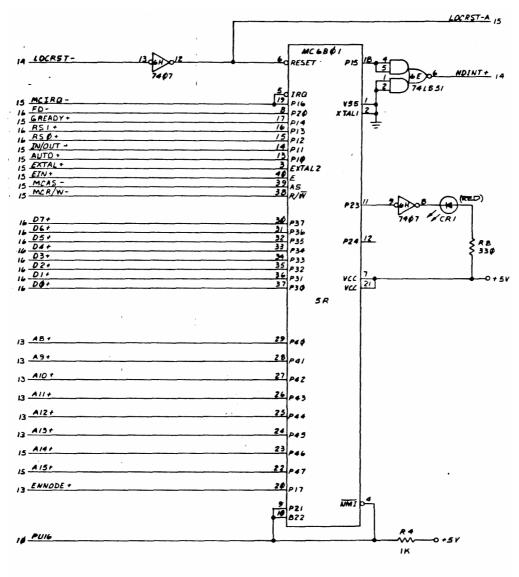


Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 15 of 20)



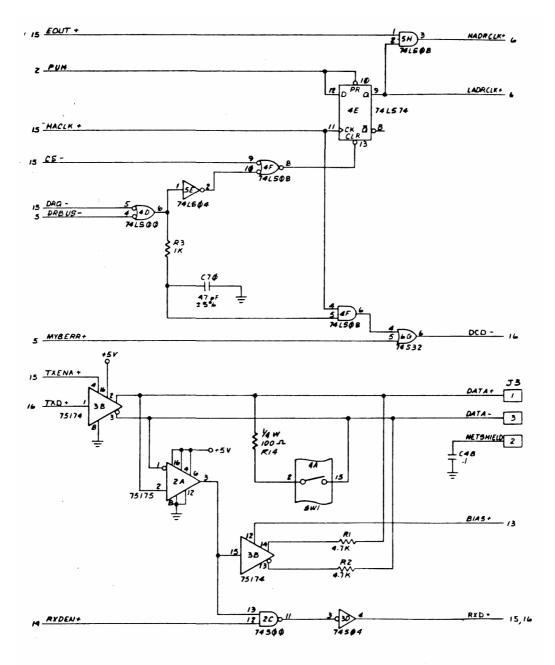
CHIP SET DATA LATCHES AND ADLC CHIP

Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 16 of 20)



MC6BOI MPU

Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 17 of 20)



DMA ADDRESS CONTROL AND NETWORK TRANSCEIVERS

Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 18 of 20)

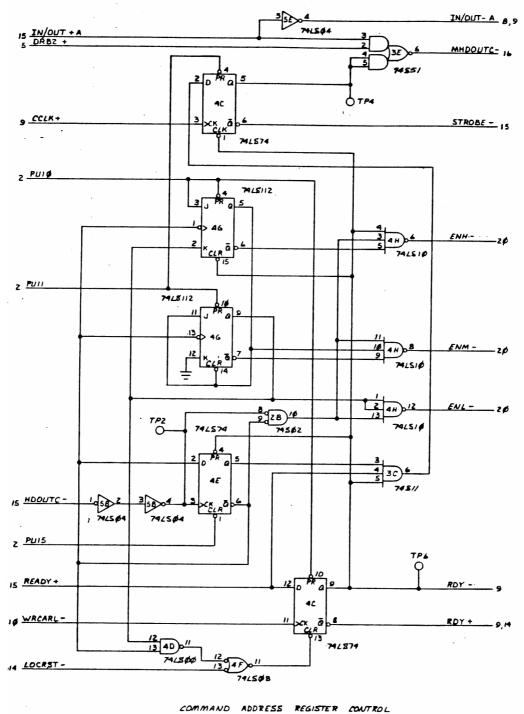
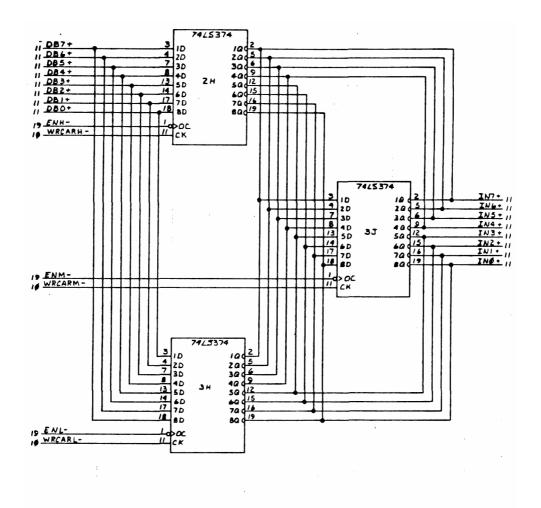


Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 19 of 20)



COMMAND ADDRESS REGISTER Figure 10-6. Logic Diagram, Local Area Network Controller PCBA 903410 Rev. C (Sht. 20 of 20)

14	74415240	11	/3	19	19
		19	19		
18	74 F/39	5	13		
10	74FE40	B	13	13	13
-		13	13	13	13
ID	745240	16	16	16	16
<		16	16	16	16
IE.	7415132	13			
IF	74415244	17	n	17	17
		17	17	17	17
16	745244	1B	18	18	18
		18	48	18	18
14	74F240	16	16	16	16
		19	19	19	19
15	74A15240	10	10	1\$	10
<hr/>		10	10	NØ	10
IK	74538	15	15	15	
11	74F24Ø	160	16	16	16
<u> </u>		16	16	16	No
1M	74F244	15	12	12	R
~		12	12	12	12
IN	74ALS244	12	12	12	12
		12	12	12	12
IP	74ALSE40	12	12	12	12
<u> </u>		12	12	12	12
ZA	SPARE				
EB	74F244	/3	13	13	
20	DISCRETE				
	RESISTORS				
2 D	74AL5163	16			
2E	74ALSE44	17	17	17	17
		17	17	17	17
2F	74AL5374	17	\smallsetminus	\smallsetminus	
26	74AL5374	10	\smallsetminus	\smallsetminus	
2#	74L524¢	13	14	14	14
		14	14	14	14
27	74A15374	14	\smallsetminus		\smallsetminus
2K	74AL5244	1\$	1¢	10	10
		14	1¢	14	14
21	74AL5163	16	\smallsetminus	\bigtriangledown	
2M	74F24¢	ø	"	"	"
		"	15	15	15
EN	DISCRETE				
	RESISTORS				
21	SPARE				
-					

COMPONENT MAP

34	74 F 175	19			
36	74AL574	19	19	\sim	\sim
30	74538	11	19	19	
30	74ALS/63	110	K	K	
3E	SPARE				
F					
34	74F244	17	17	17	17
130	/+/2+4	17	17	17	
-					77
36	74F244	18	18	10	18
<u> </u>		18	18	18	18
34	74ALS/63	16		\geq	
37	74ALSE44	AP	10	14	10
L		10	A\$	NØ.	Þ
3K	74F244	10	10	10	14
		14	10	N	N¢
31	74AL5/63	10		\geq	\geq
34	74AL5374	11	\geq	\geq	\searrow
3~	74ALSE40	//	"	"	"
		"	"	"	- //
3P	74ALSOO	"	"	"	
4A	74ALSOO	19	19	19	19
48	74ALSØB	13	19	19	
40	74F10	12	19	23	$\overline{}$
4D	74F244	20	20	EØ	20
		20	20	20	20
48	74F244	20	20	EØ	20
		2¢	20	20	20
4F	74FE44	20	EΦ	20	20
		20	20	20	eø
46	74 F 2 4 4	9	9	9	3
40		9		5	5
	74AL5374	•	-	-	\leq
4 H			$\langle \rangle$	\geq	\sim
4 J	74AL5/38	13		$\langle \rangle$	$ \rightarrow $
4K	74ALS/75	14		\geq	$ \rightarrow $
42	74AL5/38	14		\sim	\rightarrow
4 M	74ALSI38	14			\geq
4 N	74F¢¢	7	15	15	15
4 P	74 FØB	//	"	15	15
					-
5A	74ALSKO	"	19	19	\geq
58	74 AL 574	/9	13	\geq	$ \ge $
50	74551	/7	23	\geq	\geq
5D	74ALS/69	EØ	\geq	\geq	\geq
5E	74AL5169	2 Ø	\searrow	\searrow	\geq
5F	74ALS/69	Zφ	$\overline{}$	\searrow	\geq
56	74585	•	\smallsetminus	\smallsetminus	\smallsetminus
5H	7415/3B	14	\smallsetminus		
55	9324	13	\triangleleft	\triangleleft	\triangleleft
5K	74 ALS 175	14		\triangleleft	\triangleleft
				~	<u> </u>

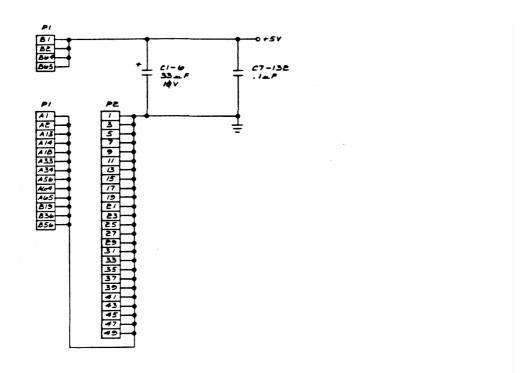
5L	74ALS32	10	"	12	15
5M	74ALSIØS	10	14	\smallsetminus	$\overline{\ }$
5N	SPARE	Ι			
5P	74AL5/49	15	15		
6A	7441500	17	17	19	19
68	74AL574	17	19		
60	74AL500	17	19	23	
6D	74AL5169	20			
6E	74ALSI69	20	~	~	~
6 F	74415169	20			
66	74585	•		7	$\overline{}$
64	74 F/38	7		\sim	\checkmark
65	74 F/38	7		\sim	7
6K	74AL5/38	7	\sim	\sim	\sim
62	74AL5/30	7	\sim	\sim	
6M	74AL500	14	15	15	.7
GN	74F\$B	10	17		
6P	74ALSOO	12	14	15	15
	ral ste				
7A	74AL5109	15	19		
78	SPARE	~			
	SPARE				
70	74F/39	2/			
			2/	\rightarrow	\rightarrow
7D	74AL5273	21	\geq	\geq	\rightarrow
7E					
-	74 AL5244	23	53	23	23
		23	23	23	23
75	74FE44	23 23	23 23	23 23	83 83
7/	745 244	23 23 23	23 23 23	23 25	23 23 23
		23 23 23 6	23 23 23 23	23 23 23	23 23 23 6
7F 76	74FE44 74FE44	23 23 23 6	23 23 23	23 25	23 23 23
7F 76 7N	74FE44 74FE44 27529	23 23 23 6	23 23 23 23	23 23 23	23 23 23 6
7F 76 7N 7J	74FE44 74FE44 27529 27529	23 23 23 6	23 23 23 23	23 23 23	23 23 23 6
7F 76 7N 75 7K	74FE44 74FE44 27529 27529 27529	23 23 23 6 •	23 23 23 23	23 23 23	23 23 23 6
7F 76 7N 7J 7K 7L	74FE44 74FE44 275E9 275E9 275E9 275E9 27529	23 23 23 6 6 6 6	23 23 23 23	23 23 23	23 23 23 6
7F 76 7N 75 7K	74FE44 74FE44 27529 27529 27529	23 23 23 6 6 6 6 6	23 23 23 23	23 23 23	23 23 23 6
7F 76 7N 7J 7K 7L	74FE44 74FE44 275E9 275E9 275E9 275E9 27529	23 23 23 6 6 6 6 6	23 23 23 23	23 23 23	23 23 23 6
7F 76 7N 7J 7K 7L	74FE44 74FE44 275E9 275E9 275E9 275E9 27529	23 23 23 6 6 6 6 6	23 23 23 23	23 23 23	23 23 23 6
7F 76 7N 7J 7K 7L 7M	74FE44 74FE44 275E9 275E9 275E9 275E9 275E9 27529 27529	23 23 23 6 6 6 6 6 6 6	23 23 23 23	23 23 23	23 23 23 6
7 <i>F</i> 7 <i>G</i> 7 <i>H</i> 7 <i>J</i> 7 <i>K</i> 7 <i>L</i> 7 <i>M</i> 7 <i>N</i>	74FE44 74FE44 275E9 275E9 275E9 275E9 275E9 275E9 275E9 275E9 275E9	23 23 6 6 6 6 6 6 6 7	23 23 23 23	23 23 23	23 23 23 6
7 <i>F</i> 7 <i>G</i> 7 <i>H</i> 7 <i>J</i> 7 <i>K</i> 7 <i>L</i> 7 <i>M</i> 7 <i>N</i>	74FE44 74FE44 275E9 275E9 275E9 275E9 275E9 275E9 275E9 275E9 275E9	 23 23 23 6 6 6 6 6 6 6 7 	23 23 23 23	23 23 23	23 23 23 6
7F 7G 7W 7J 7K 7L 7M 7N 7P	74FE44 74FE44 275E9	23 23 25 6 6 6 6 6 6 7 7 8	23 23 23 23	23 23 23	23 23 23 6
7F 76 7W 7J 7K 7L 7M 7N 7P 8A	74FE44 74FE44 275E9 274F(1) 28 275E9 274F(1) 28 275E9 274F(1) 28 274F(1) 274F(1) 28 274F(1) 274F(1	23 23 23 6 6 6 6 6 6 6 7 7 8 2/		23 23 23	23 23 23 6
7F 76 7H 7J 7K 7L 7M 7P 8A 8B	74FE44 74FE44 275E9 274F(36) 274F(36	23 23 6 6 6 6 6 6 6 6 7 7 8 7 8 2/ 14		23 23 23	23 23 23 6
7F 76 7W 7J 7K 7L 7M 7W 7P 8A 8B 8B 8C	74FE44 74FE44 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 274F(38) 74F(38) 74F(38) 74A(5)(69) 74A(5)(69) 74A(5)374	23 23 6 6 6 6 6 6 6 6 6 7 7 8 7 8 21 14 22	1 M M 0 2 2 2 2	MMM	MMM
7F 76 7W 7J 7K 7L 7M 7W 7P 8A 8B 8B 8C	74FE44 74FE44 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 274F(38) 74F(38) 74F(38) 74A(5)(69) 74A(5)(69) 74A(5)374	23 23 23 6 6 6 6 6 6 6 6 6 7 8 7 8 7 8 21 14 22 24	2 / e / / / / e / c 2 2 2 2		MMM
7F 76 7W 75 7K 7Z 7M 7N 7N 7N 7P 8A 8B 8D 8D	74FE44 74FE44 27529 27529 27529 27529 27529 27529 5PARE 74F/38 74F/38 74AL5/69 74AL5/69 74AL5374 74F240	23 23 23 6 6 6 6 6 6 6 6 6 7 8 7 8 7 8 21 14 22 24	2 / e / / / / e / c 2 2 2 2		MMM
7F 76 7W 75 7K 7Z 7M 7N 7N 7N 7P 8A 8B 8D 8D	74FE44 74FE44 27529 27529 27529 27529 27529 27529 5PARE 74F/38 74F/38 74AL5/69 74AL5/69 74AL5374 74F240	23 23 23 6 6 6 6 6 6 6 6 6 7 8 7 8 7 8 21 14 22 24	2 / e / / / / e / c 2 2 2 2		MMM
7F 76 7W 7J 7K 7L 7M 7N 7N 7N 7N 7N 7D 8A 8B 8D 8D 8D 8E	74FE44 74FE44 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 27529 274F/38 74F/38 74F/38 74AL5/69 74AL5/69 74AL5374 74FE44	23 23 23 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6	2 / e / / / / e / c 2 2 2 2		MMM

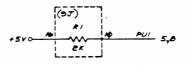
Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (2 of 24)

	COMPONENT	MAP

86	74F244	5	5	5	5										
		9	,	9	9					1					
BH	74415241	5	5	5	5		1		 	 1	\vdash				
									 		\vdash		 		
	745.0	-							 	 {	\vdash		 		
87	74F163	5		\geq	>				 				 		
BK	74 F163	5							 	 1					
BL	74F244	5	5	5	5				 				 		
		5	5	5	5				 				 		
BM	74F\$ 4	5	5	7	7		· · · ·								
		8	17												
8N	74F/38	8													
BP	74F138	8	\frown												
94	74AL5/69	21			\smallsetminus					1					
20	74AL5/69	21		1			1			 1					
90	74ALSE40	5	23	22	23		1			1					
		22							 						
90	RES NTWK	22		22	22										
Ê	220/330	22	22	22	23				 				 		
		23	23	23	23				 				 		
	(R9)								 		\vdash		 		
		23	23						 				 		
9E	74AL524Ø	23	23	23	23				 				 		
		23	23	23					 				 		
95	74F24Q	23		23	23				 						
		23	23	23	23										
96	SPARE														
94	74AL5244	9	9	9	9										
		9	9	9	9										
95	RES NTWK	4	5	9	9					1					
	2K	9	>	,						1					
	(1)	9	9	12	12										
		12	12	12						 1					
94	74 F163	5		1	\sim				 	 1					
94	74F153	8	\sim	~	~										
94	74F151	8	$\langle \rangle$	\sim	\sim								 		
	74F151		$\langle \rangle$	0	\sim						\vdash				
9/		8	\searrow	\sim	>				 		\vdash		 		
90	74FISI	8		\rightarrow					 		\vdash		 		
			·						 		\vdash		 		
											\vdash	· · · · · · · · · · · · · · · · · · ·	 		
AD H	SWITCH	•	9	9	9								 		
	(SI)	9	9	9	9										
										1					
							1	1		1					
							t			 1			 		
							1			 1			 		
			1										 		

Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (3 of 24) 10-120





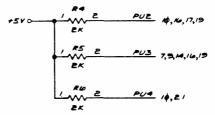


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (4 of 24)

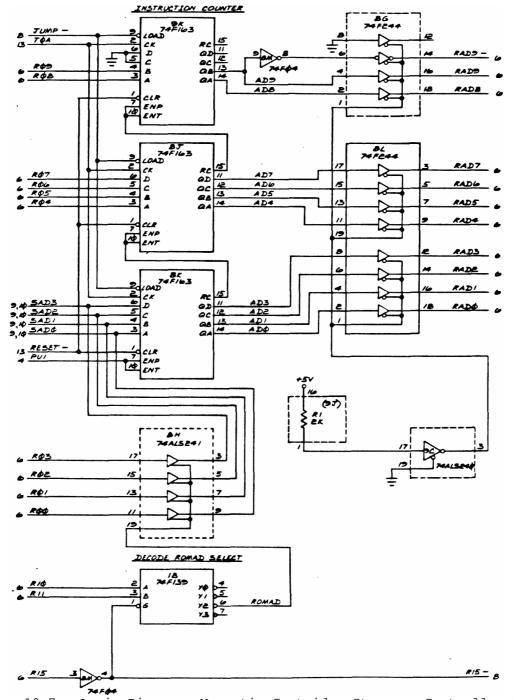


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (5 of 24)

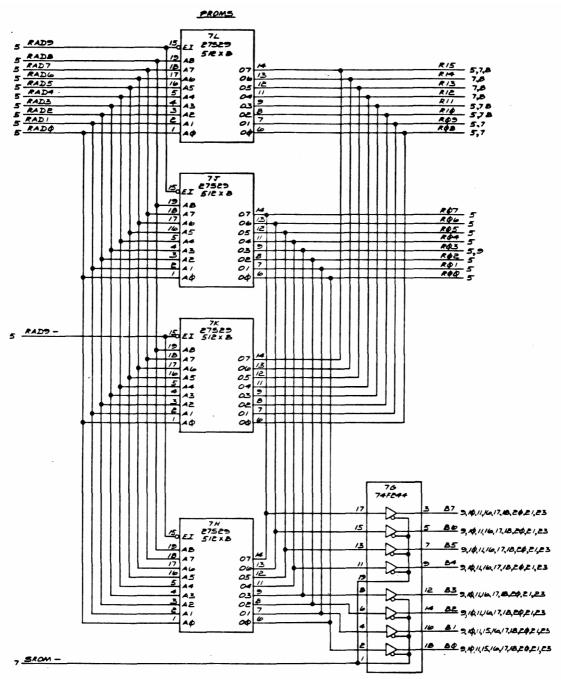


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (6 of 24)

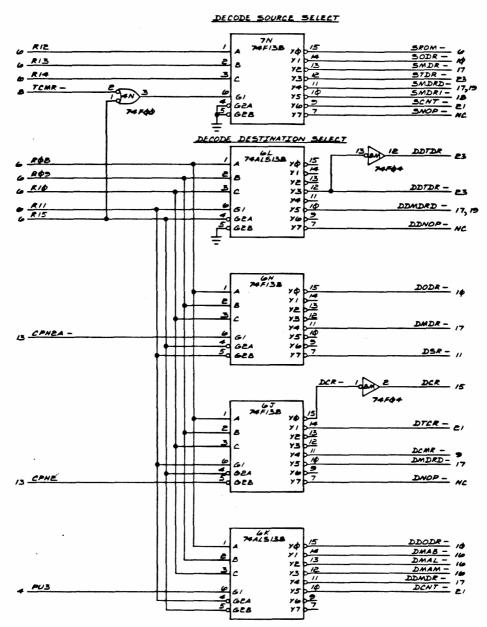


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (7 of 24)

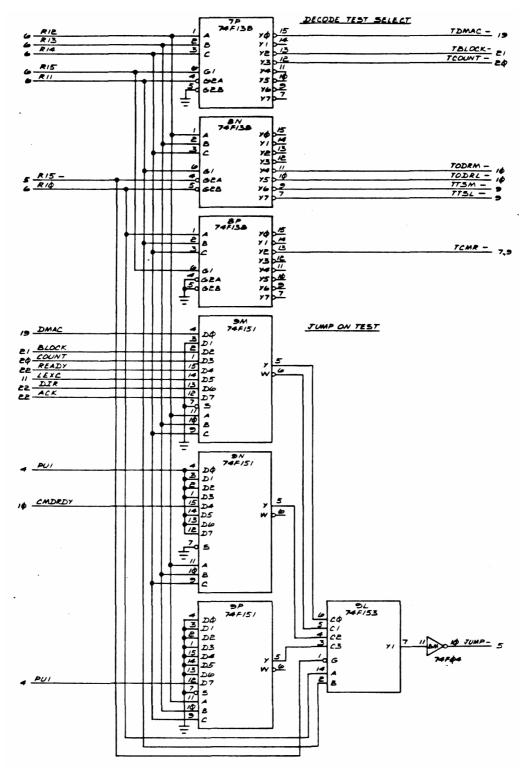


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (8 of 24)

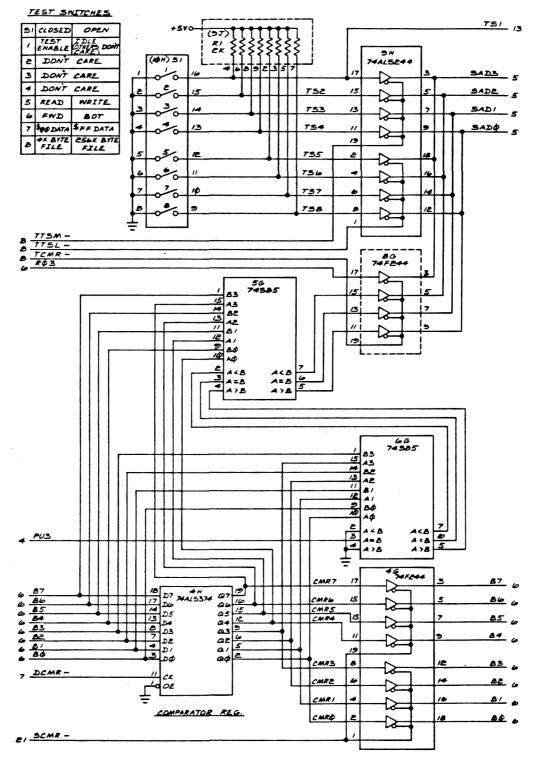


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (9 of 24)

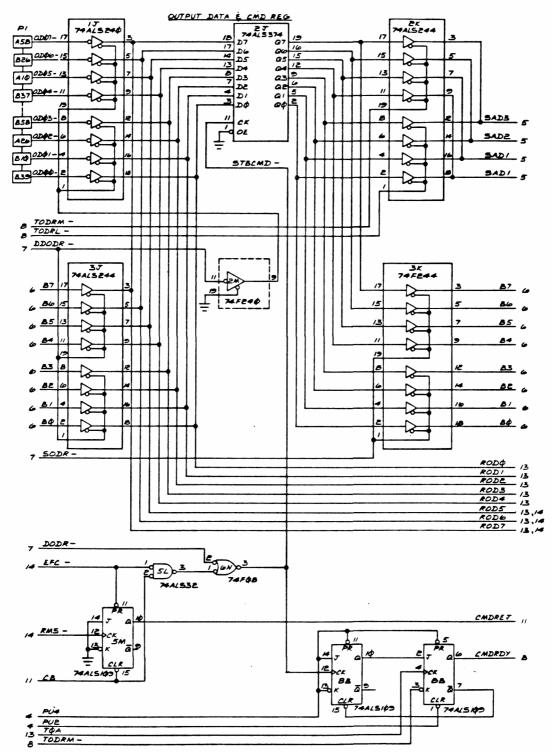


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (10 of 24)

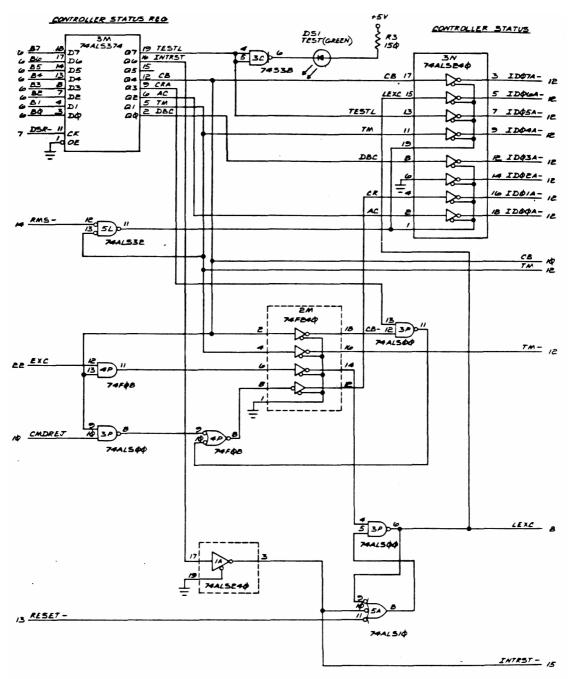


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (11 of 24)

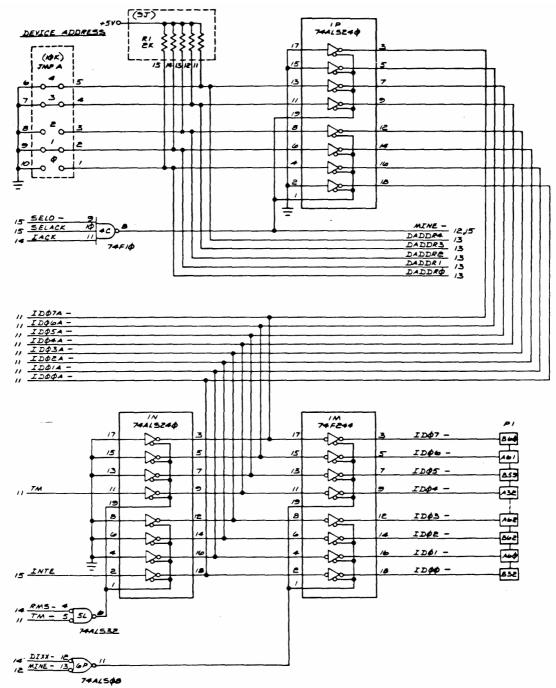


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (12 of 24)

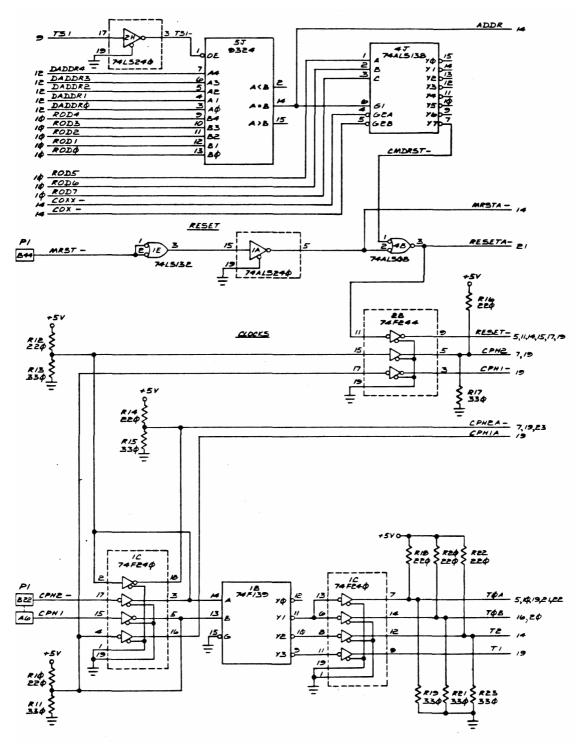
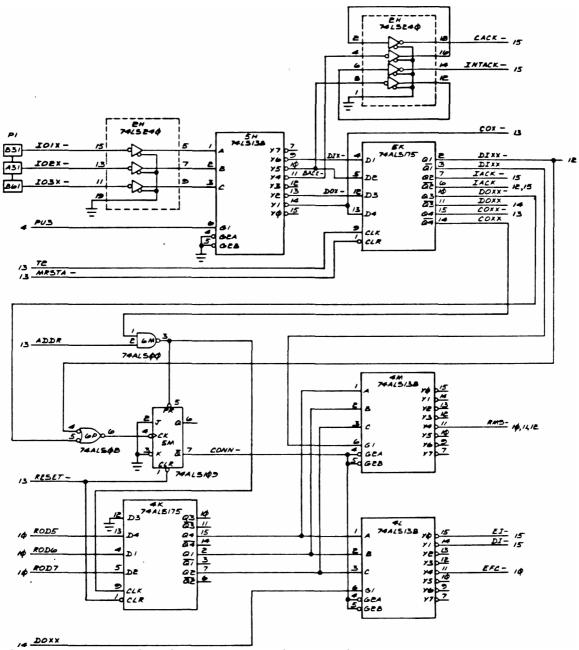
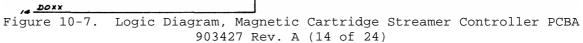


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (13 of 24)





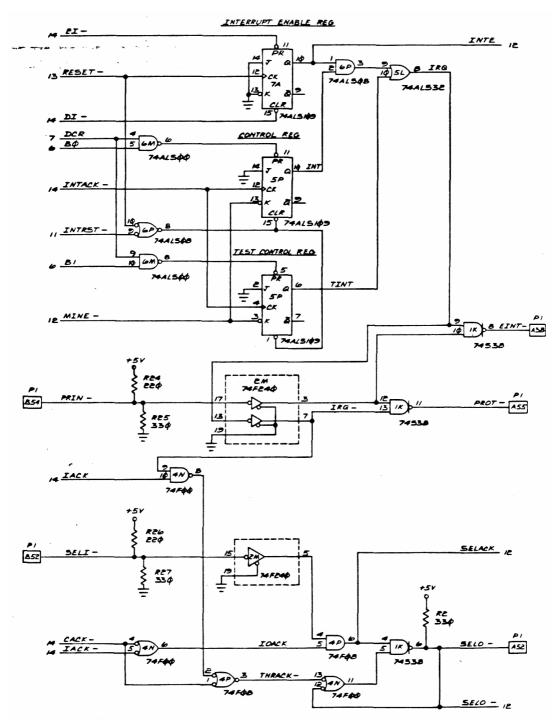


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (15 of 24)

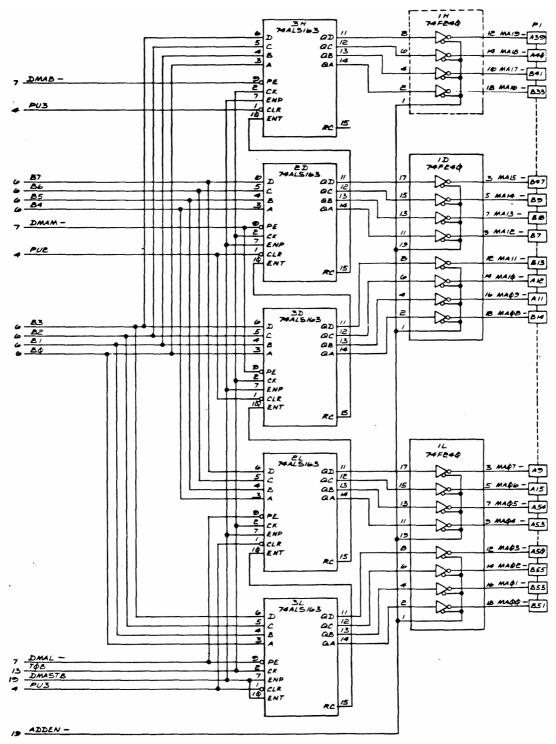


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (16 of 24)

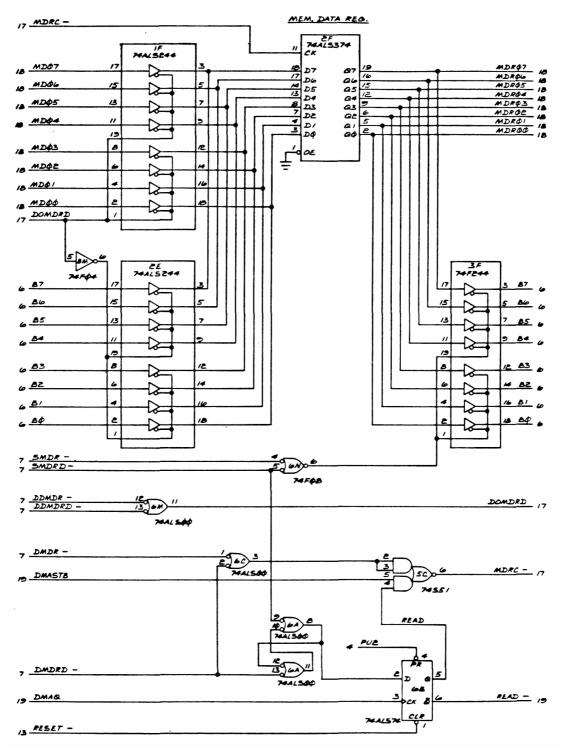


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (17 of 24)

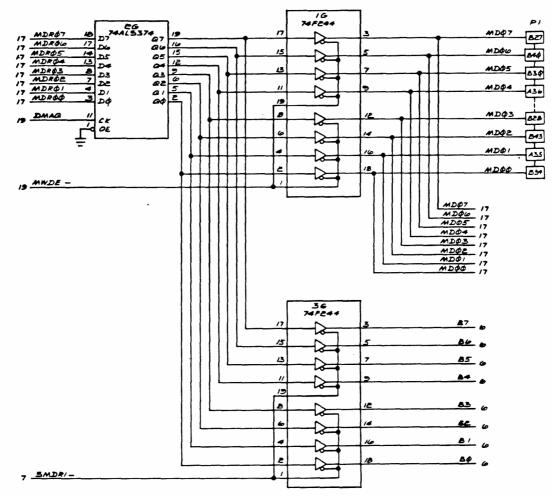


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (18 of 24)

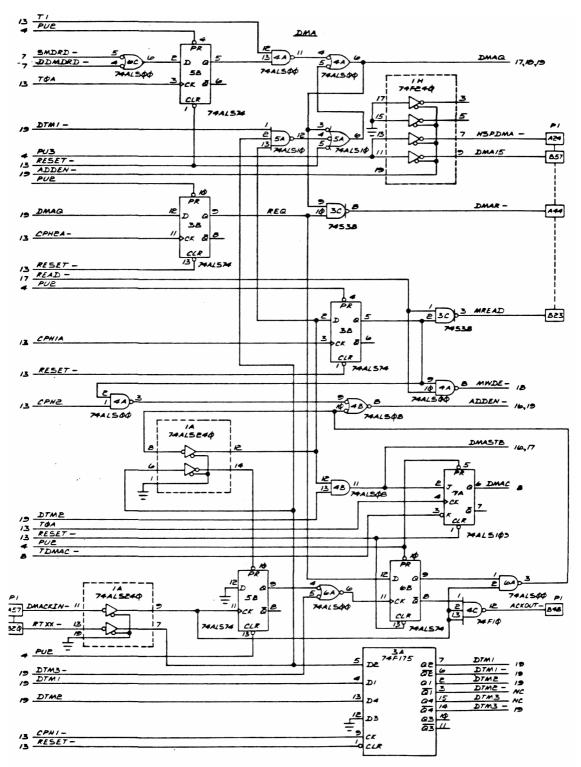


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (19 of 24)

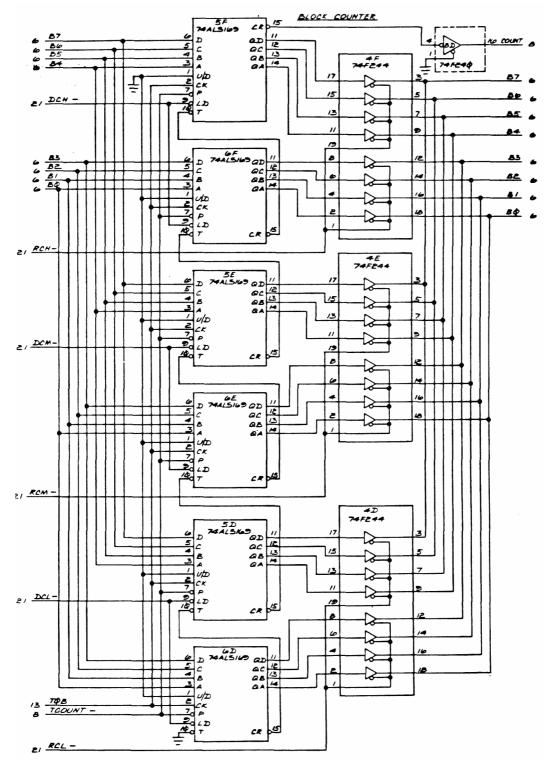


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (20 of 24)

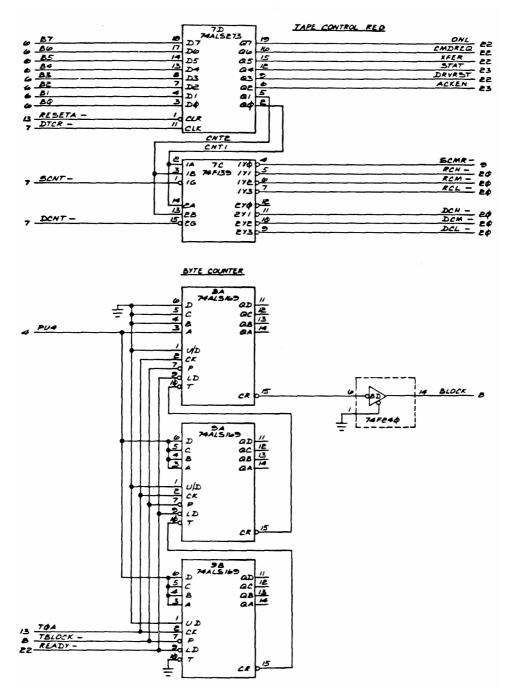


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (21 of 24)

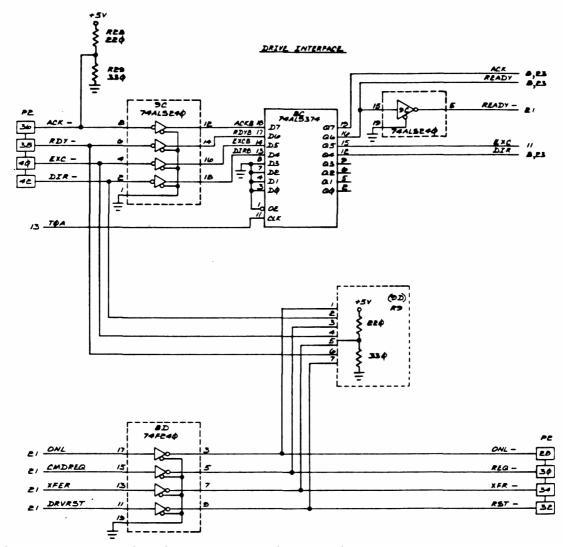


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (22 of 24)

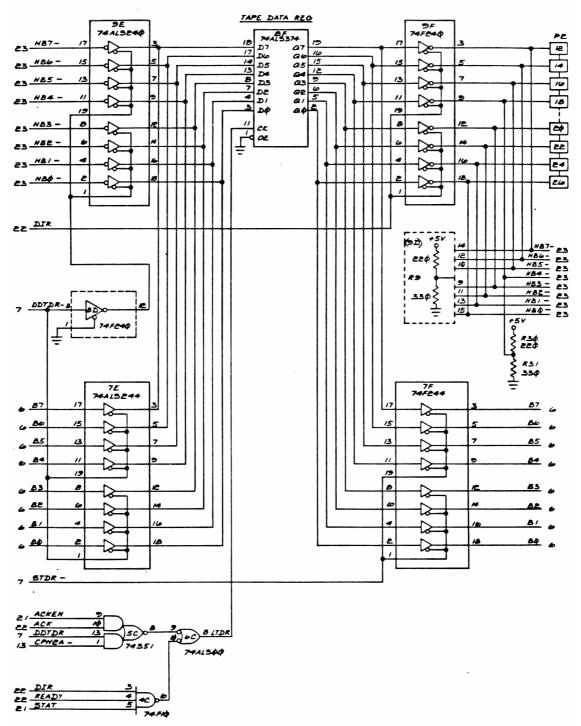


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (23 of 24)

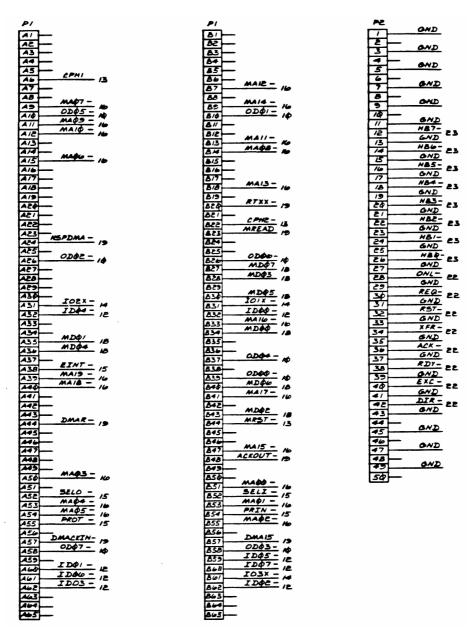
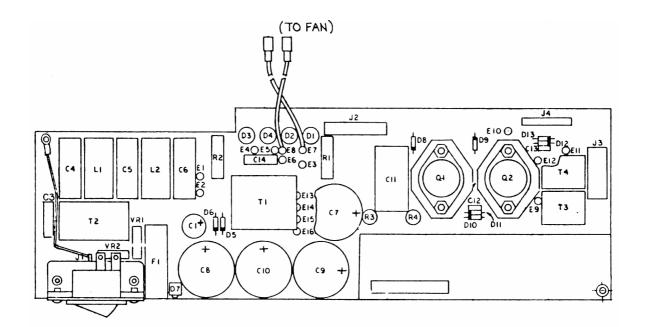


Figure 10-7. Logic Diagram, Magnetic Cartridge Streamer Controller PCBA 903427 Rev. A (24 of 24)

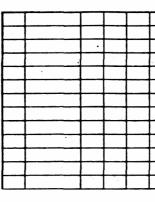


000447 001	T4-5	E12				
903443-001 AND	T4-6	EII				
903443-002	T3-5	E۹				
2002-12-2002	T3-6	EIO				
903443-001	LOCATION VRZ		50			
	E3	E6	ر ر	0		
903443-001	51-4	E5		57		
AND 903443-002	51-3	E2	4	56		
	51-2	E4		55		
	51-1	EI		54		
903443-002	E14	E15	50			
903443-001	E14	E16				
	E13	E15				
BFIS PART NO.	FROM	то	LITEM NO.			
WIRE LIST						

Figure 10-8. Logic Diagram, Power Supply Input Module PCBA, 903443 Rev. E (Sht. 1 of 1)

COMPONENT MAP

U 9	MPQ3725	6			6
UI.	LM339	3	4	4	4
UZ	LM839	4	4	4	4
13	LM539	4	4	4	4
4	JM358	5	5		
ÜS	Luss99	5	5	5	5
26	4011	5	5	5	5
5	7905	6			
08	זפר	6			
U9~	3725	6			
UIØ	7812	6			



_	_	_	_	
		-		
			·	

Figure 10-9. Logic Diagram, Power Supply Output Module PCBA, 903446, Rev. B (Sht. 2 of 6)

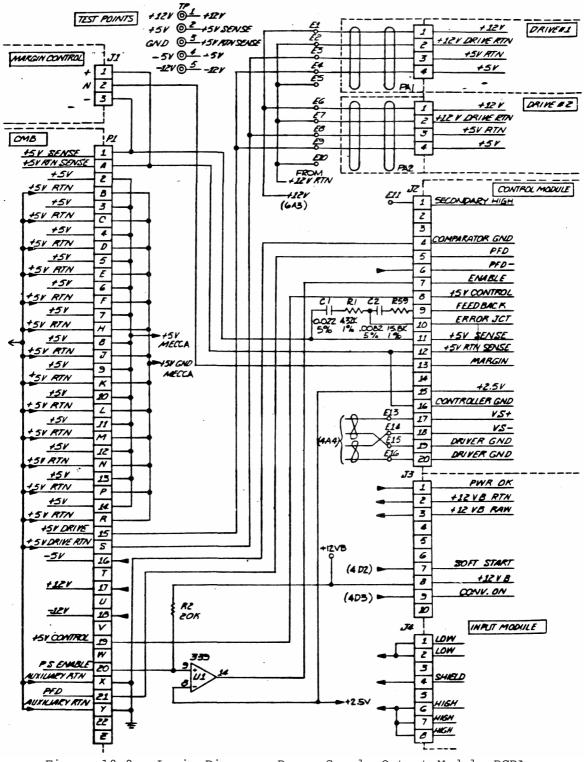


Figure 10-9. Logic Diagram, Power Supply Output Module PCBA, 903446, Rev. B (Sht. 3 of 6)

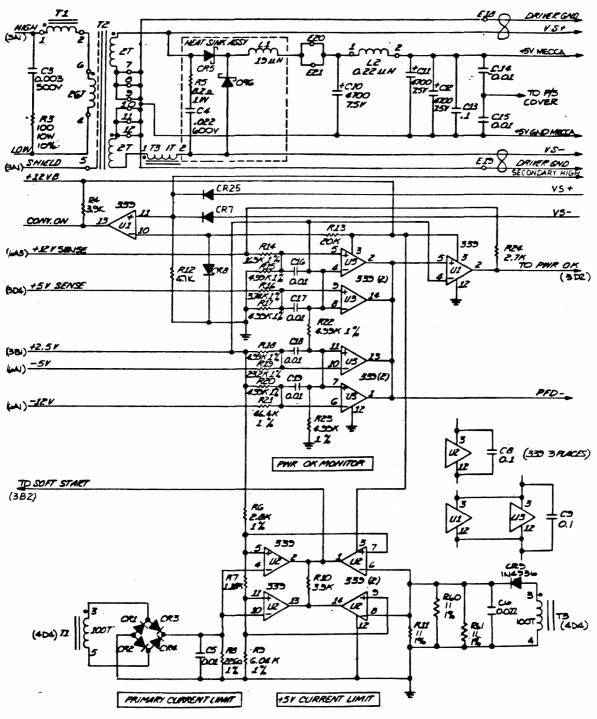
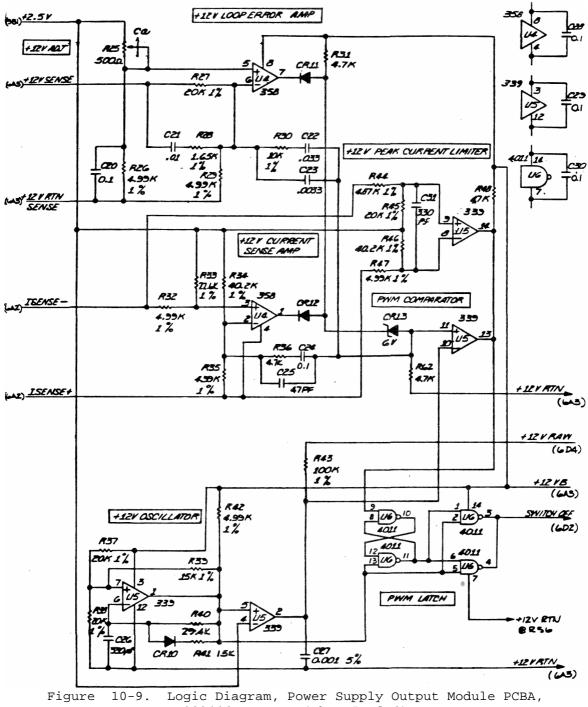
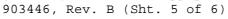


Figure 10-9. Logic Diagram, Power Supply Output Module PCBA, 903446, Rev. B (Sht. 4 of 6)





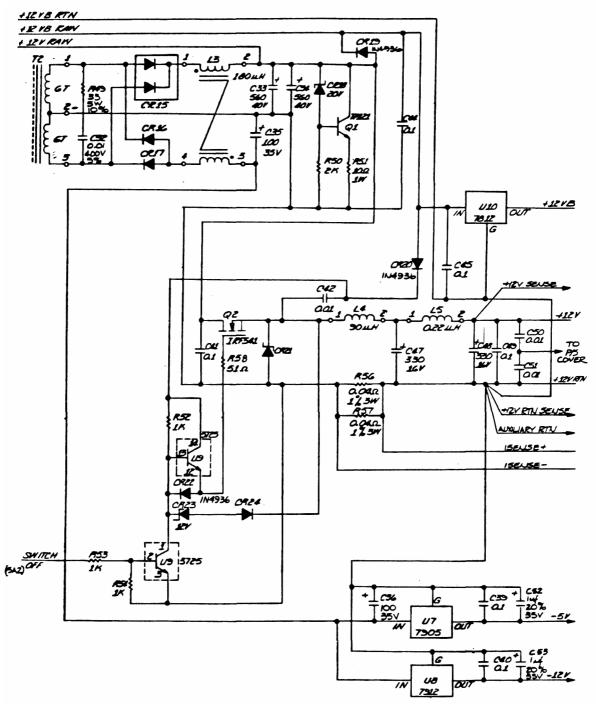


Figure 10-9. Logic Diagram, Power Supply Output Module PCBA, 903446, Rev. B (Sht. 6 of 6)

Power Supply Control Module

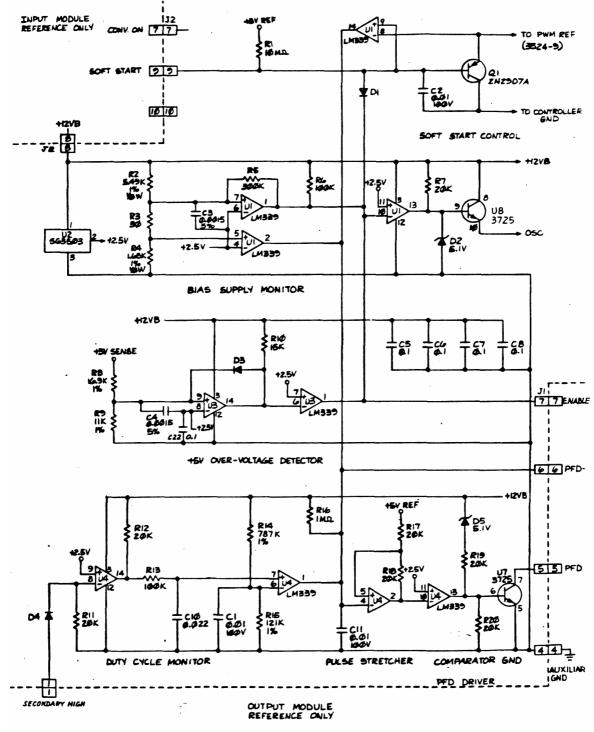


Figure 10-10. Logic Diagram, Power Supply Control Module PCBA, 903404, Rev. A (Sht. 2 of 3)

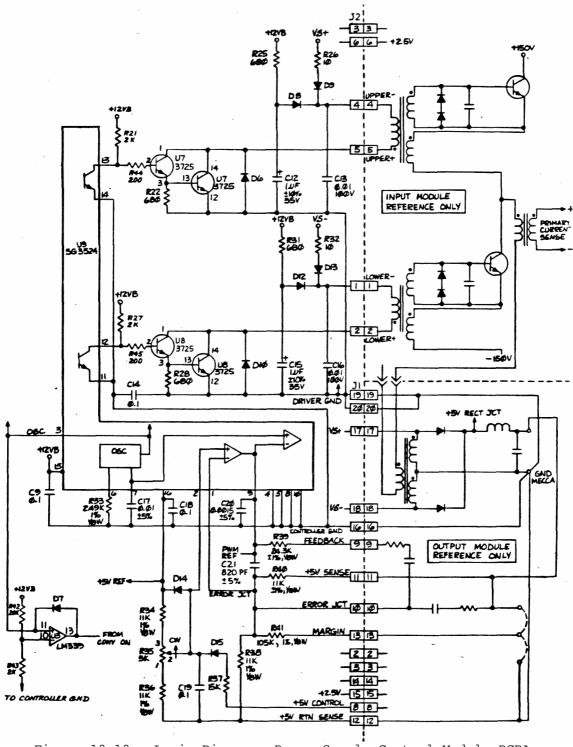


Figure 10-10. Logic Diagram, Power Supply Control Module PCBA, 903404, Rev. A (Sht. 3 of 3)